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18 November 2026

Design of a High Step-up Partial-Power Quadratic DC-DC Converter for Wide-Voltage Range Photovoltaic Applications

Federico Emir Ricci, Stefano Cerutti, Francesco Musolino, Paolo Stefano Crovetti
Department of Electronics and Telecommunications (DET), Politecnico di Torino
federicoemir.ricci@studenti.polito.it, {stefano.cerutti, francesco.musolino, paolo.crovetti}@polito.it

***Abstract*—This work presents the analysis, design, and simulation of a new multi-stage Partial Power Processing (PPP) converter with Input-Parallel-Output-Series (IPOS) topology for photovoltaic (PV) applications. An *ad hoc* design flow was developed to assist in the converter design in the 15V-45V input voltage range and 0 W-680 W power range, while simultaneously optimizing the efficiency at the desired rated voltage.**

The PPP approach enables part of the power to bypass the converter, achieving high efficiency and reduced component stresses. The integration of multi-stage and PPP approaches allows the achievement of a flat efficiency curve across the entire voltage range, a desirable feature for PV applications. The simulation results demonstrate a California Energy Commission (CEC) weighted efficiency of 97.2 % and European (EURO) efficiency of 96.8 % at rated voltage.

***Index Terms*—Partial Power Processing (PPP), Input-Parallel Output-Series (IPOS), Wide input voltage range, Photovoltaic systems, Efficiency optimization**

I. Introduction

In 2023, rooftop photovoltaic (PV) modules accounted for the largest share of installations in the European Union, 33 % of which are in the residential segment, mainly due to increasing cost of electricity [1]. Among the various architectures of grid-tied PV systems, the *ac-module* configuration, also known as micro-inverter, has gained popularity due to its ease of installation and flexibility. It consists of a dedicated DC-AC power converter for each PV module that is usually mounted in the structural frame. Compared to centralized or string systems, this approach offers superior energy harvesting capabilities thanks to the distributed Maximum Power Point Tracking (MPPT), which eliminates the mismatches associated with different shading or orientations of the PV panels [2]. However, it may suffer from lower power conversion efficiency [3], due to the high voltage gain requirement. In addition, micro-inverters should be designed to work across a wide range of operating voltages and powers, given the tight dependence of the PV electrical characteristics on temperature, irradiance, and shading scenarios [4].

Several high step-up DC-DC converter architectures have been explored in the literature, including conventional boost converters, interleaved structures, multi-stage converters, switched-capacitor and switched-inductor techniques, as well as hybrid combinations of these approaches [5]. Among these, resonant converters, especially LLC converters, are widely utilized in high step-up and step-down applications due to their soft-switching capabilities, which enhance efficiency and power density, reduce switching losses and Electromagnetic Interference (EMI) [6], [7]. Additionally, they exploit the transformer to provide the galvanic isolation while simultaneously integrating the magnetic components for the resonant tank.

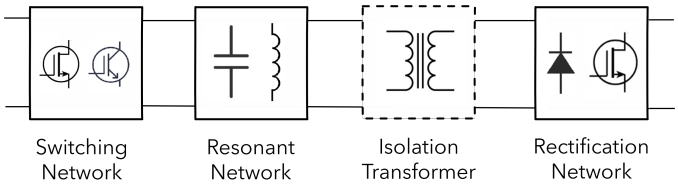


Fig. 1: General resonant converter. The isolation transformer is shown with dotted lines as its presence is not mandatory.

Conventional LLC converters are typically optimized to work in restricted range of working points. To overcome this limitation, variants of the resonant converter have been introduced to improve the converter performances on an wider gain range. These variations correspond to different alternatives for each of the fundamental building blocks shown in Fig. 1. For example, a Voltage Doubler Rectifier (VDR) is exploited in [8] to provide an additional voltage boost, while an extension of the voltage gain range is addressed in [9] by a topology-morphed rectifier and in [10] by a multi-mode modulation strategy of the switching network.

To further improve the conversion efficiency, some recent works introduce the Partial-Power Processing (PPP) technique [11], in which a fraction of power is directly transferred to the output [12], [13], or processed by a lower power stage responsible for the gain modulation [9], [14], [15]. This approach features the additional benefit of reducing the voltage and/or current stresses on the main converter components.

The converter proposed in this work combines the high efficiency and power density features of LLC converters with the electrical stress reduction offered by the Input-Parallel-Output-Series (IPOS) PPP approach [11]. In addition, the converter exploits a multi-stage configuration to specifically address the efficiency bottlenecks of a wide-range DC-DC converter. The approach of the proposed converter topology is described in

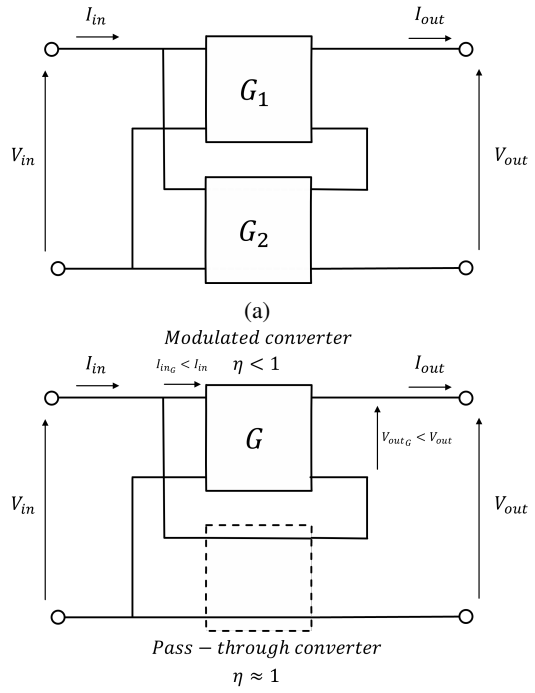


Fig. 2: System-level block diagram of the IPOS architecture. (a) General IPOS architecture with two conversion stages. (b) Modulated converter (MC) and pass-through converter (PTC) configuration.

Section II, followed by the design methodology in Section III. Section IV presents simulation results validating the proposed approach, including a discussion on loss modeling accuracy. Finally, Section V draws the conclusions and outlines future research directions.

II. Proposed Converter Topology

The conceptualization of the proposed converter topology takes advantage from the benefits offered by the PPP approach. The general block diagram of an IPOS-PPO architecture with two converter stages is shown in Fig. 2a, highlighting the parallel connection of the input ports and the series connection of the output ports. Fig. 2b is a particular configuration of the IPOS architecture, where one of the converters is a "Pass-Through" Converter (PTC), providing a direct path for a fraction of the total power, with unitary voltage gain and ideally 100 % efficiency [11]. As a consequence, the overall gain of the IPOS converter is uniquely determined by the gain G of the Modulated Converter (MC). The advantages of this configuration are an inherent increase in the overall efficiency of the full converter, since part of the power is delivered to the load with 100 % efficiency, and reduced voltage and current stresses in the MC due to lower processed power levels. However, this architecture imposes challenges in the design process:

1) *Topology restrictions*. The peculiar IPOS configuration in Fig. 2b requires the MC to adopt an isolated topology to prevent short-circuiting the input port. This design constraint not only restricts the set of eligible topologies for the MC, but also implies that, despite the galvanic isolation provided by the MC, the overall converter is non-isolated due to the direct path introduced by the PTC.
2) *Limitation of PPP benefits at high gains*. From the analysis of the converter topology in Fig. 2b, it is possible to derive:

$$\eta_{\text{sys}} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{(G+1)V_{\text{in}}I_{\text{out}}}{V_{\text{in}}(I_{\text{in}_\text{G}} + I_{\text{out}})} = \frac{(G+1)I_{\text{out}}}{G\frac{I_{\text{out}}}{\eta} + I_{\text{out}}} = \frac{G+1}{1+\frac{G}{\eta}} \tag{1}$$

where G is the voltage gain of the MC, $\eta < 1$ its efficiency, and η_{sys} is the overall system efficiency. From (1), it follows that $\eta_{\text{sys}} > \eta$, and the efficiency enhancement is more pronounced in scenarios where G is small, in which a larger fraction of the input power is processed by the PTC.

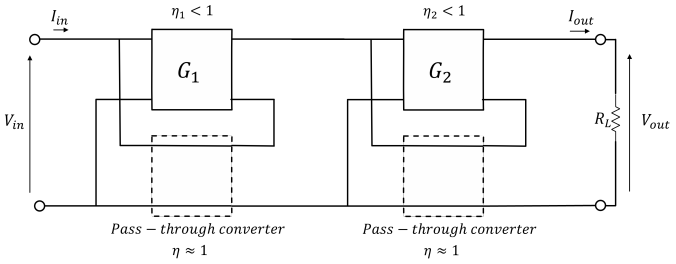


Fig. 3: System-level block diagram of the proposed converter

Since the gain of the PTC is intrinsically unitary, the architecture of Fig. 2b does not allow to fully exploit the benefits of the PPP approach when high step-up gains are required, such as in the targeted PV application. For this reason, the novelty of the proposed architecture consists in a multi-stage configuration, where two IPOS converters are cascaded. This reduces the individual gain requirements for each converter, thereby amplifying the efficiency boost effect in each PPP stage. The final proposed converter architecture is shown in Fig. 3, where two MC provide the voltage gains G_1 and G_2 with efficiency η_1 and η_2, respectively. At the same time, the multi-stage configuration increases the design flexibility, allowing to optimize the converter performance at a desired input voltage, as detailed in Section III.

The total system gain G_{sys} results:

$$G_{\text{sys}} = (G_1 + 1)(G_2 + 1)\,, \tag{2}$$

while the system efficiency η_{sys} follows from (1) and from the multi-stage configuration:

$$\eta_{\text{sys}} = \frac{G_1+1}{1+\frac{G_1}{\eta_1}}\frac{G_2+1}{1+\frac{G_2}{\eta_2}} \tag{3}$$

A well-known drawback of cascaded systems is that the overall efficiency will always be limited by the lowest effi-

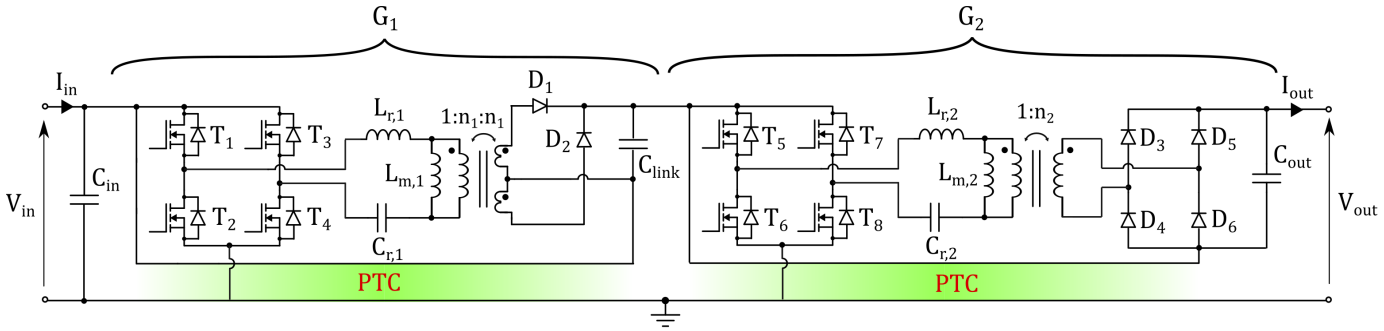


Fig. 4: Schematic of the proposed converter. PTC: Pass-through Converter.

ciency stage. However, in this case, both converters benefit from direct power paths, mitigating efficiency losses.

III. Design Methodology

The selected topology to implement each IPOS stage is the frequency modulated LLC resonant converter, compliant with the topology restrictions mentioned in Section II. The choice is motivated by the inherently high power density, by the possibility to achieve galvanic isolation, by the possible integration of inductive components of the resonant network in the transformer, and by its high efficiency thanks to the soft switching of the semiconductor devices [7]. Fig. 4 shows the complete schematic of the proposed architecture. In this section, an *ad-hoc* procedure is proposed to tune the design of both the stages simultaneously, considering the impact of the load on the regulation capabilities of the LLC converters.

A. Proposed decoupling method

The voltage gain of LLC converters operating outside the resonant frequency exhibits significant load dependency. In the proposed converter, it is important to ensure that the gain can be correctly regulated across the desired input voltage range and load variability.

By analyzing the converter under the First Harmonic Approximation (FHA) [16], the gain profile at different switching frequencies and load scenarios can be evaluated. Conventional design parameters of frequency-modulated LLC resonant converters include:

$$F_x = \frac{f_{\mathrm{sw}}}{f_{\mathrm{r}}} \tag{4}$$

$$m = \frac{L_{\mathrm{r}} + L_{\mathrm{m}}}{L_{\mathrm{r}}} \tag{5}$$

$$Q = \frac{1}{R_{\mathrm{ac}}}\sqrt{\frac{L_{\mathrm{r}}}{C_{\mathrm{r}}}}\,, \tag{6}$$

where Q is the quality factor of the resonator, m is the inductance ratio, and F_x is the normalized switching frequency.

The definitions of F_x, m and Q depend on the design parameters of the resonant tank, specifically on the leakage and magnetizing inductances L_{r} and L_{m}, on the resonant capacitance C_{r}, on the resonance frequency f_{r} and on the equivalent resistance R_{ac} associated to the first-harmonic in the FHA:

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{L_{\mathrm{r}}C_{\mathrm{r}}}} \tag{7}$$

$$R_{\mathrm{ac}} = \frac{8n^2}{\pi}R_{\mathrm{L}}\,, \tag{8}$$

where n is the turn ratio of the transformer and R_{L} is the load resistance of the MC. The magnitude of the MC voltage gain G normalized to the transformer turn ratio takes the following expression:

$$|G| = \frac{F_x^2(m-1)}{\sqrt{Q^2F_x^2(m-1)^2(1-F_x^2)^2 + (F_x^2m-1)^2}}\,, \tag{9}$$

R_{L} is not explicitly defined in the proposed architecture. In order to address this issue, the methodology described in what follows relies on a decoupling approach that enables the design of each LLC resonant converter to be carried out independently of the other. This is achieved under the assumption of decoupled dynamics, specifically, that the output capacitor of each stage is sufficiently large to prevent dynamic interaction with adjacent circuitry. As a result, the subsequent circuitry can be approximated as a constant resistive load, associated to the power being transferred at steady-state operation. This concept is graphically illustrated in Fig. 5: the equivalent load resistance R_{L} is reflected back to the output port of each MC, determined by the gain across the architecture. By taking into account the non-linear PV $P_{\mathrm{PV}}(V_{\mathrm{in}})$ curve, and assuming that the inverter regulates the voltage $V_{\mathrm{out}} = 350\,\mathrm{V}$, the equivalent load resistance can be expressed as:

$$R_{\mathrm{L}} = \frac{V_{\mathrm{out}}^2}{P_{\mathrm{PV}}(V_{\mathrm{in}})}\,. \tag{10}$$

In this work, the P-V characteristic of *3SHBGHA#-680* from 3SUN [17] is considered, shown in Fig. 6 for different irradiance levels. According to (10), R_{L} assumes a voltage- and irradiance-dependent profile. The equivalent resistance $R_{\mathrm{eq_2}}$ for the second stage LLC converter depends on its gain G_2 and becomes:

$$R_{\mathrm{eq_2}} = \frac{V_{\mathrm{out_2}}}{I_{\mathrm{out_2}}} = R_{\mathrm{L}}\frac{G_2}{G_2+1} \;< R_{\mathrm{L}}\,. \tag{11}$$

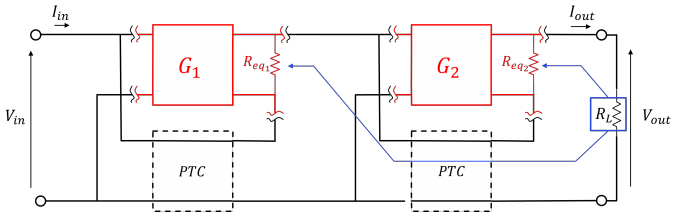


Fig. 5: Location of the equivalent decoupled system resistive loads for each stage.

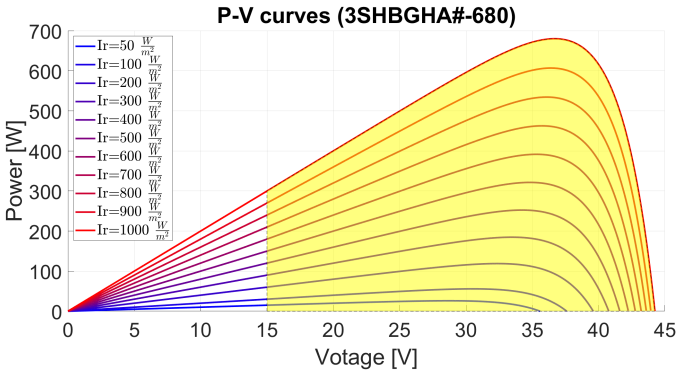


Fig. 6: P-V characteristic and operating area.

Through a similar analysis, R_{eq_1} for the first stage is defined as:

$$R_{\mathrm{eq}_1} = \frac{V_{\mathrm{out}_1}}{I_{\mathrm{out}_1}} = R_{\mathrm{L}} \frac{G_1}{G_1+1} \frac{1}{(G_2+1)^2} \ll R_{\mathrm{L}}\,. \tag{12}$$

B. System-level gain profiling

The proposed converter targets the specifications reported in Tab. I. Given the base framework to decouple each stage from the global system, and given the total gain expression in (2), it is necessary to establish a criterion for the distribution of voltage gains between the two LLC stages on the target input voltage range. When working at resonance and considering negligible parasitic voltage drops across the circuit, LLC converters exhibit a load-independent gain equal to the turn ratio of the transformer. The operation at resonance, thanks to the soft switching of both the primary and secondary side devices, represents the highest efficiency condition of the converter. A higher quality factor Q, corresponding to lower R_{ac}, allows for easier step-down of the gain when working above resonant frequency. On the other hand, lower quality factor values, corresponding to higher R_{ac}, allows for easier step-up of the gain when working below the resonance frequency [7].

This multi-stage architecture allows to select, as a degree of freedom, a desired rated input voltage V_{rated} at which both LLC stages operate at resonance, presumably offering the highest conversion efficiency. A reasonable choice is to select the nominal input voltage of the target solar module, $36.5\,\mathrm{V}$ in this case, to maximize the efficiency in the neighborhood of the most likely working points [9]. When $V_{\mathrm{in}} < V_{\mathrm{rated}}$, at least one stage must provide a gain step-up, whereas a step-down must be realized when $V_{\mathrm{in}} > V_{\mathrm{rated}}$.

TABLE I: Specifications of the proposed converter.

Specification	Value
Input voltage range	$15\,\mathrm{V} - 45\,\mathrm{V}$
Rated voltage	$36.5\,\mathrm{V}$
Output voltage	$350\,\mathrm{V}$
Power range	$0\,\mathrm{W} - 680\,\mathrm{W}$

Based on these characteristics and the expressions derived in (11) and (12), the first stage which experiences the higher quality factor values (lower R'_{L}) is devoted to the step-down behavior of the system when $V_{\mathrm{in}} > V_{\mathrm{rated}}$, while working at resonant frequency (constant gain) otherwise. The second stage is instead designed to step-up the gain when $V_{\mathrm{in}} < V_{\mathrm{rated}}$, and to work at resonance otherwise.

C. Iterative design procedure

An iterative design workflow was developed to optimize the design of the two LLC stages starting from the system-level considerations and constraints described in the previous sub-section. The workflow was developed to derive the main design parameters, such as the turn ratios, leakage and magnetizing inductances, and resonance frequencies, in order to meet the required gain profiles. For both LLC converters, the design procedure imposes constraints on the switching frequency to ensure soft switching of the primary-side transistors and to maintain operation within a range that avoids significant gain deviations due to discrepancies between the FHA and the real converter behavior [18]. The lower bound for the switching frequency is defined by the position of the peak gain under FHA, which depends on the converter quality factor Q. Since this dependency leads to a transcendental expression, the minimum frequency must be computed numerically or extracted from pre-evaluated curves, and is denoted here as $f_{\mathrm{peak}} = p(Q)$. This ensures that the converter always operates above its maximum-gain point, a necessary condition for Zero Voltage Switching (ZVS). The upper bound is chosen as twice the resonant frequency, $2f_{\mathrm{r}}$, a practical limit beyond which the accuracy of the FHA degrades significantly and the gain drops rapidly. The allowable switching frequency range is thus constrained as:

$$f_{\mathrm{sw}} \in \{f_{\mathrm{peak}} = p(Q);\ 2f_{\mathrm{r}}\} \tag{13}$$

Given the large amount of degrees of freedom, f_{r} is set for both stages at $100\,\mathrm{kHz}$, a typical value for LLC converters in this power range employing Si MOSFET technology. C_{r} and L_{r} are then selected to match the resonant frequency and to maximize/minimize the quality factor in each converter accordingly, limited by the market capacitance values considering RMS current limitations, and leakage inductance limitations which appear in the design of the transformer.

For the remaining degrees of freedom, the two gain profiles for G_1 and G_2 are proposed, fixing by consequence the turn

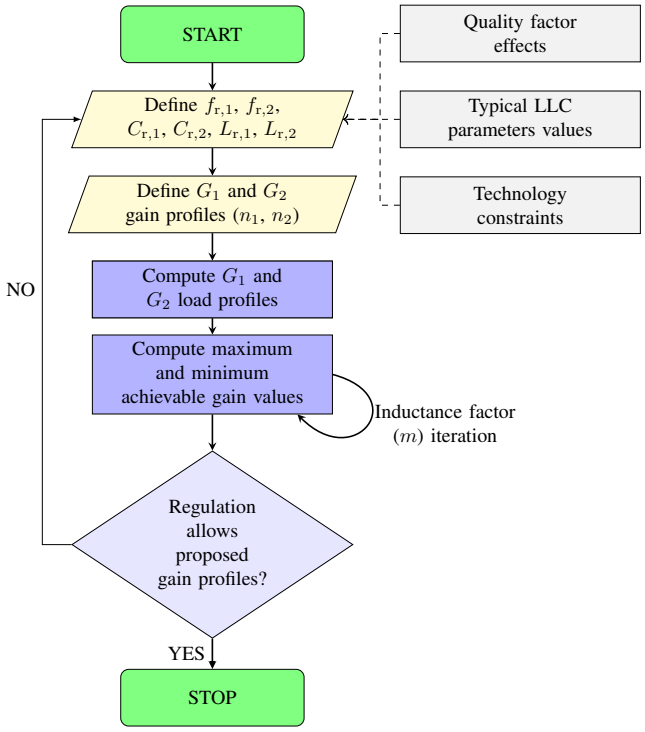


Fig. 7: Iterative design workflow.

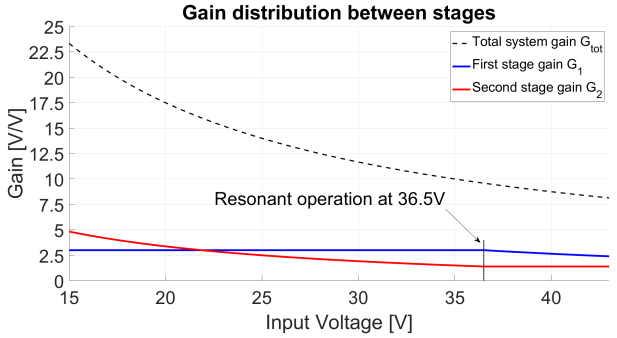
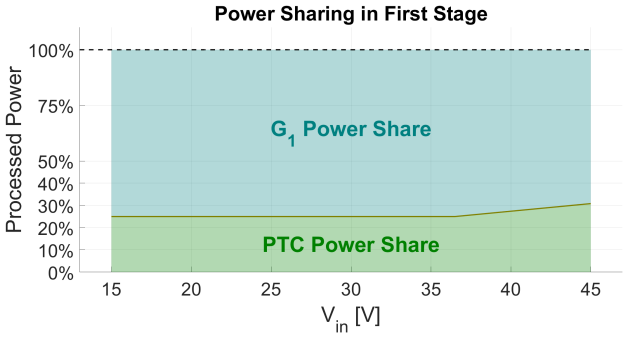
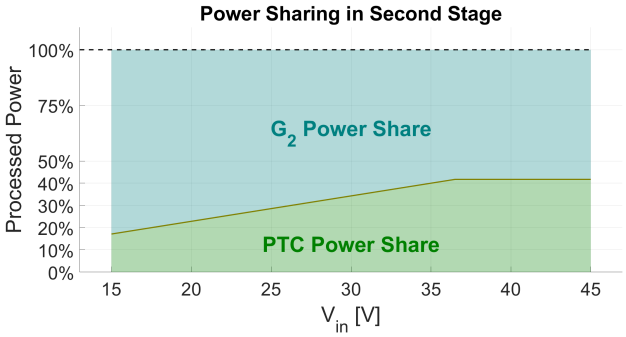


Fig. 8: Gain profiles for both stages and overall system.



(a)



(b)

Fig. 9: Power fractions across the architecture depending on operating voltage (a) First stage power flow. (b) Second stage power flow.

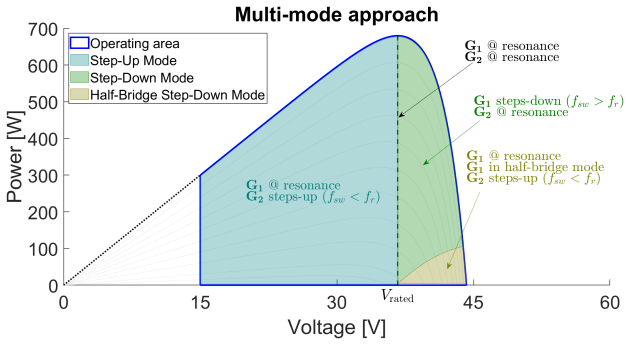
ratio for each transformer. The load profiles are then derived from (11) and (12). The considered load profiles represent the most critical scenarios in terms of voltage regulation for each stage at each voltage value for different inductance ratios, i.e. the heaviest load in the step-up region ($V_{\text{in}} < V_{\text{rated}}$) and the lightest load when in the step-down region ($V_{\text{in}} > V_{\text{rated}}$). The gain limitation is then compared to the initially proposed gain profiles, having to iterate the design if regulation is not possible. Due to the discrepancies of the FHA model with the real gain regulation of the system, a margin is taken to comply with possible gain limit errors.

A flowchart of the iterative procedure, implemented in a *MATLAB* [19] script, is illustrated in Fig. 7.

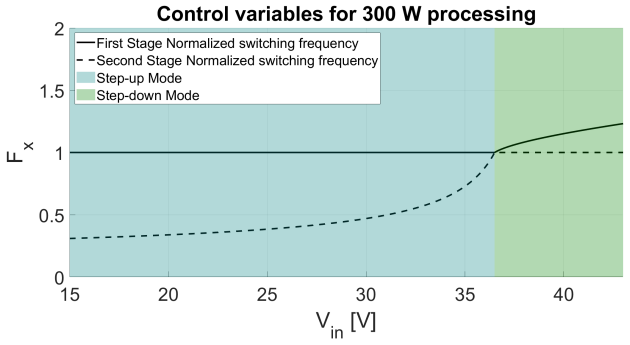
The resulting gain profiles for each stage as well as the required global gain profile are shown in Fig. 8 versus the input voltage V_{in}. These gains were selected to impose the resonant operation of both stages at rated input voltage, $36.5\,\text{V}$. The resulting optimal gain profiles represent a trade-off between the need of simultaneously maximizing the direct power flows in both stages at the rated input voltage, and the desirable minimization of the current stresses at the interface between the first and second stage. Further limitations include the feasibility of the turn ratios of the transformers.

According to the imposed gain profiles, an analysis on power flow through the architecture can be carried out. Fig. 9 shows the fraction of power delivered through the PTC and MC for each stage, versus the target $15\,\text{V} - 45\,\text{V}$ input voltage range. As it can be observed, the direct power flow in the second stage progressively decreases by working at lower input voltages. At the rated voltage, around $25\,\%$ and $40\,\%$ of the total input power are transferred through the PTC of the first and second stage, respectively.

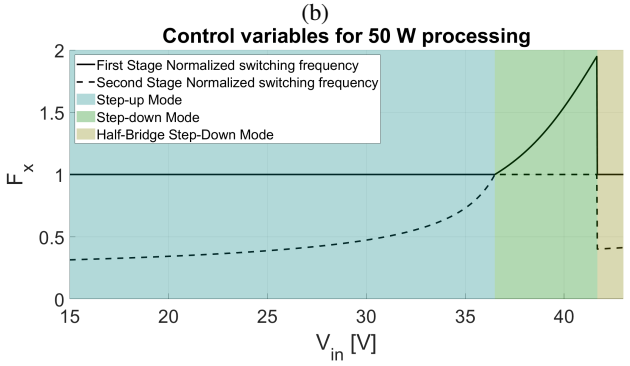
Fig. 10a illustrates the multi-mode behavior of the converter on the targeted operating area, illustrating the control mode for the two LLC converters in each section of the power-voltage plane. In step-up mode, the first stage lowers its switching frequency to increase the gain, while the second stage remains at resonance. In step-down mode, the second stage rises its switching frequency to decrease the gain, while the first stage remains at resonance Extreme light load scenarios, i.e. in case of particularly low irradiance, challenge the step-down gain regulation capabilities of the first stage for $V_{\text{in}} > 36.5\,\text{V}$. In these conditions, the first stage is designed to morph its full-



(a)



(b)



(c)

Fig. 10: Multi-mode approach of the architecture (a) Operating area and modes. (b) Controlled variables for 300 W extraction case. (c) Controlled variables for 50 W extraction case

bridge input inverter into a half-bridge inverter, effectively halving the gain of the first stage. This will force the gain to lower values, having to utilize the second stage in step-up mode, which does not struggle to regulate for extreme light load scenarios, while the first stage remains at resonance.

Figs. 10b and 10c show the required normalized switching frequencies to modulate the gain of each stage over the complete input voltage range and at two power conditions, 300 W and 50 W. By design constraint, the two switching frequencies are bounded as reported in (13).

IV. Simulation Results

With reference to Fig. 4, the two LLC stages share the same full-bridge configuration at the input sides, while they differ in the implementation of the rectifiers. In the first stage, characterized by higher current stresses, the transformer is implemented with a center tap to reduce the number of diodes of the rectifier. In the second stage, instead, characterized by lower current stresses, a full-bridge diode rectifier is preferred to limit the peak voltage stresses across the diodes below V_{out}.

Tab. II lists the main parameters adopted for the simulation of the system, derived from the design methodology and adjusted to the characteristics of off-the-shelf components.

The simulations are performed in *LTSpice* [20] with the inclusion of SPICE models for the MOSFETs and diodes, for a representative estimation of the losses. Additionally, transformer winding losses were modeled through the implementation of Dowell's model with Wojda's modification for Litz wire modeling [21]. The core losses P_{core} are also incorporated into the simulation through the application of the incremental expression of Steinmetz equation:

$$P_{\text{core}} = k_f V_e p_{v_{\text{sin}}} \left(\frac{f}{f_b}\right)^{\alpha} \left(\frac{B}{B_m}\right)^{\beta} \left[\frac{W}{set}\right] \qquad (14)$$

where $p_{v_{\text{sin}}}$ is the core loss density per volume, $\frac{f}{f_b}$ and $\frac{B}{B_m}$ are the normalized frequency and peak magnetic flux density, V_e is the volume of the core set, while k_f, α and β are the Steinmetz coefficients of the material, as reported in the manufacturer datasheet.

Capacitor losses are modeled through the insertion of the Equivalent Series Resistance (ESR) parameter given by the manufacturers, considering the worst-case scenario in terms terms of operating frequency.

To evaluate the efficiency of the proposed quadratic IPOS converter across a wide operating range, its performance is analyzed at multiple operating points, coherent with the specifications of Tab. I. Fig. 11a shows the power flows of the circuit for the rated operating point of the system, $V_{\text{in}} = 36.5\,\text{V}$ and $P_{\text{out}} = 680\,\text{W}$, while Fig. 11b shows the power budget in this condition. Approximately 25 % and 40 % of the total power flows through the PTCs, respectively, allowing for a significant reduction of the current stresses on

TABLE II: Components and parameters used in the simulations.

Component / parameter	Stage	Value	Part number
MOSFETs $T_1 - T_4$	1	N/A	STL120N10F8
Resonant inductor $L_{\text{r},1}$	1	11.3 µH	N/A (custom)
Magnetizing inductor $L_{\text{m},1}$	1	120 µH	N/A (custom)
Turn ratio $1 : n_1 : n_1$	1	5:14:14	N/A
Resonant capacitor $C_{\text{r},1}$	1	224 nF	4 x R76PN25605000J
Resonance frequency $f_{\text{r},1}$	1	100 kHz	N/A
Diodes $D_1 - D_2$	1	N/A	STTH30R04-Y
DC-link capacitor C_{LINK}	1-2	33 µF	R75IW533050H4J
MOSFETs $T_5 - T_8$	2	N/A	STB80N20M5
Resonant inductor $L_{\text{r},2}$	2	9.38 µH	N/A (custom)
Magnetizing inductor $L_{\text{m},2}$	2	60 µH	N/A (custom)
Turn ratio $1 : n_2$	2	14:20	N/A
Resonant capacitor $C_{\text{r},2}$	2	270 nF	R76MN32705050J
Resonance frequency $f_{\text{r},2}$	2	100 kHz	N/A
Diodes $D_3 - D_6$	2	N/A	STTH30R04-Y
Output capacitor C_{out}	2	4.7 µF	B32774H8475K000

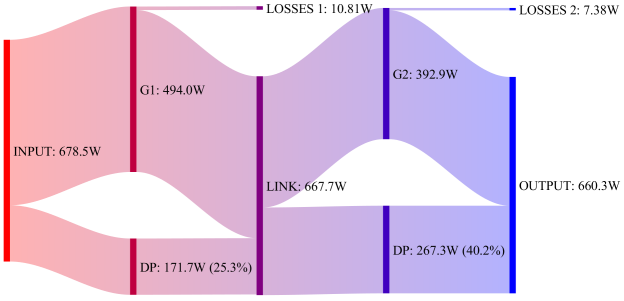
TABLE III: Comparison of Step-up Techniques

Reference	[22]	[23]	[24]	[25]	[9]	[13]	Proposed
Step-up technique	Voltage Multipliers	LLC	Topology-morphed LLC	Partial Power Flyback	Partial power multi-mode asymmetric IPOS	Partial power multi-stage IPOS	Partial power multi-mode multi-stage IPOS
Isolation	No	Yes	Yes	No	No	No	No
Number of switches	4	4	6	1	9	2	8
Number of diodes	7	2	7	1	2	3	6
Magnetic components	6 (ind.)	1 (transf.), 2 (ind.)	1 (transf.)	1 (transf.)	1 (transf.), 1 (ind.)	1 (transf.), 2 (ind.)	2 (transf.)
Capacitors	9	4	8	2	6	4	4
Rated power	1 kW	500 W	300 W	275 W	750 W	200 W	680 W
Input voltage range	25–40 V	20–60 V	25–50 V	31 V	15–45 V	20 V	15–45 V
Total DC gain range	10–16	5.8–17.5	10–20	5	7.8–23.3	5.5	7.8–23.3
Fraction of directly transferred power at rated voltage	–	–	–	17.2 %	–	– (I), 22.2 % (II)	25.3 % (I), 40.2 % (II)
Efficiency range	97.2–97.9 % (1 kW)	94.5–95.6 % (300 W)	94.5–95.5 % (300 W)	97.6 % (275 W, sim.)	94.6–97.1 % (300 W, sim.)	94 % (100 W)	92.6–97.3 % (300 W, sim.)

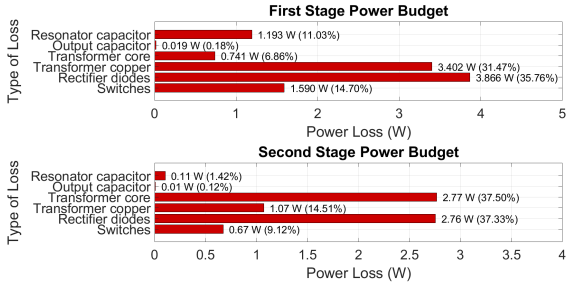
all the components compared to a conventional full-power multi-stage converter.

Fig. 12a shows the behavior of the efficiency as a function of V_{in} at three different power levels, with the voltage range compliant to the power availability, according to Fig. 10. The efficiency has a monotonic increasing tendency, as lower system gain values present more power flow through the efficient PTCs. Above the nominal input voltage 36.5 V, the efficiency tends to acquire a flatter profile, as further increasing the direct power flows is compensated by the lower performance of the first LLC stage, operating outside resonance.

Fig. 12b shows the behavior of the efficiency as a function of P_{out} at three different voltage levels, namely 15 V, 36.5 V and 43 V. The efficiency for nominal input voltage, where both the LLC stages always operate at resonance, exhibits a flat profile above 97 % between 200 W and 680 W. A peak efficiency of 97.54 % is achieved between 60 % and 70 % of the rated output power, with a 97.2 % California Energy

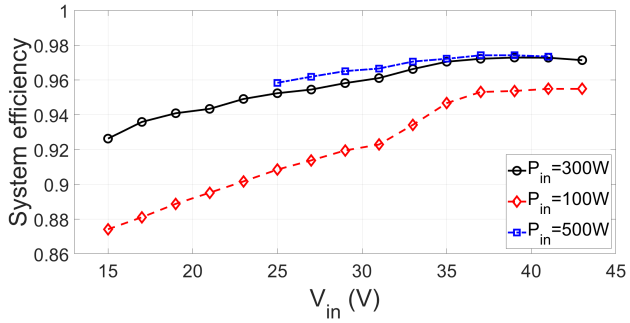


(a)

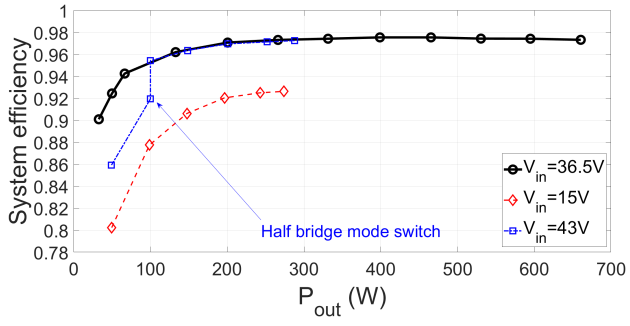


(b)

Fig. 11: Sankey diagram of the power flows of the system and power budget for $V_{\text{in}} = 36.5\,\text{V}$ and $P_{\text{in}} = 680\,\text{W}$. (a) Sankey diagram from simulation power output. (b) Power budget chart plot from simulation power losses output.



(a)



(b)

Fig. 12: Main efficiency simulation results for different voltage and power sweeps. (a) Efficiency as a function of the input voltage, at three representative power levels (100, 300, 500 W). (b) Efficiency as a function of the output power, at three representative voltage levels (15 V, 36.5 V, 43 V).

Comission (CEC) weighted efficiency, and a 96.8 % EURO weighted efficiency, conventional figures of merit for realistic outdoor scenarios where solar irradiance may vary throughout the day. In the extreme lowest voltage scenario, $V_{\mathrm{in}} = 15\,\mathrm{V}$, the converter efficiency drops due to the high step-up gain required by the second stage LLC and the lower fraction of power through the PTC. For the high input voltage scenario, $V_{\mathrm{in}} = 43\,\mathrm{V}$, the first-stage LLC morphs its full-bridge inverter into a half-bridge inverter at light loads, allowing to achieve the required voltage gain at the expense of an efficiency drop.

Tab. III compares the main features and results of the proposed converter with other state of the art solutions. The proposed multi-mode approach allows to achieve one of the widest input voltage operation with a limited efficiency drop. At the same time, the design flexibility offered by the multi-stage approach allows to achieve a high $97.3\,\%$ peak efficiency at the rated input voltage. The proposed solution and design methodology can easily be exported to different design specifications or applications requiring a wide gain range and a wide load range.

V. Conclusions

This paper presents the analysis, design, and simulation of a novel DC-DC power converter for wide-range photovoltaic applications, utilizing an innovative multi-stage, multi-mode architecture in Partial Power Processing configuration. The proposed converter is designed to work on the wide $15\,\mathrm{V} - 45\,\mathrm{V}$ input voltage range and $680\,\mathrm{W}$ rated power. An ad hoc iterative design procedure allows to identify an optimal set of design parameters to maximize the fractions of power directly transferred, while ensuring the correct regulation on the complete voltage range. Simulation results show a EURO weighted efficiency of 96.8 % and a CEC weighted efficiency of 97.2 %. These results indicate a high level of performance in a vast range of operating conditions. Future work will focus on different branches from this work such as the inclusion of DC-AC conversion with isolation, mission profile-oriented design, resonant tank optimization, cost analysis, experimental validation, and exploring alternative applications. In conclusion, the proposed power converter offers a high efficiency solution for photovoltaic systems designed to operate on a wide voltage and power range.

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