Closed-Loop Control Implementation of a 50 W Grid Adapter with Capacitive Isolation

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***Abstract*—This article proposes the design, implementation, and simulation of a closed-loop voltage-mode controller for a grid adapter featuring an innovative, capacitive-isolated, Multi-Period Damped Resonant (MPDR) DC-DC converter. After presenting a mathematical model of the converter in open loop, different control strategies, i.e. frequency modulation (FM), Pulse-Width Modulation (PWM), Bang-bang control, and Dyadic Digital Pulse Modulation (DDPM), are introduced and analyzed. The four controllers are designed and compared in terms of dynamic performances by Simulink simulations. Preliminary experimental tests validate the converter operation on the four control strategies.**

***Index Terms*—DC-DC Conversion, Control Design, Capacitive Power Transfer, Power Converter Modelling, Frequency Modulation, Pulse Width Modulation, Bang-Bang Control, Dyadic Digital Pulse Modulation.**

I. Introduction

Grid adapters for consumer applications such as laptop and mobile chargers need to combine conflicting specifications such as high power density, high efficiency, galvanic isolation, high step-down ratio and low cost. Aiming to meet these requirements, several power converters have been proposed in the literature over the last years, including solutions derived from the conventional buck [1], [2] or buck-boost [3] topologies. These solutions feature a simple design and PWM control but are limited in efficiency and power density due to the hard-switching operation and to the presence of multiple magnetic components. In addition, they do not include the desirable galvanic isolation.

Some solutions propose isolated flyback-derived topologies [4], [5], which, however, require auxiliary passive networks to overcome the intrinsic limitations of flyback converters, namely the high voltage stresses across the main switch, and the hard switching.

Higher efficiency and power density solutions combine Wide Bandgap (WBG) devices with high-frequency transformers in resonant isolated topologies [6]–[8]. The use of GaN High Electron Mobility Transistors (HEMT) offers superior switching performances, but the transformer usually represents the efficiency bottleneck of these solutions.

A competitive alternative to Inductive Power Transfer (IPT) solutions to provide galvanic isolation while overcoming the size and loss limitations of transformers is the Capacitive Power Transfer (CPT), based on high-frequency electric fields induced between two metal plates [9]. CPT-based solutions are gaining attention in various low-power and high-power applications for the lighter weight, reduced Electromagnetic Interference (EMI) and tolerance to misalignments [9]–[11], but usually need complex compensation networks to reduce the sensitivity of the resonance frequency to components tolerances [12].

In our previous work [13], we proposed a step-down grid adapter that uses two interface capacitors to provide galvanic isolation and a single compensation inductor to minimize the component count and maximize the power density. Differently from the Series Resonant Converter (SRC) proposed in [11], our converter exploits the Multi-Period Damped Resonant (MPDR) mode, which enables high power density by reducing the size of passive components while keeping switching losses low [13].

However, the design and implementation of a control strategy aiming to regulate the output voltage has not been proposed so far. This work addresses this gap by exploring several closed-loop control techniques for MPDR converters and comparing them based on different criteria, such as conversion efficiency, the possibility of achieving soft-switching of the converter transistors, and induced voltage ripple. The four controllers, based on Frequency Modulation (FM), Pulse Width Modulation (PWM), Bang-bang (BB) control and Dyadic Digital Pulse Modulation (DDPM), are individually designed to regulate the output voltage under varying load conditions, ensuring stability and maximizing system performance.

The article is structured as follows: Section II describes the proposed converter topology and the mathematical model used to analyze the static gain and dynamics of the system; Section III introduces the four control strategies for the converter and their design tuning; Section IV shows simulation results for the different control strategies and offers a comparison between them; Section V presents preliminary experimental results of this converter, while conclusions and future work are presented in Section VI.

II. Proposed Converter Topology and Modeling

The topology of the proposed grid adapter consists of two cascaded stages, an unregulated diode-bridge rectifier followed

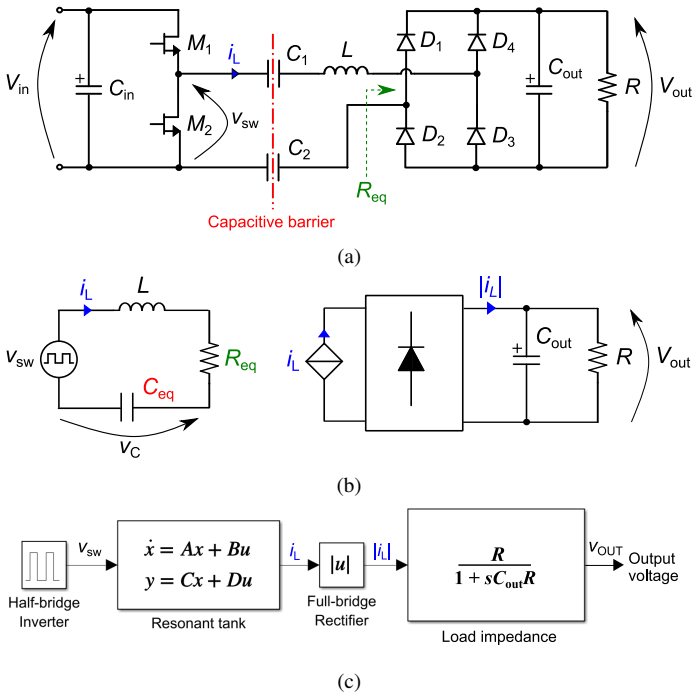

Figure 1: Schematic and corresponding modeling of the proposed converter. (a) Schematic of the DC-DC stage; (b) Equivalent circuits representation; (c) Corresponding block-diagram representation used for the converter control.

by a step-down regulated DC-DC stage. This work only focuses on the implementation of a closed-loop control for the DC-DC stage, whose schematic is shown in Fig. 1a. The topology was already presented in our previous work [13], and consists of a half-bridge inverter, a capacitive interface made of two discrete capacitors that provide the galvanic isolation, a secondary-side single inductor compensation network, a full-bridge rectifier, and an output DC filter capacitor. This low-components-count configuration was chosen to optimize cost, complexity, and efficiency for the target application.

As described in [13], the core innovative idea of the converter, compared to other conventional resonant converters [6], [11], is to operate the half-bridge inverter at a switching frequency much lower than the resonance frequency of the $L - C_1 - C_2$ tank: in this way, it is possible to design the passive components of the resonant tank to operate at a higher frequency, without a corresponding increase of the switching losses of M_1 and M_2. The proposed operation is thus called MPDR and is characterized by the presence of multiple resonant periods inside a switching cycle. The complete derivation of the static characteristic and voltage gain as functions of the switching frequency and load resistance is provided in [13] and is out of the scope of this work. For modeling and control design purposes, it is helpful to introduce a set of two equivalent circuits, shown in Fig. 1b. Assuming that the input capacitor C_{in} is large enough to maintain a constant voltage V_{in}, the switching node voltage can be modeled as a square wave voltage generator stepping between 0 V and V_{in} with frequency

Table I. Main design specifications (Spec.) and parameters (Param.) of the proposed converter.

Spec. / Param.	Value
Input voltage V_{in}	330 V
Output voltage V_{out}	20 V
Rated power P_{out}	50W
Resonant inductor L	37 µH
Capacitors C_1, C_2	15 nF
Output capacitor C_{out}	1 mF
Resonance frequency f_{res}	300 kHz
Switching frequency f_{sw}	115–145 kHz

f_{sw} and duty cycle d, modified by the control. The rectifier input is represented by an equivalent resistor R_{eq}, which mainly depends on the load resistance, the rectified output voltage V_{out} and the forward conduction voltage of the diodes V_γ, i.e., $R_{eq} = R_{eq}(R, V_{out}, V_\gamma)$. Its exact expression is provided in [13]. The two isolating capacitors $C_1 = C_2 = C$ can be embedded in a single equivalent capacitance $C_{eq} = \frac{C}{2}$.

The equivalent circuits can be further simplified into the block diagram representation of Fig. 1c. The time-domain operation of the resonant circuit in Fig. 1b can be described in terms of state-space equations:

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_C \end{bmatrix} = \begin{bmatrix} -\frac{R_{eq}}{L} & -\frac{1}{L} \\ \frac{1}{C_{eq}} & 0 \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{v_{sw}}{L} \\ 0 \end{bmatrix}, \tag{1}$$

where i_L and v_C are the state variables x_1 and x_2, the voltage of the switching node v_{sw} is the input u, and i_L is selected as the output y.

The rectifier stage of the converter acts as an absolute value function that introduces a non-linearity. The operation of the rectifier and output DC filter can be described by (2). In the block diagram of Fig. 1c, this second part of the circuit is modeled as an absolute value function followed by a first-order low-pass filter representing the load impedance.

$$|i_L| = C_{out}\frac{dv_{out}}{dt} + \frac{v_{out}}{R}. \tag{2}$$

Tab. I lists the main design specifications and parameters of the converter. The DC-DC stage is designed to step-down to 20 V the rectified grid voltage 330 V, with a target efficiency higher than 85 % at the rated load power 50 W. The values of the resonant inductance and capacitances are designed to ensure the Zero-Voltage Switching (ZVS) of the transistors M_1 and M_2, and based on both efficiency and gain regulation criteria [13]. As explained in [13], the converter can work in two different operating modes according to the damping strength. When the resonant oscillations are completely extinguished before the end of the half-switching period, the converter is said to work in the Completely Damped Oscillations (CDO) mode, characterized by a linear power-frequency behaviour. Otherwise, the converter operates in the Partially Damped Oscillations (PDO) mode, characterized a strongly non-linear and non-monotonic power-frequency dependence. Since the PDO mode allows to regulate the output voltage in a reduced

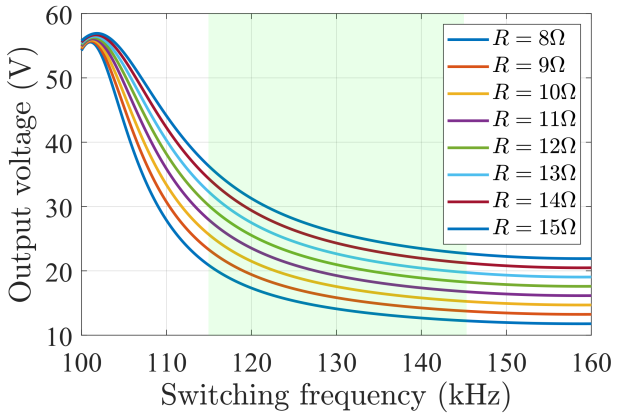

Figure 2: Behaviour of the output voltage as a function of the switching frequency, for various load conditions.

frequency range and to achieve the ZVS of the half-bridge FETs, the converter and control parameters were designed to work in this mode.

III. Control Strategies Implementation

The controllers proposed in this work refer to modulation strategies for the GANFETs M_1 and M_2. This section introduces the four approaches, by presenting the input-output static characteristic under different load scenarios, deriving empirically the control-to-output transfer functions and detailing a design approach to tune the controller parameters. Since the objective of this work is to compare different control strategies, common design constraints must be defined to provide a fair comparison. In this case, all the controllers are designed to achieve, for the worst-case load scenario, a control bandwidth of 1 kHz, to exploit the first-order dynamic behaviour of the converter, as it will be detailed in the following sections.

A. Frequency Modulation (FM) control

This approach consists in varying the switching frequency f_{sw} of the gate signals while keeping 50 % duty cycle and 180° phase shift to avoid the cross-conduction of the transistors. As described in [13], this control sequence results in a symmetric operation in the two half-periods. As mentioned in Section II, the frequency range is selected to ensure the PDO operation. In these condition, the static characteristic $V_{out}(f_{sw})$ assumes the non-linear behaviour shown in Fig. 2, whose analytical model can be found in [13]. The selected frequency range $f_{sw} \in [f_{min}; f_{max}] = [115; 145]$kHz, highlighted in green, is located between 1/3 and 1/2 of the resonance frequency ($\approx$ 302 kHz), ensuring ZVS for all the frequencies and avoiding high power conditions. As it is possible to observe, the FM does not allow to achieve the target $V_{out} = 20$ V for any load condition, but only for $R < 14\,\Omega$, meaning that this controller cannot ensure the correct regulation at light loads.

By design choice, the selected control function exploits a normalized switching frequency $u \in [-1; 1]$ such that:

$$f_{sw}(t) = \frac{f_{max} + f_{min}}{2} - u(t)\ \frac{f_{max} - f_{min}}{2}\,. \tag{3}$$

Table II. Empirical parameters of the simulated transfer function Bode plots, for the FM control.

Load resistance (Ω)	DC gain (V)	Pole frequency (Hz)	Zero frequency (kHz)
8 Ω	16.0	19	3.2
13 Ω	2.51	12	3.2

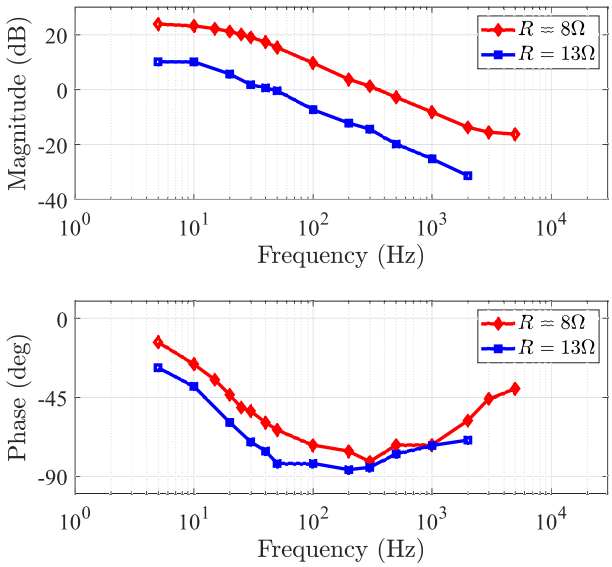

Figure 3: Simulated Bode plots of the control-to-output transfer function $V_{out}(u)$ for the FM controller at two load conditions, 8 Ω and 13 Ω.

A Proportional-Integral (PI) regulator was designed for the closed-loop output voltage control. The derivation of the control-to-output transfer function $\frac{\hat{v}_{out}}{\hat{u}}(s)$ was performed through simulations in Matlab-Simulink, by measuring the dynamic response of V_{out} to small-signal oscillations of the control action u around the rated 20 V output. Fig. 3 reports the simulated Bode plots of the control-to-output transfer function in two extreme load conditions, the rated load resistance 8 Ω (corresponding to the rated 50 W power) and the highest resistance 13 Ω still allowing the output voltage regulation to 20 V. As it can be seen, the transfer functions exhibit a first-order low-pass filter behaviour characterized by load-dependent DC gains and pole frequencies. An additional first-order zero is introduced by the output capacitor Equivalent Series Resistance (ESR) at approximately 3.2 kHz. The empirical parameters of the two transfer functions are reported in Tab. II: since the 8 Ω case represents the worst-case condition from stability perspectives, it is selected as the reference condition for the PI coefficients design.

Considering the PI regulators transfer function expressed in (4), the K_p and K_i coefficients are designed so as to achieve a zero-pole compensation and, at the same time, to set the crossover frequency of the loop gain at 1 kHz. The selected coefficients are reported in Tab. V.

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{4}$$

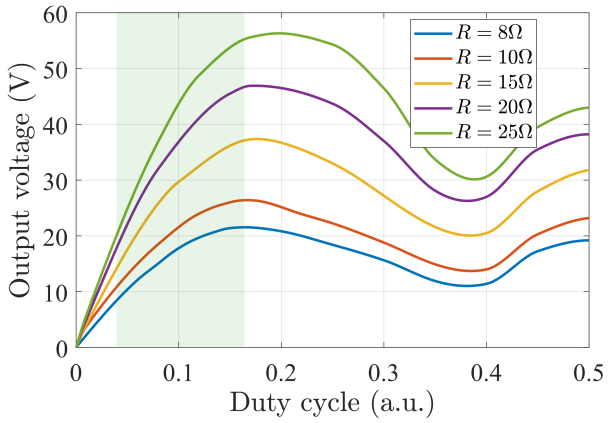

Figure 4: Behaviour of the output voltage as a function of the duty cycle, for various load conditions.

B. Pulse Width Modulation (PWM) control

In the FM control, the 50 % duty cycle ensures symmetric operation and uniform electrical stresses on the two transistors. One of the main limitations, as mentioned, is the regulation at light loads, which can be overcome by reducing or increasing the duty cycle away from 50 %. The result is that the current and voltage waveforms lose the symmetry in the two fractions of the switching period, and the transistors M_1 and M_2 experience unbalanced current stresses. Since the analytical model proposed in [13] does not apply to asymmetric half-periods, simulations were carried out to derive the static characteristic $V_{\text{out}}(d)$, where d is the duty cycle. In the PWM control, the switching frequency was set to 115 kHz. From the simulation results, shown in Fig. 4 for different load conditions, it is possible to observe that there always exists $d \in [0\,\%; 17\,\%] \cup [83\,\%; 100\,\%]$ such that the target 20 V can be achieved. It is possible to prove that the static characteristics are perfectly symmetric around the 50 % axis, so the 50 % – 100 % range is not reported.

As in (3), the PWM controller exploits a normalized control action $u \in [-1; +1]$ such that the duty cycle d is always constrained in a limited range, namely $d \in [d_{\min}, d_{\max}] = [0.04; 0.17]$:

$$d(t) = \frac{d_{\max} + d_{\min}}{2} + u(t)\ \frac{d_{\max} - d_{\min}}{2}. \tag{5}$$

With the same approach exploited for the FM, the Bode plots of the control-to-output transfer functions $\frac{\hat{v}_{\text{out}}}{\hat{u}}(s)$ for two extreme load conditions were derived and are shown in Fig. 5. As in the FM case, the transfer functions exhibit load-dependent DC gain and first-order pole frequency, and a fixed first-order zero related to the output capacitor ESR. The empirical parameters of the transfer functions are reported in Tab. III. The highest DC gain condition, corresponding to the 25 Ω, was selected as worst-case for the design of the coefficients of a PI regulator.

Table III. Empirical parameters of the simulated transfer function Bode plots, for the PWM control.

Load resistance (Ω)	DC gain (V)	Pole frequency (Hz)	Zero frequency (kHz)
8 Ω	3.27	19	3.2
25 Ω	19.9	6.4	3.2

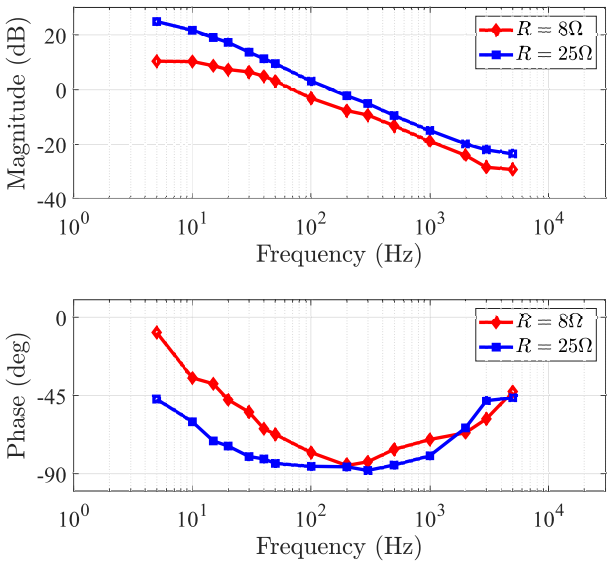

Figure 5: Simulated Bode plots of the control-to-output transfer function $V_{\text{out}}(u)$ for the PWM controller at two load conditions, 8 Ω and 25 Ω.

C. Bang-bang (BB) control

The bang-bang controller, also known as ON-OFF controller, operates by switching between two states depending on the instantaneous output voltage value. The converter can operate in the ON state, where the transistors switch at $f_{\text{sw}} = 115$ kHz and $d = 50\%$, and OFF state, where no switching occurs and there is no instantaneous power transfer between source and load. The alternate switching between ON and OFF states keeps the output voltage close to the reference, with an oscillation amplitude that depends on the threshold voltages defined at the control design level. The advantage of this controller is that it works for any load value, but the hysteresis operation causes an increased output voltage ripple. This control strategy has been widely studied in different converters, such as in [14]. Differently from the previous controllers, no control variable can be defined for the bang-bang controller, which intrinsically works in a closed loop.

D. Dyadic Digital Pulse Modulation (DDPM) control

The DDPM was firstly introduced in [15] as a way to relax the filtering requirements to extract the baseband component of Digital PWM signals, and was later applied to different application fields, such as the limitation of the Limit-Cycle Oscillations (LCO) in digitally-controlled power converters [16]. When used as a modulation strategy, the DDPM consists in skipping selected pulses of the gate signals, while distributing the remaining ones in a uniform fashion. With

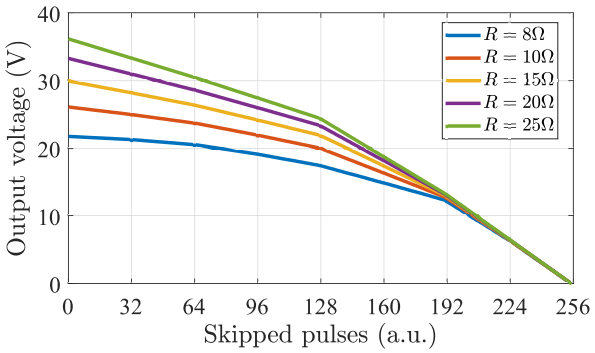

Figure 6: Behaviour of the output voltage as a function of the number of skipped pulses n, for various load conditions.

this approach, compared to the bang-bang controller, the ripple superimposed to the output voltage is minimized. The switching frequency and duty cycle are kept fixed, namely at 115 kHz and 50 %, respectively. The number of skipped pulses n, effectively representing the control variable of this modulation, is bounded between 0 and $2^N - 1$, where N is the number of bits on which the bit-stream can be represented. It is intuitive that, the larger n, the lower the output voltage. In the extreme case $n = 0$, the converter works with fixed duty cycle and frequency. Fig. 6 shows the static characteristic $V_{\text{out}}(n)$ for different load resistances, assuming $N = 8$ and, consequently, $n \in [0, 255]$. As for the PWM case, it is always possible to find n such that the target 20 V can be achieved.

A normalized control action $u \in [-1; 1]$ is used as the output of a PI controller and is related to n by:

$$n(t) = \text{round}\left[\frac{1 - u(t)}{2}\left(2^N - 1\right)\right]. \tag{6}$$

Adopting the same approach exploited for the FM and PWM, the Bode plots of the control-to-output transfer functions $\frac{\hat{v}_{\text{out}}}{\hat{u}}(s)$ were derived in simulations for 8 Ω and 25 Ω load conditions. The Bode plots of the transfer function, shown in Fig. 7, exhibit a load-dependent DC gain and low-frequency pole, as in the FM and PWM cases. Compared to the previous cases, since the pulse sequence corresponding to a certain n lasts for $2^N T_{\text{sw}}$, the dynamics of the system can only be characterized below $\frac{f_{\text{sw}}}{2^N} \approx 3.6$ kHz, using $N = 5$. As a result, the effect of the zero introduced by the output capacitor ESR cannot be visualized from the presented transfer functions.

The empirical parameters associated to the two transfer functions are reported in Tab. IV of the transfer functions are reported in Tab. III. The highest DC gain condition, corresponding to the 25 Ω, was selected as worst-case for the design of the coefficients of a PI regulator, which outputs the number of skipped pulses $n \in [0, 2^N - 1]$. An optimized software implementation of the DDPM algorithm can be found in [17].

IV. Simulation Results

In this section, the effectiveness and stability of the closed-loop controllers are validated through Matlab-Simulink sim-

Table IV. Empirical parameters of the simulated transfer function Bode plots, for the DDPM control.

Load resistance (Ω)	DC gain (V)	Pole frequency (Hz)
8 Ω	7.1	19
25 Ω	20.0	6.4

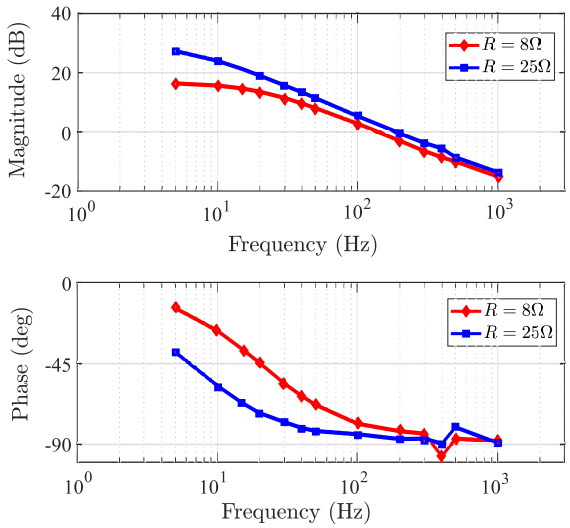

Figure 7: Simulated Bode plots of the control-to-output transfer function $V_{\text{out}}(u)$ for the DDPM controller at two load conditions, 8 Ω and 25 Ω.

ulations. The controllers were developed using the design parameters reported in Tab. V, derived from the design constraints introduced in Section II. Fig. 8 shows the evolution of the output voltage in the four controller cases, assuming that the reference voltage V_{ref} steps to 20 V at time $t = 0$ s and the load resistance R steps from the rated 8 Ω to 13 Ω (for the FM controller) or to 25 Ω (for the other three controllers) at $t = 60$ ms. Fig. 8a shows the dynamic response for the FM controller, showing that the switching frequency saturates to the lower bound, 115 kHz, to ensure the maximum power transfer until the target 20 V are reached. After the load step, f_{sw} is adjusted to around 130 kHz. Fig. 8b shows that, for the PWM controller, the duty cycle is initially saturated to 17 % until $V_{\text{out}} = 20$ V, then is adjusted to around 12.5 % and 4 % at steady state operation with 8 Ω and 25 Ω, respectively. Differently from the FM and PWM controllers, the BB controller always maintains V_{out} within a hysteresis band, thus no overshoot is observed when the load step occurs. The behaviour of the BB controller is shown in Fig. 8c. Finally, Fig. 8d shows the evolution of the output voltage and of the control variable, the number of skipped pulses n, in the DDPM case. During the startup, n saturates to 0, ensuring the maximum power transfer until the target 20 V are reached, and then stabilizes around 13 and 21 at steady state for 8 Ω and 25 Ω loads, respectively. A larger ripple at steady state can be observed compared to FM and PWM, due to the presence of skipped switching pulses. Tab. V compares the

Table V. Comparison among the implemented control strategies.

Control strategy	Control variable	Frequency / Duty cycle	Controller type	Designed bandwidth	V_{out} peak-to-peak ripple	Controller parameters	Load range	2% Settling time	Overshoot to load step
FM	Switching frequency f_{sw}	Variable / Fixed	PI	1 kHz	1.1%	$k_p = 3.3$, $k_i = 390$	Limited (8 Ω–13 Ω)	30 ms	0.3 V
PWM	Duty cycle d	Fixed / Variable	PI	1 kHz	1.3%	$k_p = 6$, $k_i = 320$	Full	18 ms	0.18 V
BB	ON-OFF switching	Fixed / Fixed	Hysteresis	N/A	1.6%	$V_h = 20.1$ V, $V_l = 19.9$ V	Full	23 ms	Null
DDPM	Skipped pulses n	Fixed / Fixed	PI	1 kHz	1.8%	$k_p = 1.5$, $k_i = 200$	Full	23 ms	0.27 V

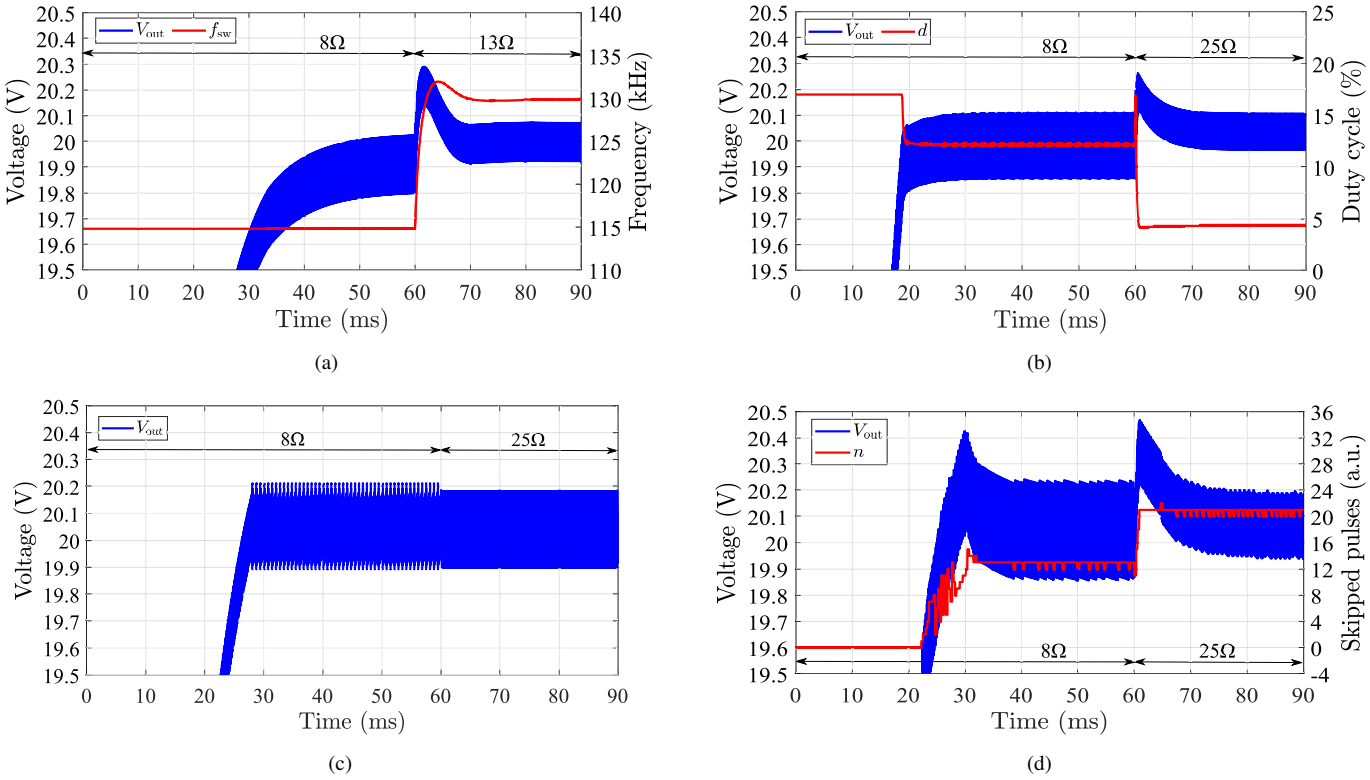

Figure 8: Simulation results of closed-loop regulation of V_{out} in presence of a load step, for the four proposed controllers, using the control parameters of Tab. V. (a) FM; (b) PWM; (c) BB; (d) DDPM.

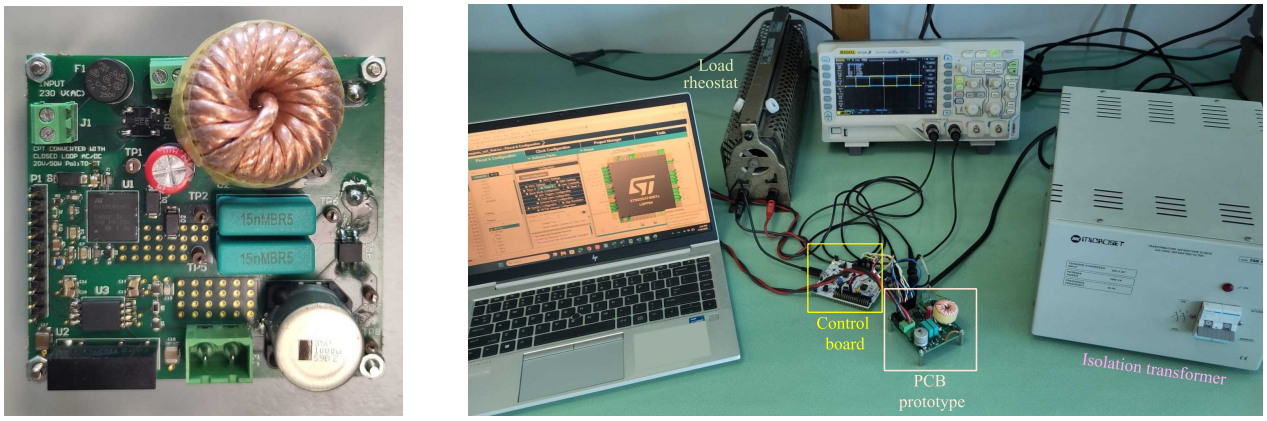

Figure 9: Photos of the converter PCB prototype and the experimental setup used for the testing. (a) PCB prototype; (b) Experimental setup.

controllers according to common figures of merit, such as the ripple superimposed to the output voltage, the settling time (the time required for the controlled variable to reach V_{ref} within a 2 % tolerance) and the observed overshoot caused

Table VI. Bill of material of the converter prototype.

Component	Part number
GANFETs $M_1 - M_2$	MASTERGAN1
Grid rectifier	Z4GP206L-HF
Input capacitor C_{in}	860021374027
Resonant inductor L	N/A (custom, 37 µH)
Isolating capacitors $C_1 - C_2$	PHE850EB5150MB15R17
Load rectifier $D_1 - D_4$	CDBHM240L-HF
Output capacitor C_{out}	MAL215099014E3

by the load step, reminding that the controllers were designed according to a common bandwidth. As it can be seen, the BB and DDPM controllers introduce a larger voltage ripple due to the alternate ON-OFF states of the control voltage pulses. The PWM controller ensures the fastest settling time, while the BB controller minimizes the overshoot in correspondence of the load step, since the controlled voltage is forcibly bounded within the designed hysteresis band.

V. Experimental Results

A PCB prototype, shown in Fig. 9a, was built based on the specifications and design parameters of Tab. I. Specific choices for the bill of material (BOM) of the prototype were taken to maximize the power density: the gate driver and power GANFETs are integrated in the same package, integrated bridge rectifiers are used for the two rectifying stages, and a relatively low capacitance (22 µF) is used to stabilize the DC rail voltage V_{in}. Such a value of C_{in} allows to select a compact capacitor, at the expense of expected larger fluctuations on V_{in}. The BOM is listed in Tab. VI. The goal of the experimental testing is to validate the converter operation in the four modulation strategies, as an essential step for the implementation of the closed-loop controllers. The testbench used for the experimental tests is shown in Fig. 9b: the grid voltage is fed to the converter through an isolation transformer, while a rheostat is used as load resistance. The gate signals are generated from a STMicroelectronics NUCLEO-G474RE development board.

Fig. 10 shows some of the relevant converter waveforms, namely the control voltage of the low-side transistor v_{GS2}, the switching node voltage v_{sw}, the isolating capacitor C_2 voltage v_{C2}, and the resonant current i_L, at the rated 8 Ω load, in the four controllers cases. Fig. 10a refers to the rated operation in FM with f_{sw} = 115 kHz and d = 50 %, characterized by equal current stresses and ZVS for both the GANFETs. As described in [13], each switching period contains multiple resonant periods, and the frequency range is selected to avoid the complete damping of the resonant current, necessary condition to achieve the ZVS of the half-bridge transistors. Fig. 10b shows the same waveform in the PWM case, with f_{sw} = 115 kHz and d = 17 %, highlighting the asymmetrical operation of the converter within a switching period. The current stresses become unbalanced between the half-bridge transistors, but the polarity and amplitude of the

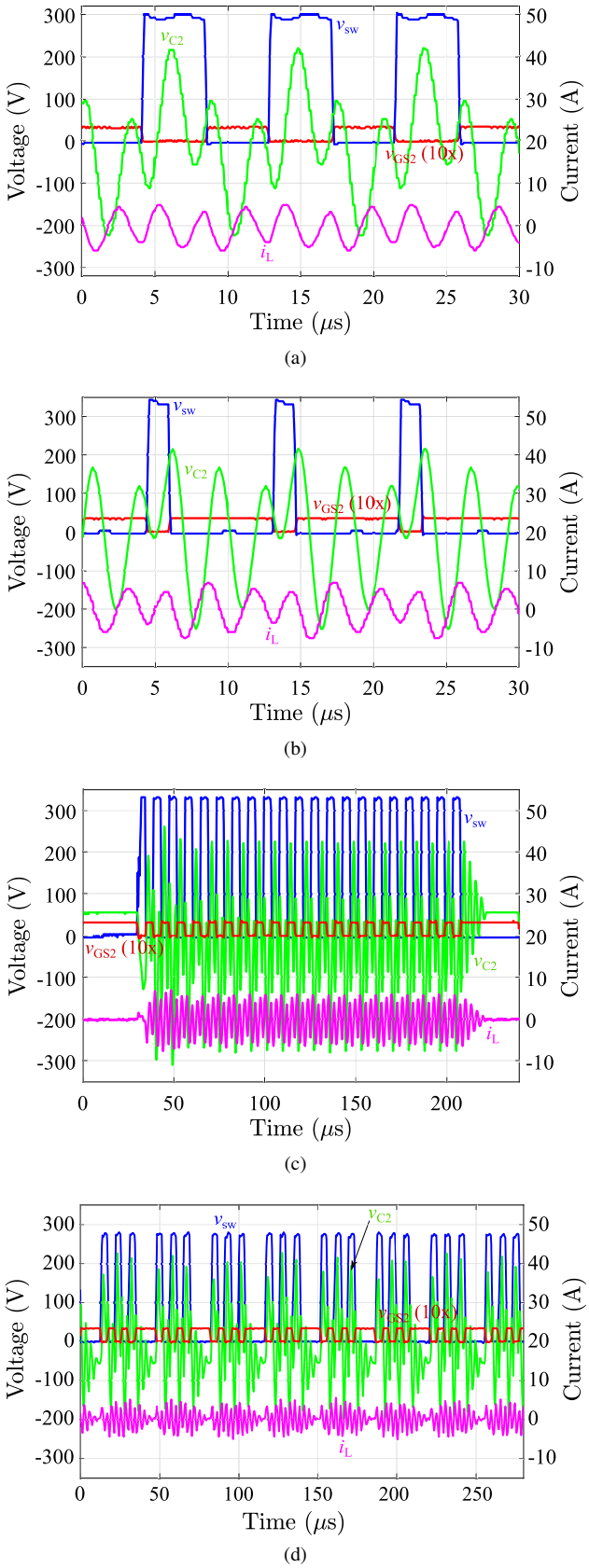

Figure 10: Main relevant voltage (v_{GS2}, v_{sw}, v_{C2}) and current (i_L) waveforms for the four controllers, extracted for 8 Ω load resistance and 20 V output. (a) FM; (b) PWM; (c) BB; (d) DDPM.

resonant current in correspondence of the switching events are still sufficient to ensure their ZVS. Fig. 10c shows the converter waveforms during the BB controller operation. During the OFF state, v_{GS2} is kept "high" to force the switching node voltage to 0, in order to prevent the power transfer from the grid. During the ON state, the waveforms reproduce perfectly the symmetric operation of the FM (Fig. 10a), with balanced current stresses and ZVS for the GANFETs. When the upper voltage threshold is reached, the converter switches to the OFF state, and the resonant current exponentially decays to 0. As a result, the first commutation of the following ON state sequence will be hard-switched. It is important to notice that the duration of the ON state depends on the instantaneous C_{in} voltage and load, while the duration of the OFF state is uniquely related to the time constant of the load, i.e. on the load resistance. No significant current spike is observed during the transition between OFF and ON states. Finally, Fig. 10d shows the waveforms in the DDPM case, in which 8 switching pulses are skipped out of a stream of 32 ($N = 5$). Since the implemented algorithm distributes uniformly the skipped pulses, the converter operation exhibits a $4T_{sw}$ periodicity. The ZVS is achieved inside the streams of consecutive switching pulses, but is lost every time one or more of them are skipped.

VI. Conclusion and Future Work

This work addresses the voltage control design for a step-down grid adapter with capacitive isolation. Due to the innovative MPDR operating mode of the converter, no previously established control strategies were developed. Thus, four different control approaches are designed and compared in simulations on the basis of common figures of merit. The distinctive features and limitations of each controller are investigated. While FM and PWM ensure the lowest output voltage ripple, BB minimizes the overshoot in correspondence of load steps. The PWM controller seems to exhibit the best trade-off between fast startup and low overshoot, but the impact of the asymmetric current stresses on the converter transistors should be more deeply investigated in experimental tests. At the same time, the discontinuous operation of the BB and DDPM may improve the converter efficiency. Preliminary experimental results validate the converter operation with the four different modulation strategies, at the rated load. The future work includes the firmware implementation of the closed-loop controllers and the experimental comparison of the dynamic performances, with a specific eye on the converter efficiency and electrical stresses on the components.

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