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Dynamic Redistribution of Switching Losses in Parallel Connected SiC MOSFETs for Active Thermal Balance

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***Abstract*—SiC MOSFETs are quickly replacing silicon-based devices in high-power applications because of their enhanced electrical and thermal performance. However, due to fabrication limitations, commercial SiC dies have lower current ratings compared to their silicon counterparts. Consequently, multiple SiC MOSFETs need to be connected in parallel for high-current applications. This leads to thermal imbalances among the devices, caused by asymmetrical layouts and parameter mismatches. To tackle this problem, this paper presents an active thermal balancing control strategy that monitors the case temperatures of parallel-connected SiC MOSFETs and dynamically redistributes the switching losses among the power devices. The proposed solution enables optimal utilization of each device, eliminating the need for current derating that is commonly necessary in parallel-connected switching devices. Experimental results are provided to verify the proposed approach.**

Keywords—SiC MOSFET, Parallel Connection, Active Temperature Balance, SOA, Current Derating.

I. Introduction

SiC MOSFETs are becoming an increasingly popular option in power electronic applications due to their excellent thermal properties and ability to withstand high voltages and fast switching speeds [1]. Despite their advantages, utilizing SiC-based converters in high-power applications presents certain design challenges. One key limitation is their relatively low current rating which can limit their use in applications such as electric vehicles and renewable energy systems [2]. This limitation in achieving high current with individual SiC MOSFET dies arises due to factors related to manufacturability constraints [3]. Consequently, to enhance current capability in high-power applications, such as automotive, aerospace, and industrial systems, multiple SiC MOSFETs must be connected in parallel. Nevertheless, external circuit asymmetries and device parameter mismatch, arising from the less mature manufacturing process of SiC MOSFETs in comparison to Silicon-based semiconductors, result in current and temperature imbalance issues, leading to uneven loss distribution among the devices and compromising the reliability of the system [4]. To address this issue, various techniques for paralleling SiC MOSFETs have been proposed in the literature. State-of-the-art current sharing techniques include passive and active balancing methods, each with their respective strengths and limitations.

Passive methods include chip screening techniques which classify the devices with matching parameters [5], and tuning circuit parameters through the use of external components, such as differential inductors and decoupling capacitors, to increase current loop impedance and restrain circulating currents [6]. These techniques enhance current sharing but they restrict the design flexibility of the power converter, fail to adapt to component parameter deviation over time due to aging [7], and introduce additional parasitics that can lead to voltage overshoot.

Conversely, **active methods**, including Active Gate Drivers [8], [9] and feedback systems using FPGA [10], can real-time control the switching dynamics of individual MOSFETs, improving current distribution and reducing thermal stress on the devices. However, their main drawback is that these methods can be costly and complex to implement, especially in fast-switching conditions where accurate timing and current sensing are crucial.

This work presents an active thermal balance control system that leverages the case temperatures of parallel-connected SiC MOSFETs to maintain thermal equilibrium and indirectly ensure more equitable current distribution. By adjusting the reference duty cycle of each device, the switching losses are redistributed among the devices, preventing excessive thermal gradients and improving overall reliability.

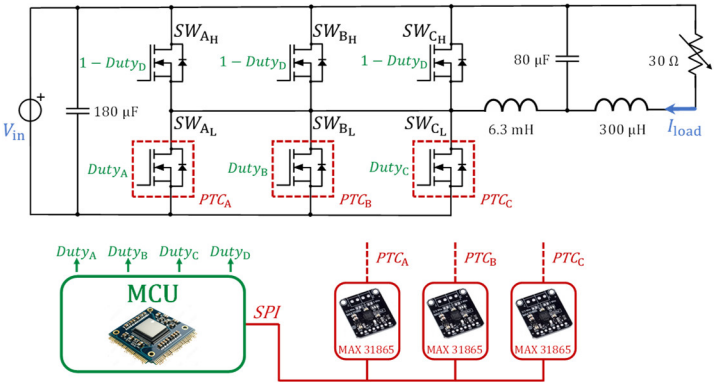


Fig. 1. Functional schematic of the proposed experimental setup.

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II. Proposed Approach

A. System Configuration

Fig. 1 shows the simplified power schematic of the test setup used for the validation of the proposed approach. It consists of a half-bridge converter with three parallel-connected IMZ120R030M1H 30 mΩ CoolSiC 1200 V SiC trench MOSFETs, manufactured by Infineon, on both the low and the high side. Each low-side MOSFET has a dedicated gate driver, while the high-side devices share a common gate driver. The converter is supplied by a DC voltage generator and the load consists of a variable resistor interfaced with the converter through an LCL filter. The low-side MOSFETs are thermally monitored via PTC thermistors and actively balanced according to the proposed method. It must be noted that in the proposed setup the load current is entering the switching node, therefore **only the low-side devices are operating in thermally critical hard switching mode, while the high-side switches are operating in soft switching mode**.

B. Thermal Balancing Control

Fig. 2 shows the functional schematic of the proposed thermal balance control where the temperature of one of the low-side devices is selected as the reference temperature (e.g. device B_L is selected as the reference device) while the temperatures of the remaining devices (i.e. devices A_L and C_L) are actively controlled by adjusting the reference duty cycle so that the temperature of each device matches the temperature of the reference device.

In other words, when a temperature mismatch occurs between a device and the reference device, the duty cycle of the corresponding device is offset by the corresponding proportional-integral (PI) regulator to redistribute the switching losses and eventually balance the temperatures. In this case, $Duty_B$ equals the reference average duty cycle of the half-bridge converter, while $Duty_A$ and $Duty_C$ are offset with respect to the average duty cycle for active thermal balance. The duty cycle $Duty_D$, common to all the high-side devices, is computed assuming to have only one device at the low-side whose duty cycle is the maximum one between $Duty_A$, $Duty_B$ and $Duty_C$. This enables adding the correct dead time without any risk of leg short circuit.

Two compensation methods are investigated, as shown in the experimental tests:

a) **Selective Turn-On Compensation**: the duty cycle offset is synchronized to the turn-on command, as shown in Fig. 3a. This approach aims to redistribute switching losses by controlling the turn-on events.

b) **Selective Turn-Off Compensation**: the duty cycle offset is synchronized to the turn-off command, as shown in Fig. 3b. This approach aims to redistribute switching losses by controlling the turn-off events.

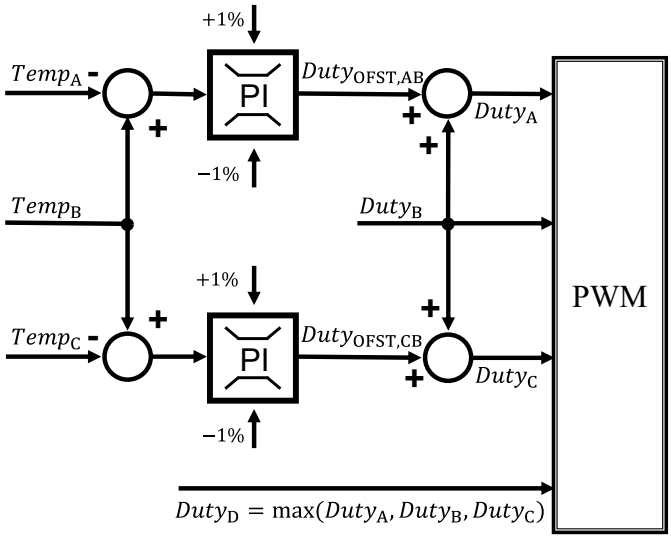


Fig. 2. Functional schematic of the proposed thermal balance control.

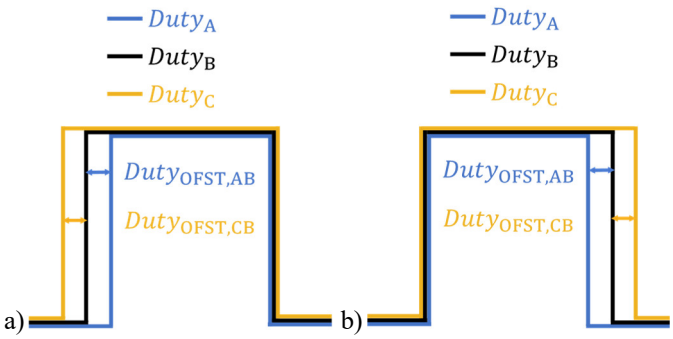


Fig. 3. Representation of duty-cycle offsets from reference $Duty_B$.

III. Experimental Set-Up

Fig. 4 shows the experimental setup for validating the proposed control strategy, as schematically shown in Fig. 1. The low-side MOSFETs' case temperatures are monitored using PTC thermistors connected to a MAX31865 conditioning circuit. This circuit communicates the measurements to the MCU board via multi-slave SPI, enabling the MCU to drive the switches. The selected MCU embeds a high-resolution timer enabling 0.002% duty cycle discretization, considering a switching frequency of 100 kHz and a dead time of 500 ns. Each device has a dedicated, naturally cooled heatsink as shown in Fig. 4b and the leg layout is intentionally asymmetrical.

To evaluate the performance of the proposed control strategy, a constant load current test was performed for three cases:

1) **Without thermal compensation**, with $Duty_A = Duty_B = Duty_C$.

2) **With selective turn-on active thermal compensation**, where the turn-on of the devices is anticipated or delayed while keeping the turn-off synchronized as shown in Fig. 3a.

3) **With selective turn-off active thermal compensation**, where turn-off is changed keeping the turn-on synchronized as shown in Fig. 3b.

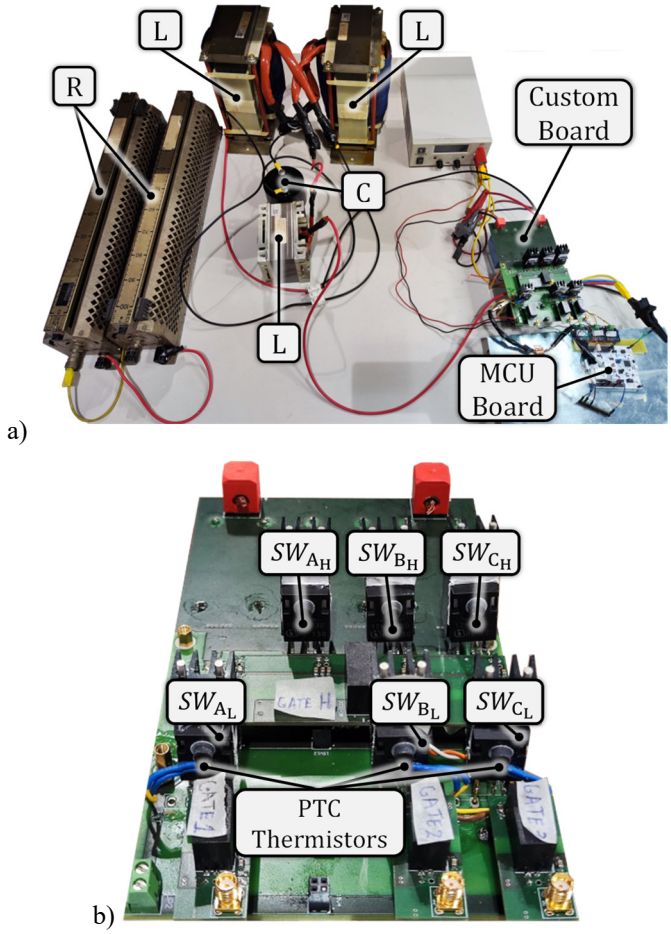


Fig. 4. Experimental test rig: a) Testbench overview. b) Custom power board.

IV. Experimental Results

Experimental results are illustrated in Fig. 5 for the following test conditions: $Rg_{low_ON} = Rg_{low_OFF} = 39\ \Omega$, $Rg_{high_ON} = Rg_{high_OFF} = 18\ \Omega$, $Vg_{ON} = 15\ V$, $Vg_{OFF} = -5\ V$, $R_{load} = 30\ \Omega$, $V_{in} = 500\ V$, $Duty_{ref} = Duty_B = 55\%$ and $f_{sw} = 100\ kHz$, thus resulting in a constant load current of around 7 A. The control's interrupt service routine has a frequency of $f_{ISR} = 20\ kHz$. The modulation is stopped automatically when any thermistor reaches 80°C, thus avoiding to damage the system. All tests start with the devices being at room temperature.

Fig. 5a refers to the case **without thermal compensation,** where the temperature limit of 80°C is reached after 82.8 s with a maximum temperature imbalance of 14.43°C between the coolest device C_L and the hottest device B_L.

Fig. 5b refers to the case with **selective turn-on compensation.** In this case, thermal balance is achieved by effectively redistributing the switching losses among the devices, extending the time to reach the temperature limit of 80°C to 96.7 s. The duty cycle compensation offsets reported in the bottom plot are very low, below 0.2% of the duty cycle, thus having a negligible impact on the load voltage.

Fig. 5c refers to the case with **selective turn-off compensation,** where the temperature limit of 80°C is reached after 80.5 s coinciding with a maximum temperature imbalance of 14.87°C between the coolest device C_L and the hottest device B_L, and no effective balancing effect. In this case results are similar to the case without thermal compensation and the thermal imbalance is unsolved. The duty cycle compensation signals reported in the bottom plot reach the saturation limit set to 1%. The compensation is not effective as the turn-off losses are negligible compared to turn-on losses, as reported in the datasheet of the component [11] and do not impact thermal performance.

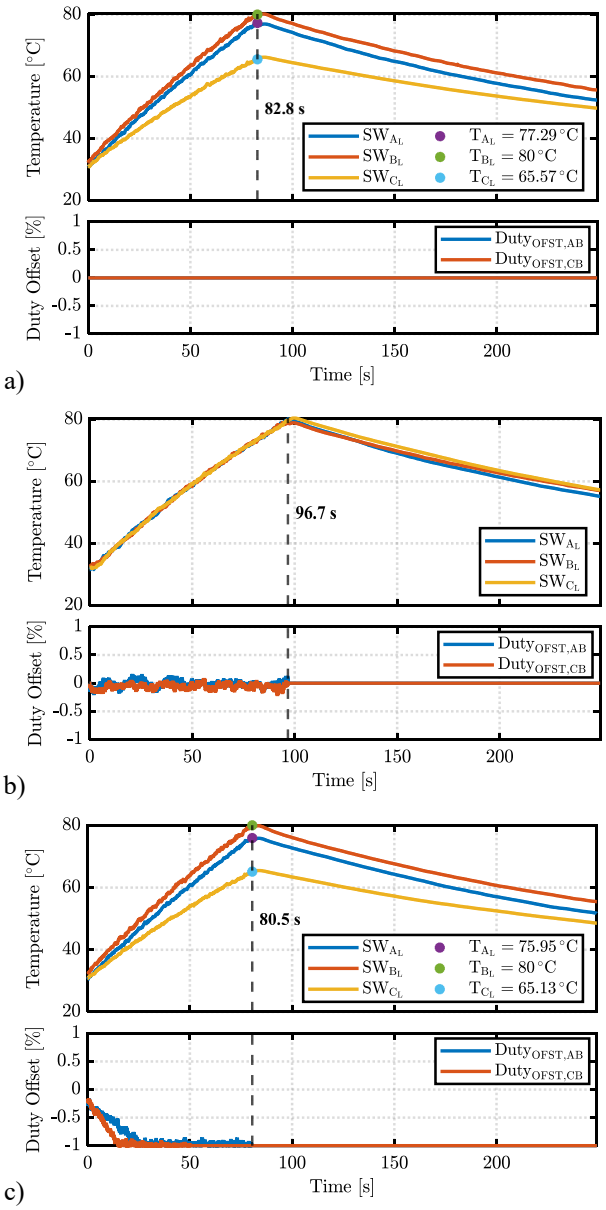


Fig. 5. Temperatures and duty-cycle offsets of the devices during the constant current test at 7 A load current. a) No active temperature balance control. b) Selective turn-on active temperature balance control. c) Selective turn-off active temperature balance control.

V. Data Analysis and Considerations

A. System Configuration

The proposed technique improves the distribution of losses, which helps to reduce both the maximum operating temperature and the thermal fluctuations of the devices, all while maintaining the same operating conditions (i.e., the same output current, switching frequency, output voltage and so on).

A comparison between the temperature rise shown in Fig. 5a (without thermal compensation) and Fig. 5b (with selective turn-on compensation) clearly shows that the maximum temperature limit is reached significantly later when selective turn-on compensation is applied. Differently said, under the same load condition in the case of active turn-on compensation, the temperature of the hottest switch will be considerably lower compared to the case without compensation.

This comparison is pointed out in the bar plot shown in Fig. 6a, which shows the **temperature difference** among the three switches in the case without compensation (Fig. 5a) and in the case with turn-on compensation (Fig. 5b), measured at specific time instants. For example, after 20 seconds from the beginning of the test, the temperature of the switch B_L is around 3°C higher in the case without compensation, with respect to the case with turn-on compensation. On the contrary, the temperature of the switch C_L is 2°C lower. However, when assessing component aging, it is crucial to consider the worst-case operating condition, which in this case is determined by the higher temperature of the switch B_L. As the test progresses, after 80 seconds, the selective turn-on compensation achieves a 6°C maximum case temperature reduction of the hottest device B_L.

By reducing the maximum case temperature between the devices, the proposed technique enables a reduction in both the maximum switch junction temperature and its' swing during the power cycle. As it is widely accepted in the literature, the number of cycles to failure depends upon these two conditions [12]-[15]. As a result, selective turn-on compensation enhances the system's lifetime and overall reliability.

On the contrary, as we can see in Fig. 6b, between the selective turn-off compensation and no applied compensation, the difference of the devices' case temperatures is minimal. This is because, as mentioned in Section IV, the compensation was not effective because turn-off losses were negligible and did not impact thermal performance.

B. Long Term Reliability and Self Resilience

Even as the aging process will eventually lead to the degradation and alteration of the devices' parameters, the proposed methodology is based on the measured case temperature of the devices, therefore it is substantially more reliable than approaches that use TSEP parameters to estimate the junction temperature of the devices [9], [16]-[19].

Furthermore, when one of the devices' parameters changes (i.e. $R_{DS_{ON}}$ increase) the system will automatically redistribute the switching losses to the remaining devices, reducing its thermal stress and eventually achieving the increase of the lifetime of the worn-out device. By achieving self-resilience in a system of parallel SiC MOSFET configuration where its lifetime is dictated by the average lifetime of all the devices, the proposed methodology is successful in extending the system's longevity and long-term reliability.

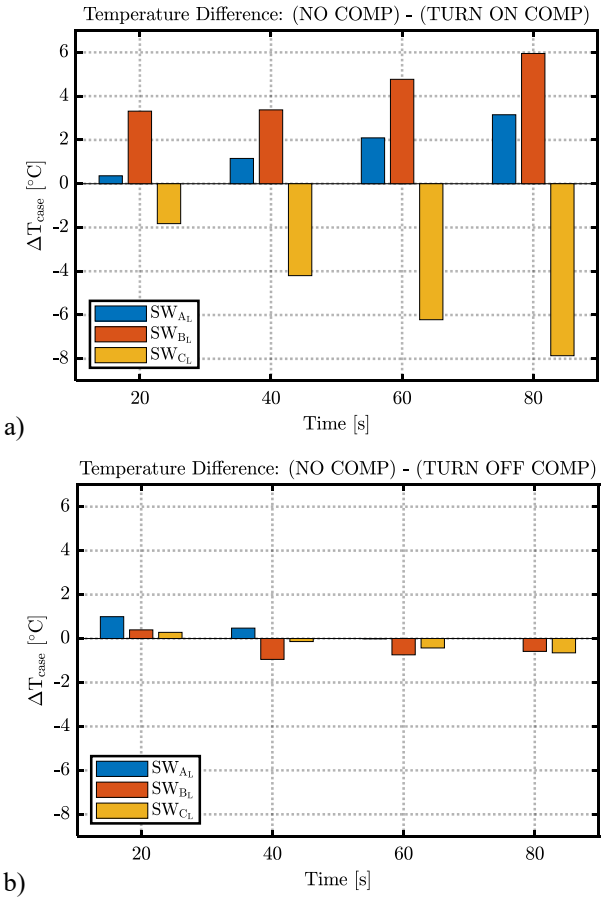


Fig. 6. Temperature difference comparison of each device at four time snapshots between: a) No active temperature balance control and Selective turn-on active temperature balance control, b) No active temperature balance control and Selective turn-off active temperature balance control.

VI. Redistribution of Switching Losses via Active Compensation

In this section, the analysis focuses on the redistribution of turn-on losses among the paralleled low-side MOSFETs, as these events represent the dominant contribution to overall switching losses. Measurements related to the turn-off process are omitted, since their impact on thermal performance is minimal in the present operating conditions. The instantaneous current through each device was captured during turn-on transitions for the different compensation strategies, utilizing three SDN-414-01 coaxial shunt resistors. Both compensated and uncompensated cases are presented to illustrate how the controller dynamically reshapes the distribution of switching losses and case temperatures. All oscilloscope snapshots correspond to representative instances during constant-current operation, with the compensation-induced duty cycle offsets varying continuously according to the control action (for example, the continuous adjustment is depicted in Fig. 5b).

A. Switching Loss Redistribution during Turn-on

Fig. 7 presents the time-domain responses during the turn-on event for each control approach.

- No Compensation (Fig. 7a) With all three low-side MOSFETs driven using identical duty cycles, turn-on occurs simultaneously for each device. This leads to persistent thermal imbalance, matching the trend reported in Fig. 5a, with switching losses distributed nearly equally.

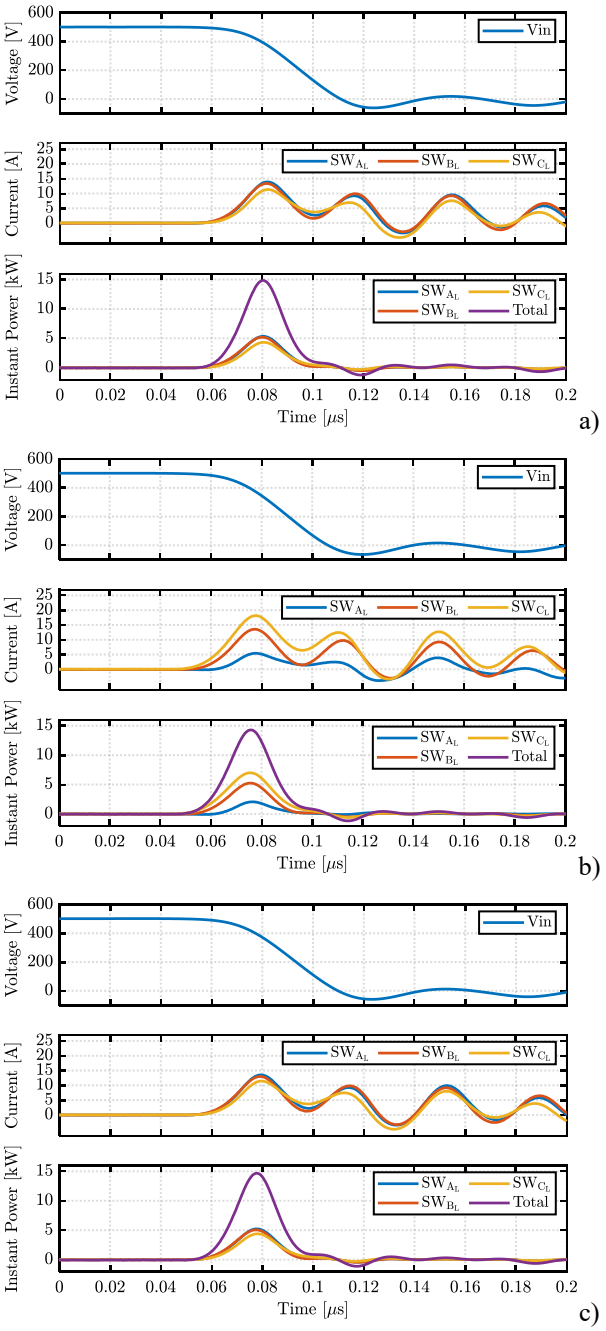


Fig. 7. Current and instant power of the low-side devices during turn-on. a) No compensation. b) Selective turn-on compensation. c) Selective turn-off compensation.

- Selective Turn-On Compensation (Fig. 7b) The compensator recognizes the temperature mismatch among the devices and advances the turn-on signal of C_L, while delaying the turn-on signal of A_L, relative to B_L. Therefore, turn-on losses are primarily on C_L and B_L, while device's A_L losses are substantially decreased. This effective redistribution of the turn-on switching losses minimizes the thermal imbalance among the devices.

- Selective Turn-Off Compensation (Fig. 7c) The devices turn on simultaneously, without redistribution of turn-on switching losses, as this technique does not impact the turn-on signals. The waveforms are similar to the case with no active thermal compensation.

B. Steady State Current Sharing

The current waveforms during conduction steady-state conditions were compared for the two cases of No Compensation and Selective Turn-On Compensation, as shown in Fig. 8. In both cases, device currents are not equally distributed due to the different R_{ON} of the chips. The positive R_{ON} temperature coefficient partially redistributes currents among the devices by limiting the current in the hotter ones, but this does not guarantee thermal equilibrium. The results further confirm that the major contribution to the thermal imbalance is related to the switching losses, which are predominant compared to the conduction losses in this system, operated at 100 kHz . Other imbalances derive from the parametric dispersions of the thermal conductivity of the switches, as reported in the datasheet of the component [11].

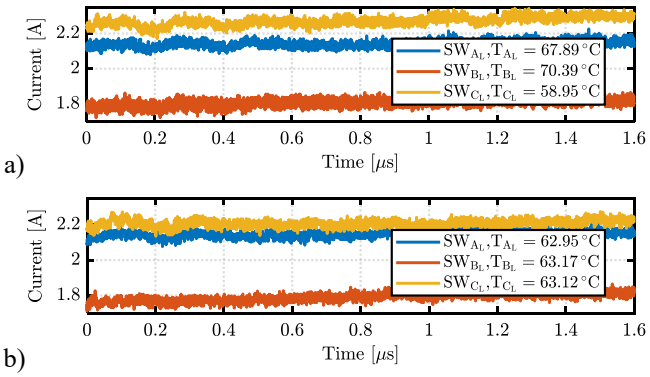


Fig. 8. Current sharing among the low-side devices during conduction. a) No compensation. b) Selective Turn-on compensation.

C. Comparative Assessment of Turn-on Loss Redistribution

The turn-on switching losses of the three low-side devices were calculated by integrating the instantaneous switching power over the switching period for the turn-on events. Further analysis of the turn-off losses was not performed, as it was assessed unnecessary in the light of them representing a minor portion of total switching losses, and are only slightly affected by the compensation strategies. The losses were averaged across ten snapshots taken during constant load current tests. The results presented in TABLE I. show how the control techniques impact the distribution of turn-on switching losses. The analysis reveals that while the selective turn-on compensation redistributes the losses among the devices, the total turn-on losses remain nearly identical in comparison to the other cases. This consistency highlights that thermal balancing is achieved without increasing the overall system losses. According to Fig.

5a, without thermal compensation, device C_L remains the coolest device during the constant current test. However, as shown in TABLE I. , the selective turn-on compensation increases the losses of device C_L, redistributing them from the other two devices to achieve thermal equilibrium. Despite this redistribution, the total turn-on switching losses across the devices vary by less than 3 µJ, demonstrating the effectiveness and efficiency of the proposed method.

TABLE I. TURN-ON LOSSES

Device / *Comp. Mode*	A_L	B_L	C_L	*Total (uJ)*
-	106	103.3	88.2	297.5
Turn-On	68.2	96.6	134.9	299.7
Turn-Off	107.7	103.2	88.3	299.2

VII. CONCLUSIONS

This paper introduces an active thermal balancing control strategy aimed at addressing the thermal imbalances inherent in parallel-connected SiC MOSFETs by utilizing the case temperature feedback and dynamically redistributing switching losses among devices. Experimental validation highlights the effectiveness of the selective turn-on compensation in achieving thermal equilibrium, reducing temperature imbalances, and enhancing system reliability and expected lifetime. Conversely, the selective turn-off compensation is ineffective due to the negligible contribution of turn-off losses on thermal performance, as most of the switching losses occur during the turn-on phase. The proposed strategy offers key benefits, including simplicity, cost-efficiency, and robustness, without relying on complex junction temperature estimation. Additionally, it provides inherent self-resilience by adapting to device degradation, thus improving the expected lifetime of the system. This innovative method presents a practical and scalable solution for improving the performance and lifecycle of SiC-based power converters, with promising potential for broader applications in industrial and renewable energy systems. Future work will focus on expanding the approach to multi-phase configurations and diverse load conditions to further study its industrial applicability.

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