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***Abstract*—This work presents a novel SPICE modeling methodology for accurately predicting the dynamic switching behavior of parallel-connected Silicon Carbide (SiC) MOSFETs. In high-power converter applications, parametric dispersion among nominally identical SiC devices-such as variations in gate threshold voltage, transconductance and conduction resistance-poses a significant challenge to balanced current sharing and thermal balance. By leveraging Double Pulse Test (DPT) experimental data, the proposed approach addresses the critical issue of parametric dispersion in SiC devices by enabling the emulation of individual device behavior under transient switching conditions, which is essential for designing reliable high-power converters. The proposed technique does not require modification of the internal SPICE model of the MOSFET, which is often encrypted or vendor-specific, instead, external gate-driving parameters are selectively tuned to emulate the dynamic response of each device. This preserves model integrity while significantly improving simulation accuracy, supporting a wide range of application domains, including electric vehicles, renewable energy systems, and industrial power electronics. The proposed methodology enhances the design of robust parallel-connected systems, ensuring improved current sharing and reduced thermal stress.**

Keywords—SiC MOSFET, Double Pulse Test (DPT), SPICE Modelling, Parallel Operation.

I. Introduction

Silicon Carbide (SiC) MOSFETs have become essential in modern high-power converters due to their superior electrical characteristics, including higher switching speed, reduced conduction losses, and enhanced thermal performance compared to traditional silicon-based devices [1], [2]. Their excellent trade-off between high-voltage ratings and low conduction resistance makes them particularly suitable for applications demanding high efficiency, compactness, and robustness, such as electric vehicles, renewable energy systems, and advanced industrial drives [3]-[6]. Nevertheless, as a relatively new technology, their current capability per die remains limited compared to more mature silicon (Si) devices [7]. Consequently, high-current applications typically require multiple devices to be connected in parallel [8].

However, parallel-connected SiC MOSFETs exhibit complex switching behavior, highly driven by intrinsic variation in device parameters such as gate threshold voltage, transconductance, conduction resistance, and switching speed. Even slight discrepancies among these parameters can significantly affect the dynamic current sharing during the device commutation [9], leading to uneven thermal stress distribution, localized overheating, and therefore system reliability concerns [10]. These imbalances are further exacerbated by asymmetrical circuit layouts and parasitic inductances, inherent in power electronic converter printed circuit boards [11].

Several methodologies have been proposed to address these challenges, including passive solutions like parameter-based chip screening [12]-[14], carefully matched circuit layouts [15] and active gate driving strategies [16], [17]. However, chip screening does not comprehensively address transient switching behaviors due to its reliance on static transfer curves or simplified parameter estimations. Passive methods, although straightforward, typically lack adaptability and cannot compensate for device parameter degradation over operational lifetime. In contrast, active gate driving strategies dynamically adjust the gate signals of individual MOSFETs to equalize transient currents and device temperatures, improving thermal distribution and enhancing reliability, nevertheless at the cost of increased complexity and expense.

In parallel, significant advancements have been made in simulation techniques to predict the transient behavior of SiC MOSFETs accurately. SPICE-based simulation approaches have emerged as the standard due to their broad acceptance in industry and academia, providing a practical trade-off between model complexity, computational speed, and accuracy [18]. Recent SPICE modelling techniques incorporate empirical adjustments, behavioral subcircuits, and refined gate voltage-dependent capacitances, effectively capturing device-specific transient characteristics observed experimentally [18], [19]. Alternative modelling approaches, such as physics-based electrothermal models and compact semi-physical representations, have also been developed to address specific simulation limitations of standard SPICE models [20], such as limited accuracy under high-frequency transient conditions, inadequate description of temperature-dependent effects, and poor convergence or instability while modelling complex switching events. Despite these advancements, accurately modeling the dynamic interaction among parallel-connected SiC MOSFETs remains challenging, primarily due to parametric dispersion, encrypted manufacturer models, and difficulties in accurately representing practical circuit parasitics.

Therefore, there is a critical need for reliable, efficient, and accessible simulation tools capable of predicting the behavior of parallel-connected SiC MOSFETs, explicitly accounting for parameter spread. **This paper introduces a robust modelling methodology for translating Double Pulse Test experimental data into accurate SPICE models. Unlike traditional techniques, the proposed approach enables to accurately reproduce the switching behavior of each component, taking into account the parametric dispersion and does not require altering the SPICE model of the MOSFET that in many cases is encrypted or difficult to manipulate**.

The methodology involves testing multiple samples of the same SiC MOSFET device to quantify parametric variability and calibrating simulation models through targeted gate signal tuning. By adjusting each device's reference gate voltage characteristics, the tuned models enable precise prediction of device switching behavior during parallel operation, facilitating the optimized design and improved reliability of SiC-based power converters.

II. Experimental Characterization of SIC MOSFETs

The Double Pulse Test (DPT) is a widely recognized and standardized method extensively employed in both the industry and academic research for accurately characterizing power semiconductor devices' switching characteristics beyond the limited data provided by the manufacturer's datasheet conditions. In this work, an extensive experimental characterization was conducted using a Keysight PD1500A DPT system (Fig. 1), employing an MXR108A oscilloscope with 8 measurement channels, 16 GS/s sampling rate, and 10 bit vertical resolution, controlled via the dedicated PD1000A Control Software platform.

Fig. 1. Keysight PD11500A Double Pulse Test (DPT) system used for the high-precision characterization of 30 Infineon IMZ120R030M1H 30 mΩ CoolSiC 1200 V SiC trench MOSFETs.

A batch of 30 samples of Infineon's IMZ120R030M1H 30 mΩ CoolSiC 1200 V SiC trench MOSFETs were systematically tested. The measurement configuration closely replicated an actual inverter leg arrangement to ensure practical applicability of the collected data. Specifically, as shown in Fig. 2, one of the devices was placed in the high-side position, with its intrinsic body diode utilized during each DPT sequence, while the remaining devices (DUTs) were sequentially substituted into the low-side position.

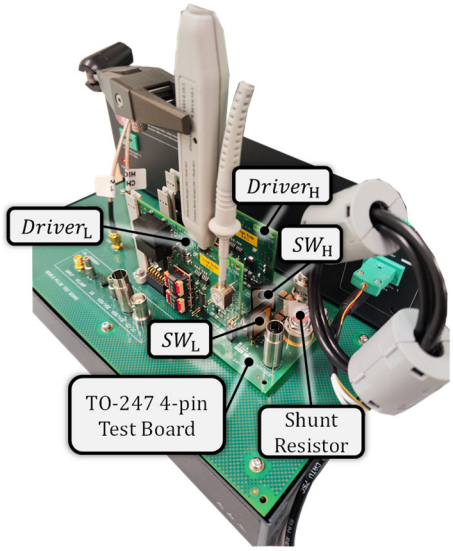

Fig. 2. Test configuration highlighting DUT, gate drivers, and current sensing.

All devices underwent a series of identical switching tests for the following experimental conditions: the gate resistances for turn-on and turn-off events were fixed at Rg_{low}=Rg_{high} = 2.5 Ω, with gate driving voltages maintained at V_{g-} = 0 V and V_{g+} = 18 V, respectively. Each device was subjected to a consistent load current I_{load} = 25 A, and a fixed DC-link voltage V_{in} = 800 V, conditions representative of a practical high-power converter scenario.

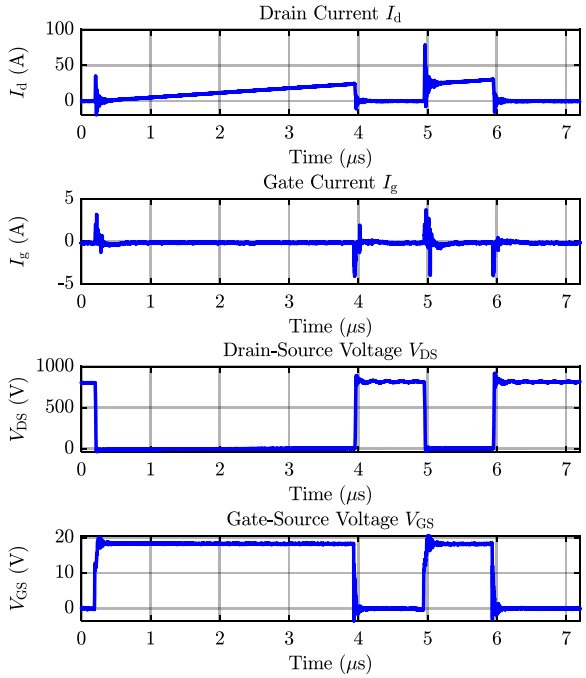

Fig. 3. Representative DPT test output waveforms, showing the drain current I_d, gate current I_g, drain to source voltage V_{DS}, and gate to source voltage V_{GS}.

Through testing, critical waveforms-including the drain current I_d, gate current I_g, drain to source voltage V_{DS}, and gate to source voltage V_{GS} -were recorded, as shown in Fig. 3, allowing detailed analysis of device-specific transient behaviors. The experimental results show the abovementioned parametric dispersion across the sampled devices, notably in switching times T_{rise} and T_{fall} and gate threshold voltages. As mentioned in Section I, such spread in the device parameters can have significant implications for parallel-device operation, potentially causing transient current imbalances and resulting in device overstressing and reduced reliability.

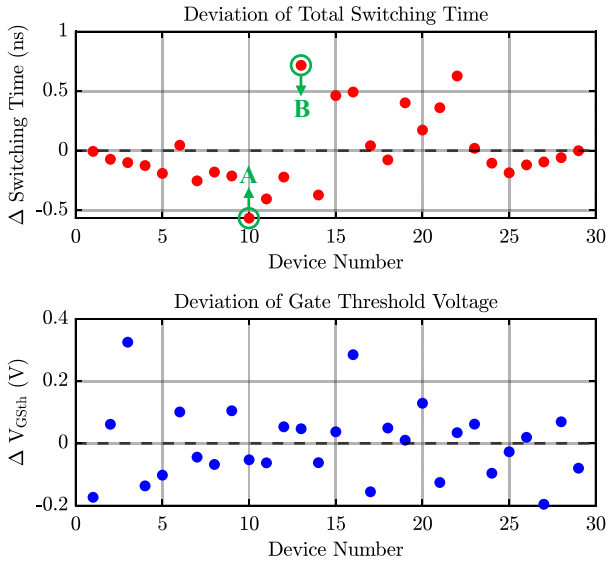

Fig. 4. Total switching time and gate threshold voltage variation among the tested devices.

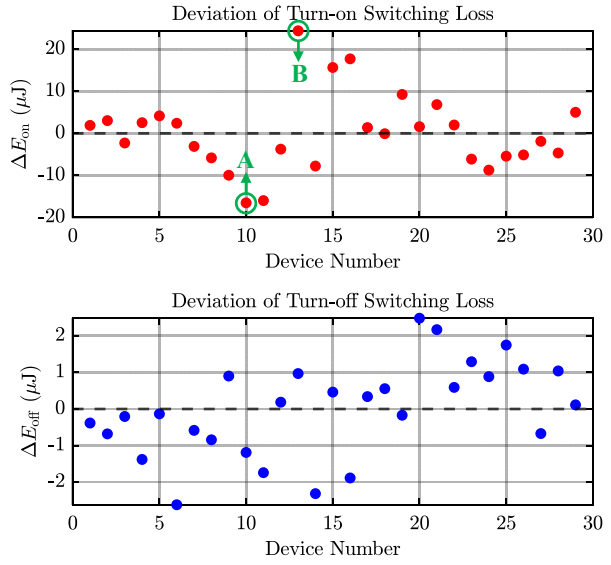

Fig. 5. Turn-on and turn-off switching loss variation among the tested devices.

As can be seen from Fig. 4, the two devices with the most significant variation of switching times between them ($T_{rise} + T_{fall}$) are devices 10 (lowest) and 13 (highest), named devices A and B respectively, for ease of discussion in the rest of the paper. As expected, these variations in turn-on and turn-off switching time transitions lead to corresponding deviation in turn-on and turn-off switching losses, as can be seen in Fig. 5. Again, devices A and B represent the samples with the most significant variation of turn-on switching losses, which in this case represent the predominant switching loss factor, in comparison to the turn-off switching losses, as specified in the device's datasheet [21].

These extreme cases were selected for further investigation as they represent worst-case scenarios in the parallel operation of power devices. Fig. 6 shows the comparison of the rise and fall time transitions of V_{ds} and I_d among devices A and B during the DPT test. It is possible to note that device A turns on and off considerably faster than device B. Accurately replicating these differing switching characteristics in the developed SPICE simulation model is essential for predicting their behavior when connected in parallel.

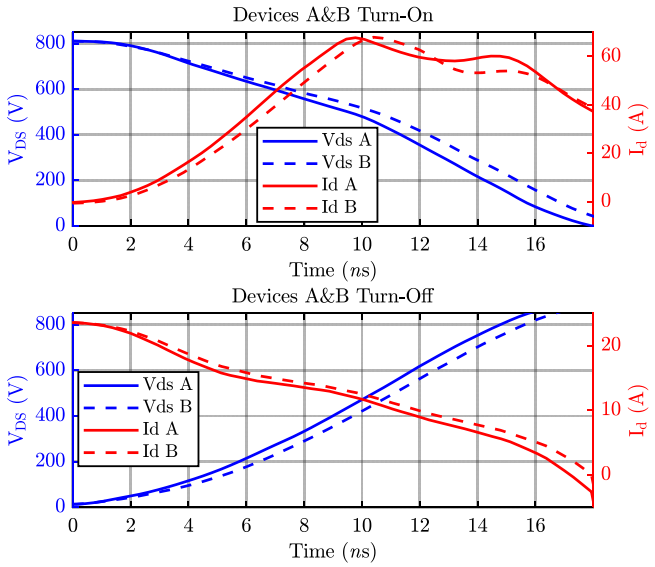

Fig. 6. Switching transitions of devices A and B.

III. SPICE Model Development and Calibration

Accurate SPICE modelling of SiC MOSFETs remains challenging due to the inherent complexity of capturing non-linear transient behaviors and precise device-specific characteristics, often further complicated by limited or encrypted manufacturer-provided models. The modelling approach proposed in this paper targets to counter these limitations by leveraging external gate-driving signal adjustments, eliminating the necessity to modify internal device models.

To replicate the DPT results in simulation, a detailed model was developed in LTSpice, using the manufacturer's provided SPICE model for the IMZ120R030M1H, which comprehensively includes the non-linear device capacitances ($C_{iss}, C_{rss}, C_{oss}$), the body diode of the device with its intrinsic reverse recovery characteristics, the parasitics of the package, and so on. The test circuit, presented in Fig. 7, was built to mirror the experimental DPT setup, including the same half-bridge topology and power loop stray inductance.

The proposed approach does not require modifying the SPICE model of the MOSFET which may be encrypted or complex to understand (different manufacturers use different approaches for building their SPICE models), but simply consists of appropriately tuning two dedicated external voltage sources (V1 and V2) for precise calibration. In particular, V2 enables to modify the threshold voltage of the device with a major impact on the turn-on and turn-off delay times, and a marginal impact on the T_{rise} and T_{fall} times. For the specific model a range of [0 0.6]V successfully emulated the $[-0.2\ 0.4]$V deviation from the 5 V average value of V_{GSth}. The gate driver representation was realized using V1 combined with a series gate resistor R1 and gate loop inductance L1, effectively replicating the experimentally determined gate-loop dynamics. The gate driver imposes a positive and a negative voltage to turn on and off the power device. By individually adjusting the positive and negative gate voltage signals, we can increase or reduce the slew rate of the turn-on and turn-off transitions respectively, thus calibrating accurately T_{rise} and T_{fall}. This effect arises because a higher $V_{\text{g+}}$ charges the gate-source capacitance C_{gs} more rapidly, reducing T_{rise}, while a more negative $V_{\text{g-}}$ enhances the discharge of C_{gs}, reducing T_{fall}. Conversely, lower $V_{\text{g+}}$ or less negative $V_{\text{g-}}$ result in slower transitions. For our model, the whole range of T_{rise} deviation was achieved by imposing a $V_{\text{g+}}$ of [15.5 16]V while the deviation of T_{fall} was replicated by applying a $[-2 - 1.5]$V range of $V_{\text{g-}}$.

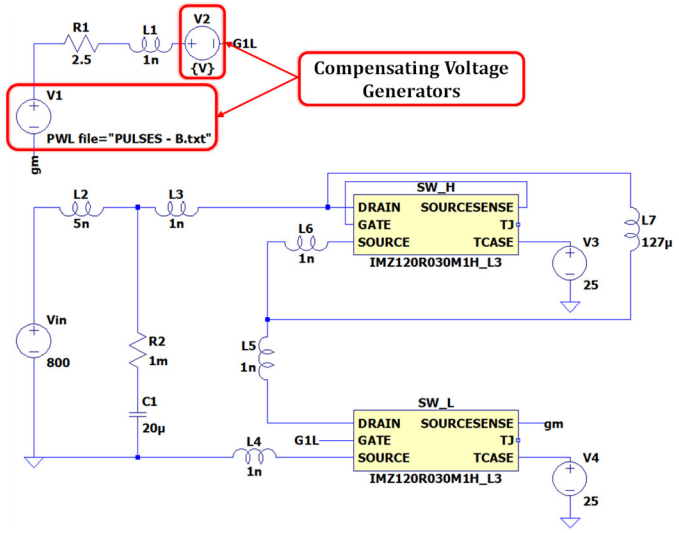

Fig. 7. LTspice circuit of the developed model.

IV. Comparison of Simulation and Experimental Results

After fine-tuning the external compensating gate signals to emulate the switching characteristics of devices A and B, a quantitative comparison between simulation and experimental results was performed. The corresponding fall and rise times were extracted from the simulated and measured waveforms under identical conditions. The resulting values demonstrated an excellent match, with deviations limited to less than 0.02 ns, showcasing the high precision of the calibration process.

Fig. 8 presents an overview of the simulation and experimental comparison between the V_{ds} and I_{d} waveforms during turn-on and turn-off transitions for the two devices. The high level of agreement confirms the capability of the proposed modelling approach to capture device-specific dynamic response, critical for the realistic prediction of parallel operation behavior.

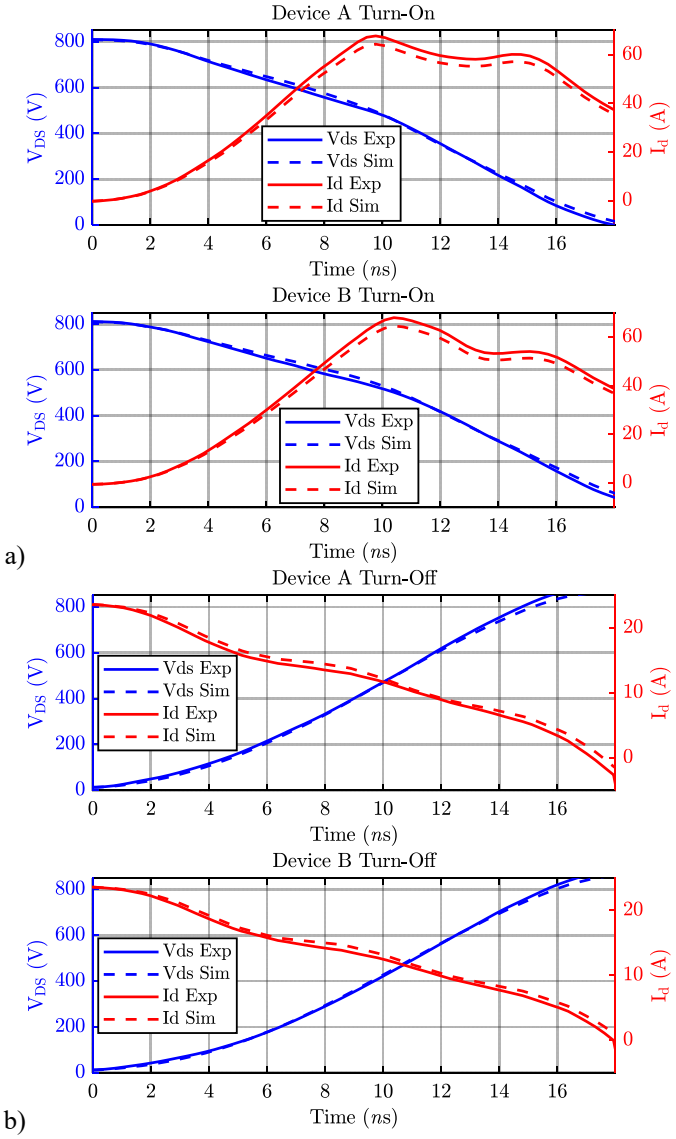

Fig. 8. Experimental vs simulation switching transitions of devices A and B.

The proposed methodology was further evaluated by simulating the parallel operation of devices A and B, taking into account their parametric dispersion in the SPICE environment. The simulation results for the parallel configuration revealed the expected dynamic drain current I_{d} imbalance during the turn-on transition: device SW_{A} (representing device A) consistently exhibited a faster response and absorbed a greater share of the initial current spike, while device SW_{B} (representing device B), showed a slower transition and lower peak current, consistent with its longer T_{fall}. This outcome demonstrates that the model not only reproduces individual device switching dynamics but also emulates the complex transient current sharing that occurs during parallel operation of devices with different switching characteristics. Overall, the results validate the robustness and

predictive accuracy of the proposed modelling methodology for both device characterization and parallel operation conditions.

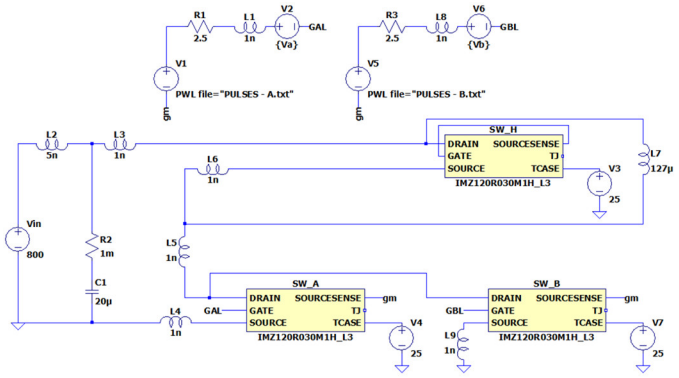

Fig. 9. LTSpice schematic for the parallel operation simulation.

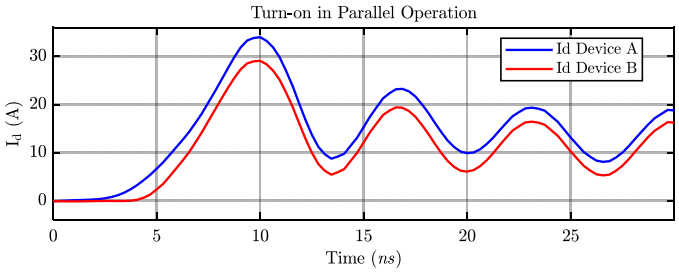

Fig. 10. Current sharing during turn-on transition in parallel operation.

V. Conclusions and Future Work

In this paper, a novel SPICE-based methodology for accurately predicting the transient switching behavior of parallel-connected SiC MOSFETs was proposed, explicitly addressing the critical issue of device parametric dispersion observed experimentally. The developed approach enables the representation of the real switching behavior of each device, enhancing the design of robust parallel-connected systems. Moreover, it does not require modification of the internal model of the devices, which is not always made accessible by the manufacturers, instead uses carefully calibrated external gate-driving parameters. The comparison between experimental and simulated DPT results validates the effectiveness of the proposed model. Future work will focus on a comprehensive extension of the approach, aiming to generalize and automate the modelling framework for a larger scale of SiC MOSFET SPICE models. Furthermore, additional experimental analysis will be performed, not only covering current sharing but also junction temperature unbalance among the switches, which will be monitored using TSEP (Thermo-Sensitive Electrical Parameters) approach [22], [23].

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