MMIC Power Amplifier in GaAs HBT Technology for Wi-Fi 6 Applications

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***Abstract*—This contribution presents a 3.5 W MMIC power amplifier in GaAs HBT technology operating at 5 V supply conceived for Wi-Fi 6 applications in the 5-6 GHz frequency range. A 3-stage corporate architecture is selected to evaluate the technology capability in terms of power, linearity and efficiency. In simulation, the designed amplifier shows a saturated output power in excess of 35 dBm with associated gain and efficiency above 27 dB and 36 %, respectively. At -26 dB of EVM (Error Vector Magnitude, MCS0 standard) the best efficiency achievable, with simple bias tuning, is 17 % with an associated output power of 29 dBm. The small-signal characterization shows a very good agreement between measurements and simulations.**

***Index Terms*—MMIC power amplifier, HBT, GaAs, Wi-Fi 6**

I. Introduction

Wi-Fi 6, also known as 802.11ax, is the latest generation of wireless networking technology, designed to improve speed, capacity, and efficiency for modern devices connected to the Internet. In comparison to previous standards, it introduces several key innovations that address the growing demand for faster and more reliable wireless connections in environments with dense device usage. Orthogonal Frequency Division Multiple Access (OFDMA) and MU-MIMO (Multi-User, Multiple Input, Multiple Output) allow multiple devices to communicate with a router at the same time, while 1024-QAM and wider channels enable higher data rates, achieving an overall improvement in network efficiency [1].

With the introduction of higher-order modulation schemes, the Error Vector Magnitude (EVM) becomes particularly critical, posing very stringent linearity requirements for the power amplifier (PA) in the transmitter chain [2]. A major player in determining the linearity performance of a PA is the technology: the aim of this work is to evaluate the potential of the H20U-C4 GaAs HBT technology from WIN Semiconductors for the development of efficient and linear high-power amplifiers for Wi-Fi 6 applications in the 5-6 GHz band. A relatively simple architecture (corporate PA) has been designed, conceived to achieve 3 to 4 watts of output power and optimized for linearity and efficiency performance, but without adopting any specific linearity enhancement technique, so as to assess the intrinsic capabilities of the technology.

The designed amplifier shows in simulation a saturated output power in excess of 35 dBm with an associated gain and efficiency above 27 dB and 36 %, respectively, while the small-signal gain is above 30 dB. Moreover, the expected PA performance under modulated signal excitation was obtained from continuous-wave (CW) power sweeps by using the method in [3], which allows to estimate the static EVM. At -26 dB of EVM (MCS0 standard) the best efficiency simulated was 17 %, with an associated output power of 29 dBm, while at the lowest tested EVM of -47 dB (MCS11 standard) the simulated output power and efficiency are 18.7 dBm and 1.3 %, respectively. The MMIC has been fabricated and measured under small-signal conditions, showing very good agreement between measurements and simulations. The assembly on carriers, which will allow for proper thermal management under large-signal conditions, is still on-going.

II. PA Architecture

The adopted WIN Semiconductors' H20U-C4 process is a 5 V InGaP/GaAs HBT MMIC technology that already proved a very good linearity-efficiency trade-off up to 5 GHz [4], [5]. In order to evaluate the capabilities of this technology in terms of power, linearity and efficiency at higher frequency (up to 6 GHz), a standard corporate architecture is selected, optimized to achieve the best power, linearity and efficiency trade-off, but avoiding the adoption of advanced linearity enhancement technique, either at bias-, circuit- or system-level.

The PA architecture is shown in Fig. 1. The final and driver stages are composed of, respectively, 4 and 2 power cells, each containing 4 identical transistors. Each driver's cell feeds 2 cells of the final stage, yielding a symmetrical structure. To enhance gain, a third stage is then added adopting a single-transistor cell.

The power cell was designed first. It contains 4 HBT devices, each with 3 μm emitter width, 40 μm emitter length,

and 4 emitter fingers, for a total emitter area of 1920 μm^2. The adopted HBT size is the largest option provided by the foundry, and the device is intrinsically thermally stable by design (layout/parasitic optimized by the foundry). The cell was carefully optimized to be also thermally and RF stable through the use of proper DC and AC base ballast resistors and capacitors [6], while shunt resistors between adjacent base lines guarantee odd-mode stability. The large-signal characterization results on the cell alone under optimized loading conditions showed up to 30 dBm of output power at 5.5 GHz. These results were in very good agreement with the cell macro-model adopted for the PA design, consisting in circuit-level HBT models and electromagnetically-simulated input and output combining structures. As can be seen in Fig. 1, the power cell is designed to be symmetric, an important feature considering the target frequency close to the technology limits. The 1-HBT cell adopted in the pre-driver stage is obtained as a cut-out of the 4-HBT cell, i.e., adopting the same base components.

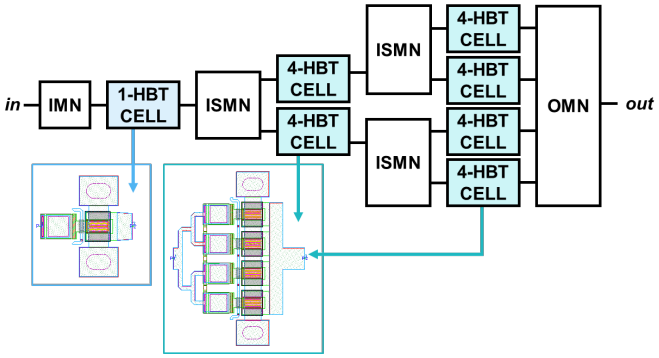

Fig. 1. Architecture of the corporate PA.

Constant-voltage bias approach was adopted, akin to FET-based design. According to HBT sample measurement results, this approach ensures a higher efficiency for the same linearity, with respect to constant-current bias. Moreover, this approach allows to assess the intrinsic linearity of the technology, while linearity improvements through active biasing techniques will be evaluated in the future [7]. All stages are biased in shallow class-AB condition, adopting the same nominal base voltage $V_{BB} = 1.351$ V for all stages, which gives, with 5 V collector's supply, a quiescent current density around 10 kA/cm^2.

From load-pull simulations, an optimum load of $(9 - j2)\,\Omega$ PA was identified for the power cells of the final stages as the best trade-off between peak PAE and output power, slightly favoring the latter to target a minimum of 3 W with 4 cells. Moreover, harmonic tuning indicates that for optimum performance the cell should be loaded at the second and third harmonics with a short and and open circuit, respectively. Semi-lumped matching networks have been adopted, exploiting integrated capacitors but replacing lumped inductors with meandered transmission lines to limit losses.

For the driver stage, a load with twice the real part was instead considered to favor linearity, while the 1-HBT cell,

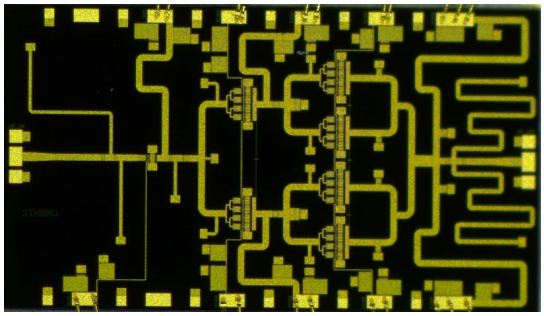

Fig. 2. Microscope picture of the PA: chip size is 4.4 mm x 2.5 mm.

added for gain, provides the required performance on a purely real 50 Ω load. Again a shorted second harmonic and an open-ended third harmonic loads give the best results. To properly account for the large variation of the final stage input impedance variation with power, the inter-stage matching network was optimized adopting a look-up-table-based active load. The optimization target was then to achieve a good match at all power levels of interest, considering back-off operation for linearity enhancement. A semi-lumped approach was followed also for the inter-stage networks as well as for the input matching one. The fabricated PA is shown in Fig. 2: the horizontal size was fixed in this foundry run by other MMICs, thus, as can be noticed, the input stage is not optimized for chip compactness.

III. Simulation Results

The large-signal simulation results are reported in Figs. 3 and 4. The saturated output power, at around 3 dB of gain compression, is above 35 dBm across the whole band. The gain and PAE are greater than 27 dB and 36 %, respectively, while the small-signal gain is above 30 dB. These results compare very well against the literature [8]–[12].

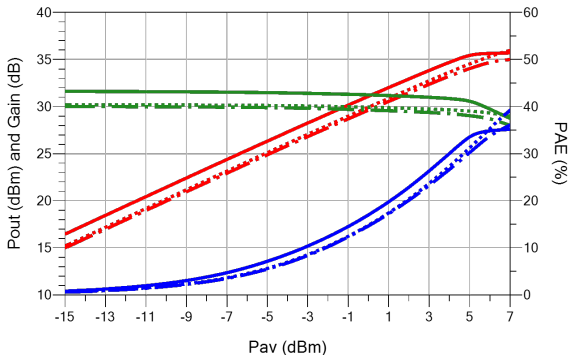

Fig. 3. CW power-sweep simulation results: output power (red), gain (green) and PAE (blue) at 5 GHz (solid), 5.5 GHz (dot) and 6 GHz (dash dot).

As the efficiency-linearity trade-off is a key point for Wi-Fi 6 applications, a practical approach to rapidly evaluate the linearity of the PA in simulation is useful, allowing for network optimization. For this purpose, the approach proposed in [3] was adopted. Starting from the simulated CW features,

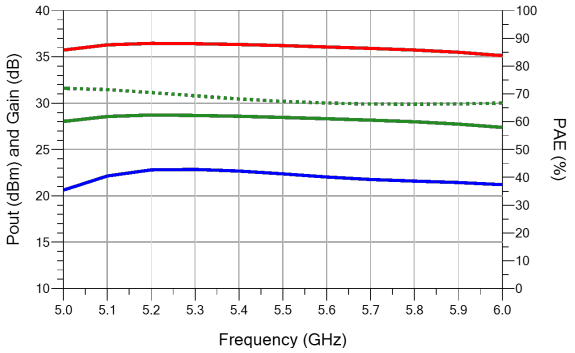

Fig. 4. Large-signal CW simulation results: output power (red), gain (green, dashed curve represents the small-signal gain) and PAE (blue) in the 5-6 GHz range.

the linearity data to be used for networks refinement were computed applying the different digital modulations schemes. It is to highlight that this approach cannot account for memory effects, thus only the static EVM data is available, which is however considered a reliable figure of merit for PA linearity optimization purposes.

Fig. 5 reports the simulation results. The best results achievable at the nominal bias are shown in green, while adjusting the base bias voltage of the final stage, an efficiency improvement can be obtained, at least in the -30 dB to -20 dB EVM range. In particular, at -26 dB EVM, as required by the MCS0 standard, a 17 % PAE can be obtained with bias tuning at an output power level of 29 dBm, while at -30 dB EVM (MCS7) 10 % PAE is achieved, which can both be considered promising simulation results [10], [13]. Clearly, without any advanced linearization technique, at lower EVM levels the efficiency penalty becomes too high. For example, at -47 dB EVM (MCS11 standard), even if the simulated output power is as high as 18.7 dBm, the associated PAE is only 1.3 %.

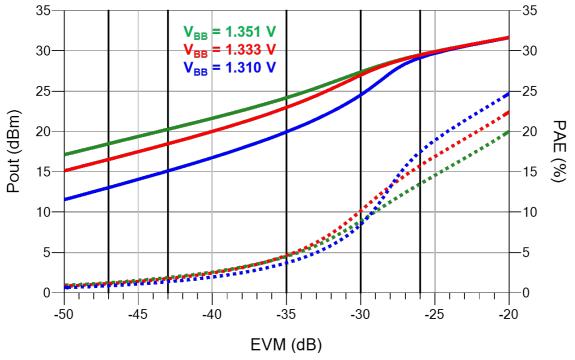

Fig. 5. Modulated-signal simulation results: output power (solid) and PAE (dash) versus EVM at three different final-stage bias.

IV. Experimental Results

The MMIC PA has been manufactured and characterized in the small signal regime showing promising results. The large-signal characterization however requires proper assembly on a test jig, specifically designed for high thermal efficiency to avoid the detrimental effects of HBT overheating. The in-jig small signal characterization results are reported in Fig. 6, showing very good agreement with simulations, and 25 dB gain in the operating bandwidth. Large signal characterization is still on-going.

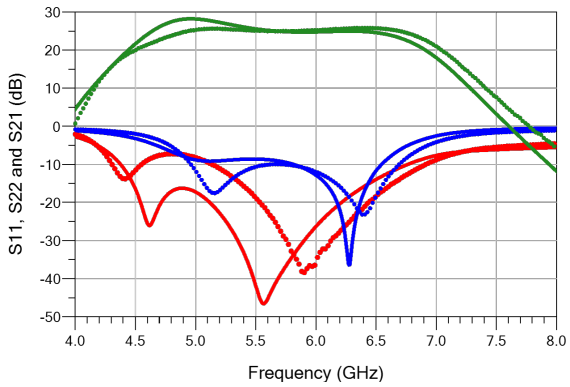

Fig. 6. S-parameters measurements (symbol) compared to simulations (solid): S_{11} (red), S_{22} (blue) and S_{21} (green).

V. Conclusions

This work presented the design and preliminary characterization of a 3.5 W MMIC power amplifier, implemented using GaAs HBT technology, conceived for Wi-Fi 6 applications in the 5-6 GHz range. A 3-stage corporate architecture has been chosen to evaluate the technology's capabilities in terms of power, linearity and efficiency. Simulations show excellent performance, with a saturated output power exceeding 35 dBm, a gain above 27 dB, and efficiency greater than 36 %. Furthermore, through simple bias tuning, an efficiency of 17 % was obtained at -26 dB of EVM, with an associated output power of 29 dBm. Small signal characterization has demonstrated a very good agreement between measurements and simulations, confirming the effectiveness of the proposed design.

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