Load/Source-Pull Evaluation of Modulated Performance in GaAs HBT Power Cells for WiFi-6

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***Abstract*—This work establishes a methodology based on continuous-wave load-pull data in order to estimate modulated figures of merit for radio-frequency transistors. By automatically accounting for source termination effects without any measurement overhead, the technique allows to fully explore the intrinsic trade-offs between linearity, gain, output power and power added efficiency. The approach is used to experimentally analyze three different layouts of gallium arsenide (GaAs) Heterojunction Bipolar Transistor (HBT) power cells for Wi-Fi 6 applications.**

***Index Terms*—Microwave measurement, HBT, GaAs, WiFi-6**

I. Introduction

The last generation of wireless networking standards (Wi-Fi 6, 802.11ax), while delivering unprecedented performance in terms of communication speed [1], imposes challenging requirements for power amplifiers (PAs) within the transmission signal chain. The adopted Orthogonal Frequency Division Multiplexing (OFDM) modulation schemes result in time-domain waveforms with peak-to-average power ratios (PAPR) in excess of 10 dB, for which specific techniques are required to obtain high-efficiency and linear PAs, particularly in the case of dense constellations [2]. These conflicting demands have to be addressed at all stages during the design process, where critical optimizations can be implemented already at transistor level [3].

In this work, three custom gallium arsenide (GaAs) Heterojunction Bipolar Transistor (HBT) power cells, implemented in the H20U-C4 process from WIN Semiconductors, are experimentally analyzed to evaluate their suitability for the realization of WiFi-6 PAs. A methodology is proposed to assess the cells' performance in the final circuit when excited with application-like modulated test signals [4], providing a comprehensive evaluation of their linearity and efficiency. Using standard continuous wave (CW) load-pull (LP) data, multiple relevant source and load impedances are tested, allowing to explore trade-offs between linearity, output power, gain, and power added efficiency (PAE), and highlighting the relative advantages of each design.

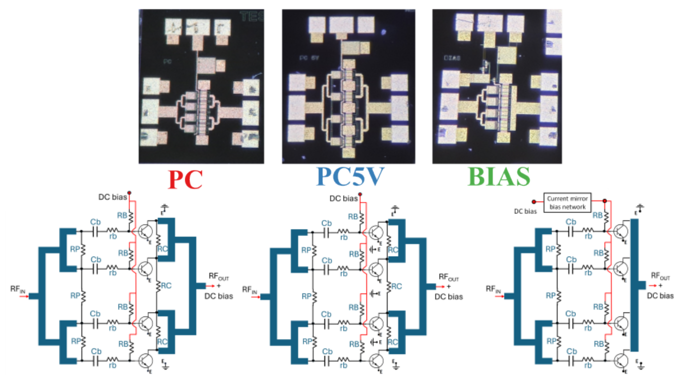

Fig. 1. Photographs and schematics of the three power cells.

II. Design of the HBT Power Cells

The photographs of the power cells (referred as "PC", "PC5V" and "BIAS", respectively) and the corresponding schematics are shown in Fig. 1. The cells are implemented by combining four 4-finger 3×40 μm^2 HBT fingers, for a total active periphery of 1920 μm^2, with expected $\sim$30 dBm of saturated output power in the 5-7 GHz frequency range. DC base ballast resistors (R_B) are used to ensure thermal stability of the power cells, while RF ballasting and feedback is implemented with r_b and C_b. All cells include odd-mode stabilization resistances (R_P and R_C). With respect to the standard combined structure in PC, PC5V adds additional ground vias to reduce the effect of source inductances. The BIAS cell, instead, modifies the output combiner structure and includes an additional current mirror bias circuit in the base.

III. Load-pull-based evaluation methodology

Each voltage-biased transistor device-under-test (DUT) is modeled as a quasi-static time-invariant nonlinear 2-port circuit terminated with a linear passive load Γ_L, as depicted

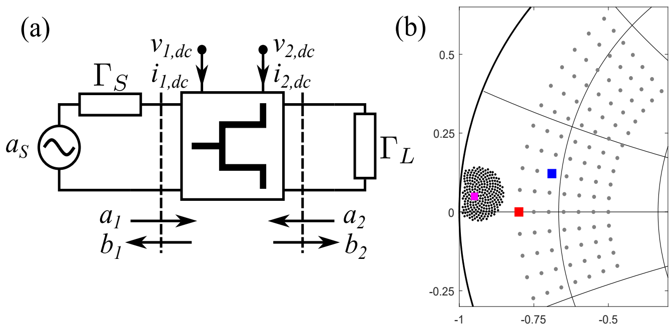

Fig. 2. (a) Schematic of a general LP experimental setup. (b) Smith chart plot for the Γ_S-grid (black), $\Gamma_S = -0.95 + j0.05$ (magenta), the Γ_L grid (grey), the maximum PAE load ($\Gamma_L = -0.69 + j0.12$, blue), the maximum P_{out} load ($\Gamma_L = -0.8$, red) in CW LP for the PC5V cell at 6 GHz.

in Fig. 2a. In this way, neglecting harmonic components and terminations, the constitutive equations read

$$b_1 = f_1(|a_1|, \Gamma_L)a_1 \qquad b_2 = f_2(|a_1|, \Gamma_L)a_1 \tag{1}$$
$$i_{1,dc} = g_1(|a_1|, \Gamma_L) \qquad i_{2,dc} = g_2(|a_1|, \Gamma_L)$$

where a_k, b_k are the incident and reflected power waves at the fundamental frequency, and $i_{k,dc}$ is the dc component of the current, each respectively at each at port $k = 1, 2$ [5]. The functions in (1) are typically extracted from vector LP experiments, where the magnitude of a_1 and Γ_L are swept independently to capture all the variables needed to provide the relevant figures-of-merit (FoMs) for the DUT. This test is often performed using a source generator with a 50-Ω impedance ($\Gamma_S = 0$), as the source impedance does not appear in any form in (1) and, therefore, does not impact most of the relevant metrics of interest for the DUT.

Results for any source termination $\Gamma_S \neq 0$ do not require additional measurements and can be obtained by suitably post-processing the standard LP data [6]. In general, any linear source can be represented as

$$a_1 = a_S + \Gamma_S b_1 \Longrightarrow a_S = a_1 - \Gamma_S f_1(|a_1|, \Gamma_L). \tag{2}$$

The a_1, b_1 and Γ_L values known from a LP experiment at $\Gamma_S = 0$ can be used in (2) to derive the "virtual" excitation a_S that would result in the exact same DUT waves, for any user-prescribed $\Gamma_S \neq 0$. Moreover, (2) can be inverted to provide a_1 as a function of a_S, Γ_S and Γ_L: $a_1 = h(|a_s|, \Gamma_s, \Gamma_L)a_s$, which can then be substituted in (1) to obtain all the other waves. This elaboration strategy allows to derive the behavior of the DUT for general Γ_S-Γ_L terminations, such as those imposed by the matching network of the final PA. The following FoMs can then be defined:

$$P_{av,S} = \frac{|a_S|^2}{2(1 - |\Gamma_S|^2)|} \qquad P_{out} = \frac{1}{2}|b_2|^2 - \frac{1}{2}|a_2|^2 \tag{3}$$
$$G_T = \frac{P_{out}}{P_{av,S}} \qquad PAE = \frac{P_{out} - P_{av,S}}{v_{1,dc}i_{1,dc} + v_{2,dc}i_{2,dc}}.$$

The post-processing of LP data by assuming a specific Γ_S is necessary for the correct evaluation of linearity, which is

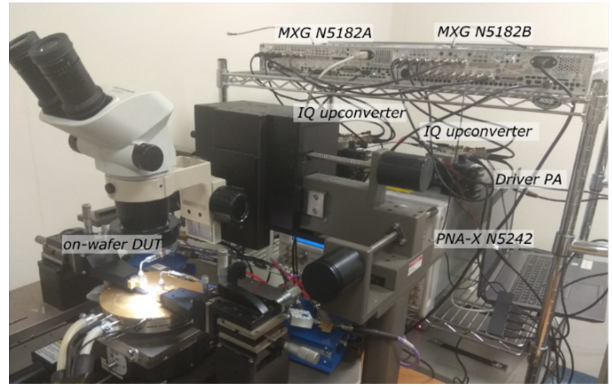

Fig. 3. The on-wafer active load-pull measurement setup used in this work.

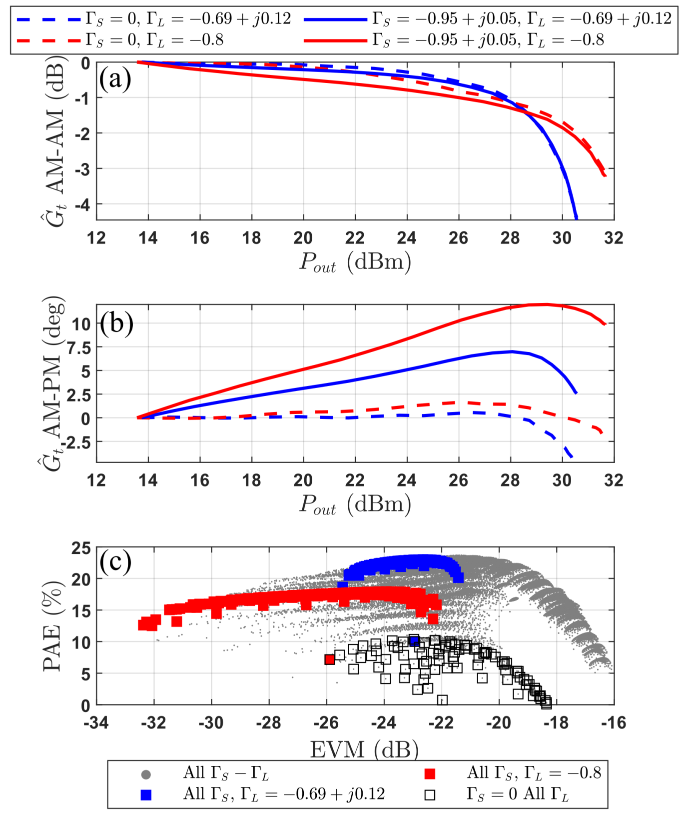

Fig. 4. (a) AM-AM and (b) AM-PM characteristics for the CW complex transducer gain $\hat{G}_T$ of the PC5V cell for $\Gamma_S = -0.95 + j0.05$ (line) and $\Gamma_S = 0$ (dash) and the maximum PAE Γ_L (blue) and maximum P_{out} Γ_L (red). (c) Modulated PAE and EVM results for the PC5V transistors for all the examined $\Gamma_S - \Gamma_L$ combinations (grey), for the maximum PAE Γ_L (blue), for the maximum P_{out} Γ_L (red) and for $\Gamma_S = 0$ (black squares).

strongly dependent on the input termination [6]. The nonlinear distortion introduced by the DUT within the final circuit is computed on the observed output b_2 (or equivalently a_2) for a given input a_S. This can be quantified using the AM-AM and AM-PM characteristics of the DUT complex transducer gain $\hat{G}_T = \frac{b_2}{a_S}$ for specific Γ_S-Γ_L conditions [6], which are generally different from the distortion between the b_2- and a_1-waves, due to the nonlinearity in (2).

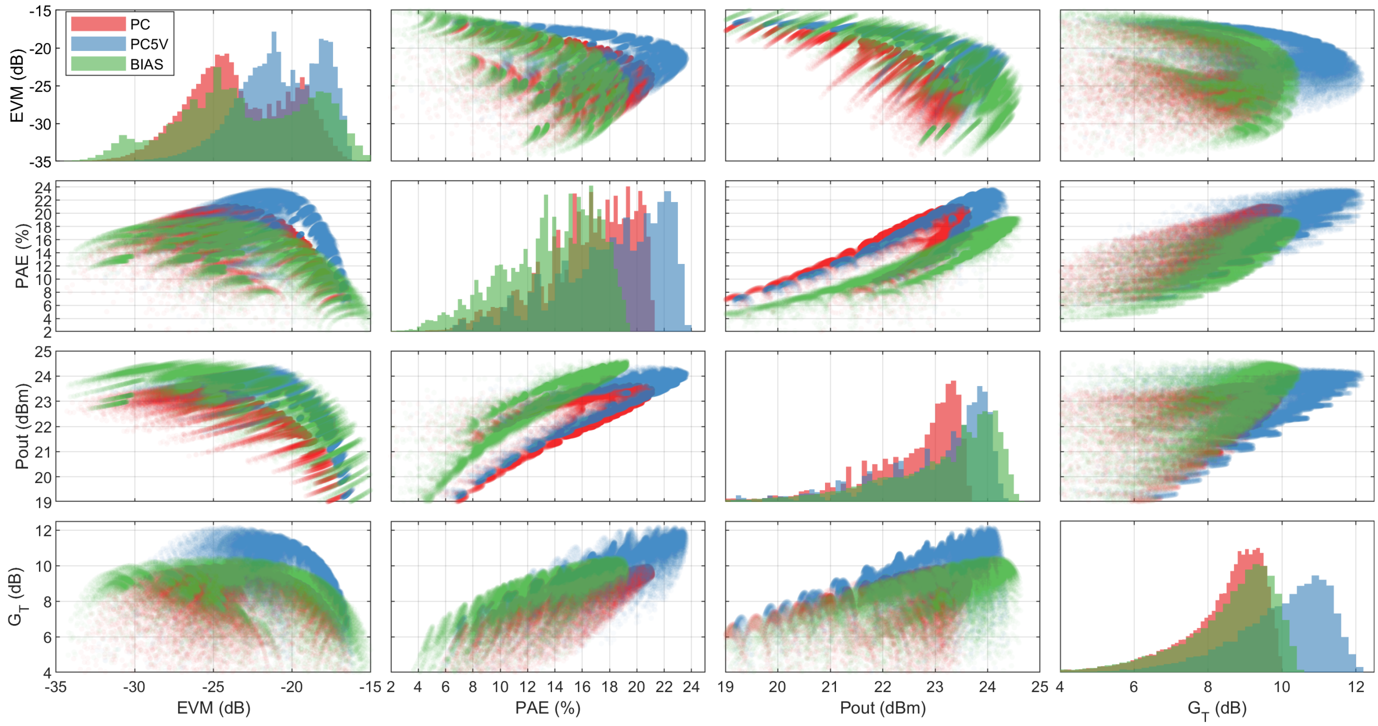

Fig. 5. Scatter matrix plots for the PC (red), PC5V (blue) and BIAS (green) cells for the EVM-PAE-Pout-GT trade-offs. Each data point represents, for a given Γ_S-Γ_L choice, the value of the respective metric for the DUT excited by a full-swing random-phase multi-sine with PAPR=10.1 dB. The X-Y intersection plots represent the metric X as a function of metric Y, while X-X plots on the diagonal represent the overall distribution of the values of variable X.

The CW operating characteristics in a specific Γ_S-Γ_L environment can also be used to estimate FoMs in modulated conditions by superimposing a specific modulated signal to a_S and by examining the resulting envelopes for the variables in (1) [4], [7]. The use of this quasi-stationary approach neglects any memory effect in DUT, but avoids the use a of a significantly more complex wideband setup for characterization [4]. In this case, the FoMs in (3) are derived as suitable statistical or time-averages of the corresponding CW quantities. Moreover, all the linearity FoMs dictated by the waveform standards can be directly computed. For example, EVM can be derived as [4], [7]

$$\mathrm{EVM} = \frac{\int |b_2(t) - G \cdot a_S(t)|^2 dt}{\int |b_2(t)|^2 dt}, \tag{4}$$

where G is the statistical average of the DUT complex transducer gain. While different input signal levels can be tested to examine performance in back-off conditions, in this work we derive each modulated FoM at “full-scale”, where the peak of the $a_S(t)$ waveform corresponds to the peak power at which the CW LP data is derived.

This methodology allows to directly map CW load-pull measurements into application-relevant modulated metrics for a given transistor, allowing for a thorough evaluation of different solutions across all the possible $\Gamma_S - \Gamma_L$ choices.

IV. Experimental Results

For the three cells, a fundamental-only LP characterization is performed at a frequency of 6 GHz using the on-wafer active setup reported in [4] and shown in Fig. 3. The quiescent point is selected as $V_C = 5$ V and $J_C = 10$ kA/cm^2 and the DUTs are kept at a fixed baseplate temperature $T_b = 30$ °C. The load grid for the LP measurements and the source grid used for the data post-processing are reported in Fig. 2b, along with the maximum P_{out} and PAE loads for the PC5V cell. The modulated signal used as excitation is a full-swing 10^4-tones multi-sine with PAPR = 10.1 dB, which can be considered as a suitable approximation for other complex-gaussian envelopes such as Wi-Fi 6 OFDM waveforms [1], [4].

Figures 4a-b report the CW $\hat{G}_T$ AM-AM and AM-PM curves for the PC5V cell for selected values of Γ_S (maximum Pout and maximum PAE in CW conditions) and Γ_S (0 and $\Gamma_S = -0.95 + j0.05$), highlighting how the source termination strongly impacts the overall circuit linearity, particularly regarding the phase distortion characteristics. PAE and EVM for the same device in modulated conditions are reported in Fig. 4c for all the tested $\Gamma_S - \Gamma_L$ combinations. The use of synthetic modulated conditions for the DUT allows to better reflect the device achievable performance in the final application. For example, it can be observed how the maximum CW PAE Γ_L is not the one providing the maximum PAE in modulated operation due to the back-offed conditions, while also featuring a sub-optimal PAE-EVM trade-off with respect to the whole ensemble. A multi-dimensional scatter plot is reported in Fig. 5, comparing the G_T-P_{out}-PAE-EVM trade-offs among the three cells. The PC5V cell is able to provide the highest overall gain (~12 dB) and PAE (~23%)

in modulated conditions, while the BIAS cell provides the highest output power (~ 24.5 dBm). It can also be observed from the PAE-vs-EVM data how the PC5V cell offers the best linearity-efficiency trade-off at high EVM values (> -25 dB), the PC cell at intermediate ones (< -25 dB and > -30 dB), and the BIAS cell for low ones (< -30 dB).

V. Conclusions

A methodology based on source termination post-processed CW LP data has been used to evaluate the expected performance in modulated condition of three HBT cells for Wi-Fi 6 applications in the 6 GHz band. The technique allows to thoroughly analyze how the trade-offs between EVM, output power, gain and PAE are affected by the different examined topologies.

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