Digital OTA with Floating-Inverter Input Stage and Isolation Resistor-Based Frequency Compensation for Ultra-Low Power CT- Modulators

Digital OTA with Floating-Inverter Input Stage and Isolation Resistor-Based Frequency Compensation for Ultra-Low Power CT-$\Sigma\Delta$ Modulators

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***Abstract*—This paper presents a fully differential floating-inverter-input digital operational-transconductance-amplifier (FI-DIGOTA) featuring isolation resistor-based frequency compensation. The proposed FI-DIGOTA achieves a DC gain of 59.2 dB, a gain-bandwidth product (GBP) of 50 kHz, and a phase margin (PM) of 47.5° while operating at an ultra-low (UL) supply voltage of 0.4 V. The power consumption of the proposed FI-DIGOTA is 7 nW, making it well-suited for energy-constrained applications. A first-order continuous-time $\Delta\Sigma$ (CT-$\Delta\Sigma$) modulator utilizing an integrator based on the proposed FI-DIGOTA is proposed as an application example and achieves a signal-to-noise-and-distortion ratio (SNDR) of 44 dB, a spurious-free dynamic range (SFDR) of 55.18 dB, and an effective number of bits (ENOB) of 7.016 bit over a 500 Hz bandwidth at 100 oversampling ratio (OSR).**

***Index Terms*—Digital-Based Operational Transconductance Amplifier (DIGOTA), Floating-inverter (FI), Isolation resistor-based frequency compensation (R_{iso}-based) technique, $\Delta\Sigma$ modulator, UL-power (sub-10 nW).**

I. Introduction

Energy-autonomous sensor nodes and wearables for emerging Internet of Things (IoT) applications demand low-cost integrated circuits with ultra-low power consumption (nW range), operation at ultra-low supply voltage (ULV), well below 1 V, and tiny physical dimensions (sub-mm scale). Aiming to meet such stringent requirements, digital-based and digital-intensive analog and mixed-signal blocks are actively being explored in the last years [1].

In this context, digital operational transconductance amplifiers (DIGOTAs) [2]–[11] are compatible with a low effort digital design flow, have demonstrated operation down to 0.3 V with a power consumption down to the sub-nW range [4] and a high energy efficiency, thanks to the suppression of static power consumption related to their inherently digital operation. At the same time, DIGOTAs suffer of limitations in their frequency response (e.g., limited gain-bandwidth product (GBW)), in linearity, and often require a relatively large output capacitor. Although these aspects have been partially addressed in other works [3]–[5], [11], more effort is needed to fill the gap with traditional analog solutions.

This paper presents the novel Floating-Inverter-based DIGOTA (FI-DIGOTA) topology, featuring a highly efficient floating-inverter (FI) input stage and isolation resistor-based frequency compensation to enhance its frequency response, and explores its application in the integrator of a first-order (CT-$\Sigma\Delta$) modulator.

Compared to previous DIGOTAs [1]–[6], [10]–[14], the proposed FI-DIGOTA effectively addresses several weaknesses of existing approaches, including frequency response limitations, inefficiencies in the Muller-C input stage and large integrated output capacitor.

The remainder of the paper is structured as follows. Sect. II introduces the proposed FI-DIGOTA topology, Sect. III covers circuit design and implementation, while Sect. IV presents simulation results and evaluates performance metrics. Moreover, Sect. V demonstrates the integration of the FI-DIGOTA into a first-order CT-$\Sigma\Delta$ modulator, while Sect. VI concludes the paper.

II. The FI-DIGOTA Topology

The architecture of the proposed Floating-Inverter-based DIGOTA (FI-DIGOTA) is illustrated in Fig. 1. This circuit consists of four primary blocks: an input stage based on a floating inverter amplifier (FIA) input stage, an inverter chain, which digitizes the FIA outputs, a common mode compensation (CMC) block, and a differential output stage. The input stage consists of two FIAs, which are dynamically biased by the CMC block to sense the differential input voltage rejecting its common-mode component, as in previous DIGOTAs [2]–[6], [12], [13], taking advantage of the inherent energy efficiency of the FIAs [9], [15].

In details, the CMC block drives the transistors $M_{\rm p}$ and $M_{\rm n}$ to connect the sources of the PMOS (NMOS) devices of the input FIAs to supply (ground) when the digital outputs INV+ and INV- of the inverter chain are 0,0 (1,1), (see Fig. 1(b)), as requested to dynamically bias the FIA to charge (discharge) the parasitic output capacitance of the FIA ($C_{\rm p}$).

As in previous DIGOTAs, when the digital outputs INV+ and INV- of the inverter chain are 1,0 (0,1) the differential output stage is operated to increase (decrease) the output differential voltage (see $I_{\rm OUT}$ and Outp-DIG in Fig. 1(b)).

Compared to previous DB-OTAs and DIGOTAs, the proposed FIA-based input stage further enhances energy effi-

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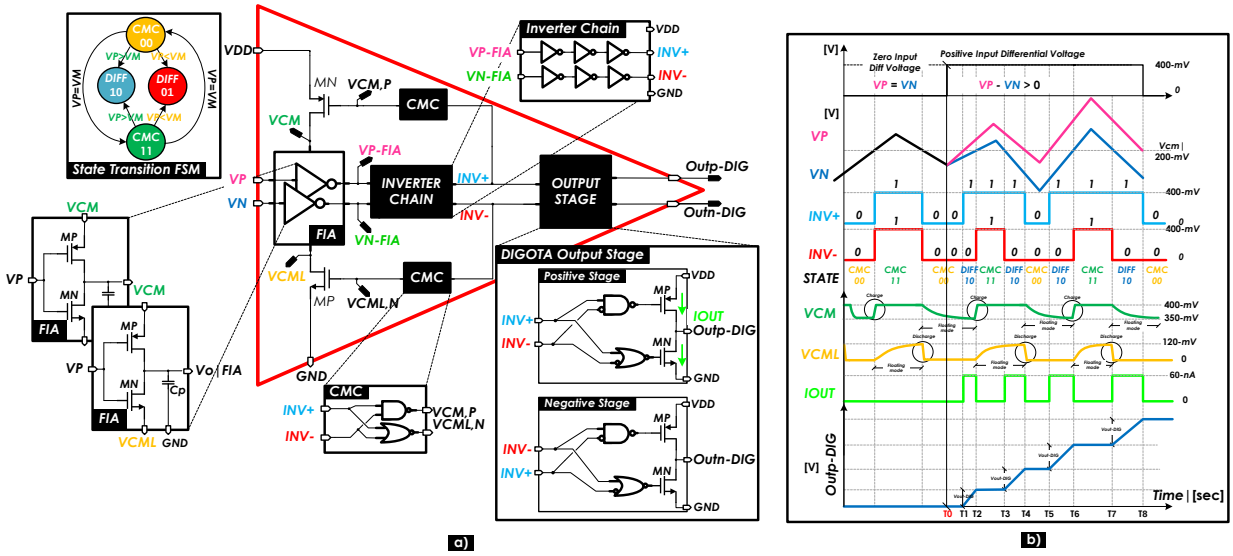

Fig. 1: a) Finite-State-Machine transition diagram and FIA-based DIGOTA block diagram, b) Waveforms of input/output of each block for zero and positive input differential voltage.

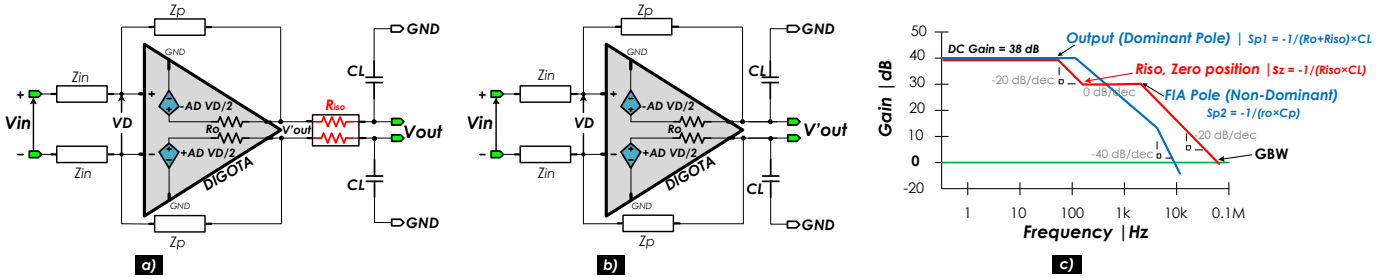

Fig. 2: Impact of the attenuation resistor (Riso) on close-loop gain frequency of voltage follower configuration.

ciency, since the input transistors are dynamically operated most of the time close to their threshold voltage, where they achieve the highest transconductance efficiency g_m/I_{DD} [15], and the same charge from the power supply is reused by the PMOS and NMOS transistors, which both contribute to the output differential current [16]. In addition, the FIA architecture inherently provides a wide common-mode input range.

A. Isolation Resistor-Based Frequency Compensation

Similarly to the DIGOTA analyzed in [8], the fully-differential FI-DIGOTA presented in this paper exhibits a two-pole open-loop gain transfer function (see Fig. 2). The dominant pole of the output stage, $s_{p1} = -1/R_O C_L$ is related to the equivalent output resistance R_O and to C_L, which is introduced to reconstruct the analog output from the pulsed current injected by the output stage. As in [2]–[6], [8], [12], dominant-pole frequency compensation can be achieved designing C_L so that $|s_{p1}| \leq |s_{p2}/A_{D0}|$, where s_{p2} is the first non-dominant pole, and A_{D0} denotes the DC gain. This ensures a phase margin (PM) of more than 45° under any resistive feedback configuration. However, this approach requires a large C_L [2]–[6], [11], limits the GBW to be less than $|s_{p2}|/2\pi$ and degrades the slew rate. Aiming to mitigate these limitations, the isolation resistor-based frequency compensation scheme [17] illustrated in Fig. 2 is utilized in the FI-DIGOTA presented in this paper. In details, a resistor (R_{iso}) is connected in series to (C_L) to introduce a zero in the loop gain transfer function, which now takes the form:

$$\frac{V'_{out}(s)}{V_D(s)} = \frac{A_{D0} \cdot (1 + s \cdot R_{iso} \cdot C_L)}{(1 + s \cdot (R_O + R_{iso}) \cdot C_L) \cdot (1 + s \cdot r_O C_p)} \quad (1)$$

Thanks to the zero related to R_{iso}, the PM is improved without significant GBW degradation, as verified in the next section. Moreover, taking the output V_{out} across C_L, the zero introduced by R_{iso} is canceled by the pole $s_{p3} = -1/R_{iso}C_L$ of the $R_{iso}C_L$ passive filter, with no impact on the external transfer function besides the increase of the closed-loop output resistance and a minor shift of the dominant pole to lower frequencies, which is almost negligible for $R_O \ll R_{iso}$. This analysis clearly reveals how the introduction of the isolation resistor in the FI-DIGOTA circuit overcomes the inherent limitations in the DIGOTA frequency response resulting from the low-frequency pole due to the large output capacitance required for analog output reconstruction.

III. Simulation Results

The proposed FI-DIGOTA has been designed and simulated in 180 nm CMOS at 400 mV supply voltage. The simulated power consumption is just 7 nW and the other performance is discussed in this Section.

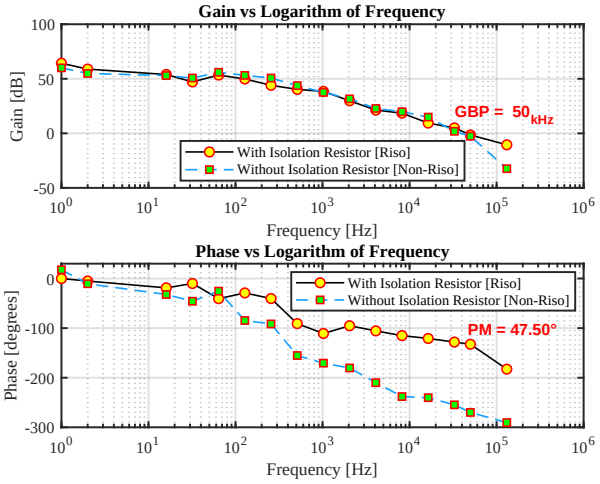

Fig. 3: Frequency response of the proposed FI-DIGOTA with and without isolation resistor-based compensation.

A. Frequency Response and Slew Rate

The open-loop frequency response of the FI-DIGOTA with (without) $R_{\rm iso}$ has been simulated based on transient analysis as in [6], and is reported in Fig. 3. The figure reveals that the DC gain and the GBW product are 59.2 dB and 50 kHz, respectively, and are almost not affected by R_{iso}. On the other hand, while the circuit without R_{iso} is unstable in the unity gain feedback configuration. The introduction of R_{iso} stabilizes its operation and guarantees a PM of $47.5°$ in unity-gain feedback. It is worth observing that the frequency response of the circuit without $R_{\rm iso}$, which is unstable in a unity gain feedback configuration, has been inferred by simulating the circuit in a configuration with a feedback factor $\beta = |Z_{\rm IN}/(Z_{IN} + Z_P)| = 1/51$, to avoid instability, where $Z_{\rm IN}$ and $Z_{\rm P}$ are defined in Fig. 2). To achieve the same PM by dominant the pole compensation adopted in other DIGOTAs [2]–[7], [12], a 100X larger C_L would be needed, with a 100X reduction in GBW and slew rate.

Since the power consumption of the FI-DIGOTA is 7 nW and the slew rate is 0.075 V/μs, the proposed FI-DIGOTA achieves competitive simulated small-signal and large-signal Figures of Merit (FOM_S, FOM_L, defined in Table. I) of 57.14 (MHz·pF/nW) and 107.14 ((V·pF)/(μs·nW)), respectively

B. Amplitude Characterization and THD

The total harmonic distortion (THD) of the FI-DIGOTA with R_{iso} in unity gain feedback configuration with a 10 Hz differential sine wave input V_{iD} is reported in Fig. 4. The simulated THD is below 1% (0.3%) for differential input amplitudes V_{iD} ranging from 10 mV to 400 mV (from 20 mV to 370 mV). The THD increases at very low amplitudes as in other DIGOTAs due to the inherent dead-zone nonlinearity [2]–[4], [6]. Despite that, the proposed FI-DIGOTA achieves better linearity compared to other DIGOTAs [2]–[6], [12], [13], [18]–[20] (see Table. I) thanks to its fully differential architecture and its FI-based input stage.

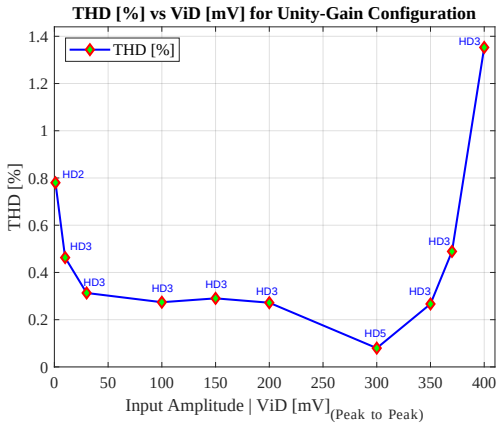

Fig. 4: THD of the FI-DIGOTA in unity-gain feedback under 10-Hz sinewave input vs.input amplitude.

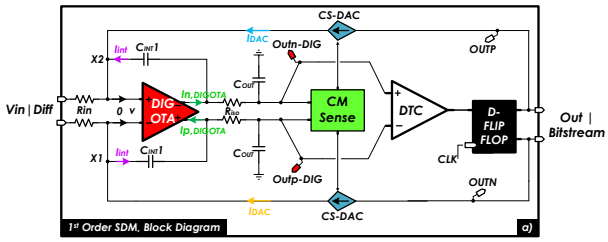

Fig. 5: 1st-order $\Sigma\Delta$ modulator block diagram.

The simulation results reported in this Section are compared with previous DIGOTAs and analog OTAs working at sub-0.4 V supply voltage reported in Tab.I. Based on the table the proposed FI-DIGOTA achieves the lowest THD thanks to the FI-based input stage. Moreover, it achieves the higher GBW and the higher DC gain compared to other DIGOTAs [2]–[6], [12], [13], while properly operating with the lowest output capacitance (10 pF), thus narrowing the gap with traditional analog approaches. The energy efficiency FoML is lower only compared [3], in view of the small C_L of our solution.

IV. FI-DIGOTA Application in a First-Order CT-$\Sigma\Delta$ Modulator

As an application example, proposed FI-DIGOTA has been used in the integrator of a first-order, Continuous-Time (CT-$\Sigma\Delta$ modulator $\Sigma\Delta$M) whose block diagram is illustrated in Fig. 5 and is based on a standard architecture including a one-bit current-steering (CS) DAC with a double-tail comparator (DTC) [9] and a D-flip flop (sampler).

The CT-$\Sigma\Delta$ modulator achieves a peak SNDR of 44 dB at 100 mV input signal within the bandwidth of 500 Hz and an OSR of 100. The SFDR is 55.18 dB and confirms the good linearity performance and low harmonic distortion as shown in Fig. 6. The overall power consumption of the modulator is 17.78 nW. The FI-DIGOTA (7 nW) and the CSt-DAC plus the CM sensing circuit (9.711 nW) account for the majority of the power consumption within the blocks, demonstrating competitive performance compared to the state-of-the-art sub 0.4 V $\Sigma\Delta$ modulators.

TABLE I: Comparison of State-of-the-Art OTAs Works; UL-power and sub-400 mV supply (best in bold).

State-of-art works	**[18]**	**[19]**	**[20]**	**[2]**	**[12]**	**[3]**	**[4]**	**[13]**	**[5]**	**[6]**	**This work**
Validation	Sim.	Meas.	Meas.	Sim.	Sim.	Sim.	Meas.	Meas.	Sim.	Meas.	Sim.
Supply Voltage V_{DD} [V]	0.4	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.4	0.4
Year	2024	2020	2020	2019	2020	2024	2021	2024	2024	2022	2025
OTA architecture	Folded-cascode	Class AB	Class AB	Digital	Digital	Digital	Digital	Class AB	Digital	Digital	Digital
Design	custom	custom	custom	std cell	std cell	std cell	std cell	std cell	std cell	std cell	std cell
Compensation method	Not-required	Nested Miller	Nested Miller	Dominant pole	Dominant pole	Dominant pole	Dominant pole	Nested Miller	Dominant pole	Dominant pole	Isolation Resistor
Phase Margin (PM) [°]	9.9	54.7	53.9/54.2	57	86	-	57.3	52	69	50	47.5
Technology [nm]	180	180	180	180	180	180	180	180	180	180	180
Power (P_{DD}) [nW]	8.03	12.6	13/12.88	7.37	10.5	2.147	**0.407**	1,800,000	4.1	95	7
Current (I_{DD}) [nA]	20.075	42	43.34	24.567	35	7.156	**1.356**	6,000,000	13.67	237.5	17.5
DC gain [dB]	69.14	64.7	**98.4/98.1**	35	22.6	34.3	31	46.2	54.4	35	59.2
GBW [kHz]	26.79	2.96	3.1/3.56	0.47	8	2.823	0.229	**2450**	0.265	-	50
Load C_L [pF]	1	30	30	80	10	150	80	2	150	10	10
SR_{avg} [V/μs]a*	2,200	4,150	**9,200**	0.0005	-	14.5 e-5	264 e-6	2.4	7 e-5	1.26 e-5	0.075
Input referred offset [mV]	-	3.2	3.19/3.1	-	-	-	1.1	-	-	-	5.426
CMRR [dB]	71.6	**110 (1)**	60 (1)	-	-	-	-	-	93	62	52 (4)
PSRR [dB]	**78.14**	50 (1)	61 (1)	-	76.8	-	-	-	63.9	55	50 (4)
THD [%]	1.25	1	0.49 (2)	3	-	1.3	1.26	0.7	0.7	1.8	**0.3 (3)**
FOM_S [(MHz · pF/nW)] b^*	3.34	7.05	7.154	34	7.62	**197.23**	45	2.72e-3	9.7	4.21	57.14
FOM_L [(V/μs) · pF/nW)] c^*	2.74 e+5	**9.88 e+6**	2.12 e+7	20	-	10.1	51.9	2.67e-3	2.56	1.26 e-3	107.14

$$a^*: \ \mathrm{SR_{avg}} = \frac{\mathrm{SR}_{(+)} + \mathrm{SR}_{(-)}}{2}, \quad b^*: \ \mathrm{FOM}_S = \frac{\mathrm{GBW} \cdot C_L}{\mathrm{Power}}, \quad c^*: \ \mathrm{FOM}_L = \frac{\mathrm{SR} \cdot C_L}{\mathrm{Power}} \tag{2}$$

(1) At DC input frequency. (2) At 10-Hz, with $V_{\mathrm{in}|@\mathrm{ac}} = 250$ mV. (3) At 10-Hz, with $V_{\mathrm{in@ac}|\mathrm{PKPK}} = 100$ mV. (4) At 0-Hz, with $V_{\mathrm{in@ac}|\mathrm{PKPK}} = 100$ mV.

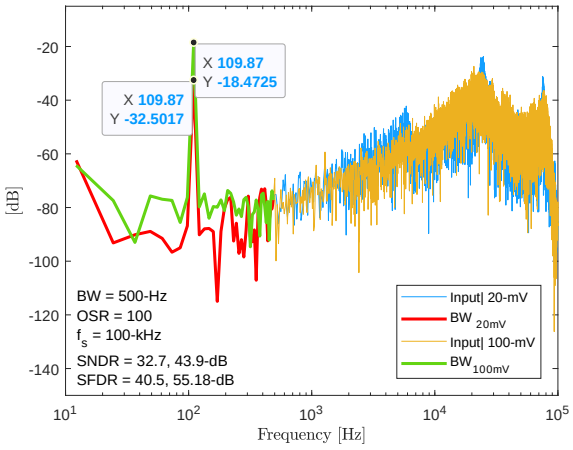

Fig. 6: Frequency spectrum of 1st-order ΣΔ modulator in two different input amplitude (20 mV, 100 mV) within 500 Hz BW.

V. Conclusion

A fully differential FI-DIGOTA with a floating-inverter input stage and isolation-resistor based frequency compensation has been presented. The proposed FI-DIGOTA retains the high energy efficiency typical of DIGOTAs while achieving an improved GBW, enhanced linearity, reduced die area, and better phase margin. A first-order CT-ΣΔ modulator including an integrator based on the proposed FI-DIGOTA is presented as an application example.

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