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Nonlinear Dynamics and Hybrid Synchronization of DC Biased Colpitts Chaotic Oscillators

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Abstract

Chaos-based wireless communication systems can enhance the physical-layer security of IoT devices, but their reliability depends on stable chaotic behavior under real conditions. We investigate a modified Colpitts oscillator with a tunable base bias voltage, introduced as an independent control parameter to flexibly adjust nonlinear regimes. Using numerical studies, SPICE simulations, and hardware experiments, we show that simplified numerical models predict only a DC offset shift, whereas realistic implementations reveal qualitative changes in the dynamics, highlighting the need for experimental validation. We further demonstrate hybrid synchronization between the analog oscillator and an FPGA-based digital model. Despite model simplifications and non-idealities, synchronization is successfully achieved using the Pecora–Carroll method, showing that preserving the core dynamic structure is more critical than exact waveform replication. These results clarify the constraints of idealized models for predicting dynamical patterns while confirming the robustness of hybrid synchronization for secure, resource-constrained communication systems.

Keywords: Colpitts chaotic oscillator; bifurcations; hybrid synchronization; chaos-based communications; Euler–Cromer numerical integration

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1. Introduction

The adoption of Internet of Things (IoT) devices in various industry sectors brings substantial improvements in energy efficiency, effective resource allocation, the creation of smart environments, and the monitoring of critical infrastructure. The typical IoT architecture includes sensors and/or actuators controlled by an embedded system located in some physical environment, such as soil, water, human body, building, or industrial facility. A node also has a communication module that enables data transfer and remote control. Wireless communications are exploited as many IoT edge modules are implemented in locations with economically unfeasible wiring installation. The choice of wireless communication technology depends on the distance between communicating modules, the amount of information, the required data rate, the available electrical energy, and the existing infrastructure [1,2]. However, wirelessly connected modules are vulnerable to attacks like eavesdropping, node capture, malicious fake node, replay, and timing attacks [3]. So, additional measures must be taken to ensure confidentiality, data integrity, and availability. Unfortunately, in most cases, sensor nodes are constrained in terms of computational power

and energy, and thus cannot implement traditional encryption protocols. To overcome this issue, lightweight cryptography aimed at implementation in IoT is under intensive research and development [4,5]. Additional technology that can enhance the security of IoT networks at the physical level is the deployment of chaos-based communication systems [6].

The chaos phenomenon is observed in nonlinear active electronic circuits producing oscillations. Current and voltage signals in chaotic oscillators are deterministic, governed by a system of nonlinear differential equations, but are characterized by a narrow self-correlation function and a wide spectrum. Also, chaotic systems are extremely sensitive to initial conditions and parameter variations. This means that two electronic circuits built with the same model components may produce different, uncorrelated signals [7]. The unpredictability of chaotic signals makes them a potential candidate for secure communication systems [8]. A vast number of scientific papers are devoted to the development of communication systems that exploit chaos in different ways. In general, chaos-based communication systems can be classified into two main categories: coherent and non-coherent. In a coherent method, the receiver must reproduce the chaotic signal to recover the transmitted message accurately, meaning the transmitter's and receiver's chaos generators must be synchronized to derive identical waveforms. Meanwhile, in non-coherent systems, demodulation is performed based only on processing the received signal without synchronization with the transmitter's chaos generator. Coherent communication techniques offer higher security levels but are sensitive to synchronization issues in noisy channels [9].

Nevertheless, the implementation of chaotic signals in communication systems has remained an active area of research for several decades, yet many challenges still need to be addressed. Researchers have recently proposed various designs of promising chaos-based communication systems using analog and discrete realizations of chaotic oscillators. In [10], the modulation is achieved by changing the numerical integration operator in discrete chaotic maps obtained by the generalized explicit second-order Runge–Kutta solver. The authors experimentally verified the performance of the proposed system, showing high noise immunity and strong confidentiality. The quadrature chaos shift keying (QCSK) communication system, which employs simple, low-cost analog chaotic oscillators, is proposed in [11]. This study outlines the importance of synchronization signal choice to achieve a better BER performance and signifies the need for a threshold-based correction mechanism to compensate for correlation coefficient disparities at higher signal-to-noise ratio (SNR) values. In publications [10,12], a comprehensive characterization of a chaotic oscillator is performed before integrating it into a communication system. Such analysis is mandatory, as different parameters of a real circuit and a mathematical model implemented in a digital device strongly affect the dynamics of an oscillator. For example, results presented in [13] demonstrate that there are regions of periodic behavior for a specific set of capacitor values instead of the expected chaotic mode. Component parameter variations are natural due to production processes, temperature, bias, and other factors. However, they can pose a significant challenge to the practical integration of analog chaotic oscillators in IoT devices. A good option is to place an additional voltage source in an oscillator's circuit to enable dynamics adjustment during the operation, as manual passive component tuning is impractical and time-consuming [13]. Two main reasons exist for incorporating voltage or current sources in chaotic oscillators. The first is the direct current (DC) offset tuning of signals observed in a nonlinear dynamic system, as shown in [14]. The second is the detailed analysis of chaotic oscillators to reveal hidden attractors and multistability, as described in [15,16]. Multistability is another feature that characterizes chaotic oscillators and can either increase potential application areas or introduce new challenges, particularly when transitions between modes of operation are unwanted [17]. Considering the dynamic

behavior of relatively simple chaotic oscillators like Colpitts, it can be concluded that a comprehensive analysis of a chaotic oscillator is needed before its deployment in a communication system. Moreover, synchronization between drive and response chaotic oscillators must be tested for different operating conditions and SNR values, as the coherent detection method strongly depends on synchronization.

Complete synchronization is the easiest way to synchronize two identical electronic oscillators, which was first introduced in [18]. In the literature, it is often called the Pecora–Carroll synchronization method, and a good example of practical realization of this method for the Vilnius oscillator is given in [19]. In addition, other types of synchronization are observed in chaotic systems, like lag, generalized, and phase synchronization [20].

Using simple and cheap analog oscillators is advantageous for IoT edge sensor nodes, as it enables enhanced security for resource-constrained devices. In contrast, gateways—where power and computational resources are less restricted—can use more sophisticated devices like field-programmable gate array (FPGA) and system on a chip (SoC), implementing complex signal processing techniques. On the other hand, using multiple reconfigurable analog oscillators on gateway boards may be challenging in terms of reliability and ease of use. To address these limitations, this work proposes a hybrid synchronization approach that enables coherent, chaos-based communication between digital gateway and sensor nodes employing analog chaotic oscillators. In this article, by hybrid synchronization, the authors understand the complete alignment between the dynamics of analog oscillators and their mathematical model implemented on an FPGA. Synchronization is bidirectional, meaning analog and discrete oscillators can be set as drive (master). The feasibility of this concept was previously demonstrated for the Vilnius and RC oscillators using Euler–Cromer numerical integration methods implemented in fixed-point arithmetic [21]. The obtained results demonstrate a high correlation between signals of synchronized oscillators and the flexibility of discrete models.

In this work, we extend the concept of hybrid synchronization by focusing on the nonlinear dynamics and FPGA-based discrete modeling of a modified Colpitts chaotic oscillator with a tunable base bias. We analyze the impact of component variations—especially capacitors and bias voltages—on the oscillator's behavior through numerical simulations, SPICE-level modeling, and physical hardware testing. A discrete implementation of the oscillator is developed using an Euler–Cromer integration scheme and tested for synchronization with its analog counterpart.

Although the chaotic dynamics of the Colpitts oscillator have been studied for several decades, our work introduces two important new aspects. First, we systematically examine the influence of an independently controlled base bias voltage across three levels of modeling: simplified mathematical equations, SPICE simulations, and hardware experiments. This multi-level comparison shows how idealized models may miss qualitative behaviors that appear in real circuits, which has not been addressed in earlier works. Second, we demonstrate hybrid synchronization for the first time between a biased analog Colpitts oscillator and its FPGA-based digital counterpart. This highlights not only the theoretical properties of chaos but also its practical applicability in resource-constrained secure communication systems. Thus, the contribution lies in the combination of tunable bias control, model-to-hardware comparison, and hybrid synchronization, which together extend beyond prior studies of Colpitts oscillators.

The structure of the article is as follows: Section 2 introduces the Colpitts chaotic oscillator and presents the mathematical model, including the effect of bias voltage tuning. Section 3 provides a detailed numerical study, including bifurcation analysis and parameter sensitivity. Section 4 describes the analog implementation using SPICE simulations and hardware prototyping. Section 5 presents the digital implementation and fixed-point

modeling on an FPGA. Section 6 evaluates the hybrid synchronization between analog and discrete realizations. Finally, Section 7 discusses the results and their implications and outlines potential directions for future work.

2. Colpitts Chaotic Oscillator

2.1. Circuit and Mathematical Model

Commonly employed for radio frequency (RF) signal generation, the Colpitts oscillator exhibits chaotic behavior under certain component values [11,22,23]. The schematic of a Colpitts oscillator demonstrating chaotic dynamics is shown in Figure 1. This oscillator consists of a bipolar junction transistor (BJT) Q_1 operating in its active region, along with an inductance and a capacitive divider, formed by C_1 and C_2 and providing positive feedback to sustain oscillations. The inductor L_1, in series with its internal resistance R_L, together with a bias resistor R_1, completes the circuit loop. The DC supply voltages V_1 and V_2 provide proper biasing for the transistor.

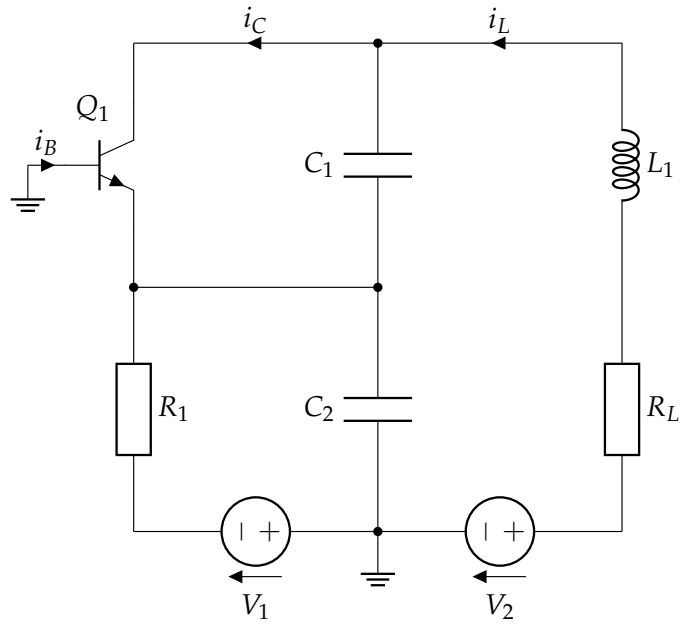


Figure 1. Schematic of the Colpitts chaotic oscillator [22].

Applying Kirchhoff's circuit laws to this topology yields the following set of nonlinear differential equations governing the oscillator's dynamics [22]:

$$\begin{cases} C_1 \dfrac{\mathrm{d}v_{C1}}{\mathrm{d}t} = i_L - i_C \\ C_2 \dfrac{\mathrm{d}v_{C2}}{\mathrm{d}t} = \dfrac{V_1 - v_{C2}}{R_1} + i_L + i_B \\ L_1 \dfrac{\mathrm{d}i_L}{\mathrm{d}t} = V_2 - v_{C1} - v_{C2} - i_L R_L \end{cases}, \tag{1}$$

where v_{C1} and v_{C2} denote the voltages across capacitors C_1 and C_2, respectively; i_L is the current through the inductor; and i_B and i_C are the base and collector currents of the transistor.

In these equations, i_B and i_C are nonlinear functions describing the transistor's operation. The transistor Q_1 alternates between the forward-active region and cutoff. A piecewise-linear approximation for the transistor currents is given by

$$i_B = \begin{cases} 0, & \text{if } -v_{C2} \leq V_{TH} \\ -\dfrac{v_{C2} + V_{TH}}{R_{ON}}, & \text{if } -v_{C2} > V_{TH} \end{cases}, \tag{2}$$

$$i_C = \beta_F \, i_B, \tag{3}$$

where V_{TH} is the base-emitter threshold voltage, R_{ON} is the small-signal on-resistance of the base-emitter junction, and β_F is the transistor's forward current gain.

Chaos emerges in this oscillator from the interplay between the transistor's nonlinear characteristics and the energy exchange among the reactive components (C_1, C_2, and L_1). This interchange produces an effective third-order nonlinear system capable of exhibiting complex dynamics. For instance, one set of component values that yields chaotic oscillations is $V_1 = 5\,\text{V}$, $V_2 = 5\,\text{V}$, $R_L = 40\,\Omega$, $L_1 = 100\,\mu\text{H}$, $C_1 = 54\,\text{nF}$, $C_2 = 54\,\text{nF}$, and $R_1 = 400\,\Omega$, using a transistor such as the 2N3904. Under these conditions, the circuit oscillates with a fundamental frequency of approximately 96.8 kHz.

2.2. Bias Voltage Tuning

This work introduces a modification to the Colpitts chaotic oscillator by incorporating a DC bias source at the BJT transistor's base. Adding an independent voltage source V_3 at the base of Q_1 (see Figure 2) significantly alters the behavior of the system. In the conventional Colpitts oscillator, the base is biased through a resistor from a DC supply, and the feedback loop consists of the inductor L_1 (with series resistance R_L) and the capacitive divider C_1–C_2. In such a configuration, the capacitor voltage v_{C2} directly influences the base-emitter junction, resulting in a relatively straightforward third-order nonlinear system model.

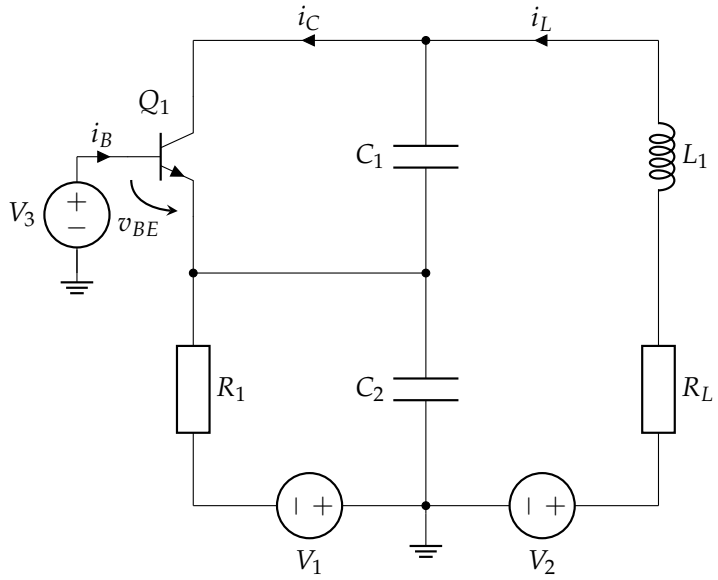


Figure 2. Modified Colpitts chaotic oscillator with an added base-bias voltage V_3.

In the modified configuration, the base is no longer biased solely through R_1; instead, it is driven by the dedicated source V_3. This change effectively decouples v_{C2} from the base-emitter voltage and alters the mathematical structure of the system. Consequently, the base-emitter voltage is now expressed as

$$v_{BE} = V_3 - v_{C2}, \tag{4}$$

which expresses v_{BE} as the difference between the bias source V_3 and the capacitor C_2 voltage v_{C2}.

This shift in bias modifies the circuit's governing equations, although the system remains a third-order oscillator with state variables v_{C1}, v_{C2}, and i_L. The resulting differential equations of the modified Colpitts oscillator are given by

$$\begin{cases} C_1 \dfrac{\mathrm{d}v_{C1}}{\mathrm{d}t} = i_L - i_C \\ C_2 \dfrac{\mathrm{d}v_{C2}}{\mathrm{d}t} = \dfrac{V_1 + v_{BE}}{R_1} + i_L + i_B \\ L_1 \dfrac{\mathrm{d}i_L}{\mathrm{d}t} = V_2 - v_{C1} + v_{BE} - i_L R_L \end{cases}, \tag{5}$$

where v_{C1} is the voltage across C_1, v_{BE} is given by (4), i_L is the inductor current, and i_B and i_C are the base and collector currents, respectively.

To model the transistor's nonlinear behavior in this biased configuration, we continue to use a piecewise-linear approximation for the base current i_B that accounts for the base-emitter threshold:

$$i_B = \begin{cases} 0, & \text{if } v_{BE} \leq V_{TH} \\ \dfrac{v_{BE} - V_{TH}}{R_{ON}}, & \text{if } v_{BE} > V_{TH} \end{cases}, \tag{6}$$

$$i_C = \beta_F \, i_B, \tag{7}$$

where V_{TH} is the base-emitter junction's threshold voltage, R_{ON} is the effective on-resistance of that junction when forward-biased, and β_F is the forward current gain. Introducing the bias V_3 shifts the transistor's operating point, thereby making the base-emitter junction more (or less) sensitive to changes in v_{C2} depending on the magnitude and polarity of V_3.

This adjustment of the base bias affects the onset of conduction in the transistor and the nature of the nonlinear feedback responsible for chaos. By shifting the transistor's conduction region through V_3, the system's bifurcation structure is altered, allowing one to tune the characteristics of chaotic oscillations. In the mathematical model, V_3 enters as an additional offset in the base–emitter voltage, which shifts the equilibrium point of the transistor without changing the system order or introducing new nonlinearities in the simplified equations. Thus, V_3 provides an independent control parameter that decouples biasing from the feedback network, enabling flexible, real-time tuning of the oscillator's operating regime without hardware modifications. This extra degree of freedom enhances design flexibility and ensures adaptive control of chaotic dynamics, which has potential applications in secure communications, sensing, and programmable chaotic signal generation.

3. Numerical Study

The first step in investigating the applicability of the proposed modified Colpitts oscillator for chaotic communication systems is to carry out a detailed numerical analysis. This study aims to predict the circuit's possible dynamical behaviors under parameter variation. Such analysis serves two key purposes: on the one hand, it enables designers to intentionally adjust parameters to achieve desired nonlinear modes; on the other hand, it helps anticipate how the circuit's dynamics may shift due to component tolerances, ageing, thermal effects, or other physical processes.

Section 2 defines the system's range of parameters under study. Introducing the new voltage source V_3 could change the system's dynamics. Thus, the effects of V_3 on the phase portraits and bifurcation diagrams are studied first.

Figure 3 represents the phase portraits of the system, corresponding to three different values of $V_3 = \{-2.5, 0, 2.5\}$ V. It could be clearly seen that the introduction of additional biasing voltage to the transistor base, according to Model (5), does not cause significant qualitative changes in the system's dynamics. The attractor shifts along the y-axis, demonstrating the well-described offset-boosting effect [24].

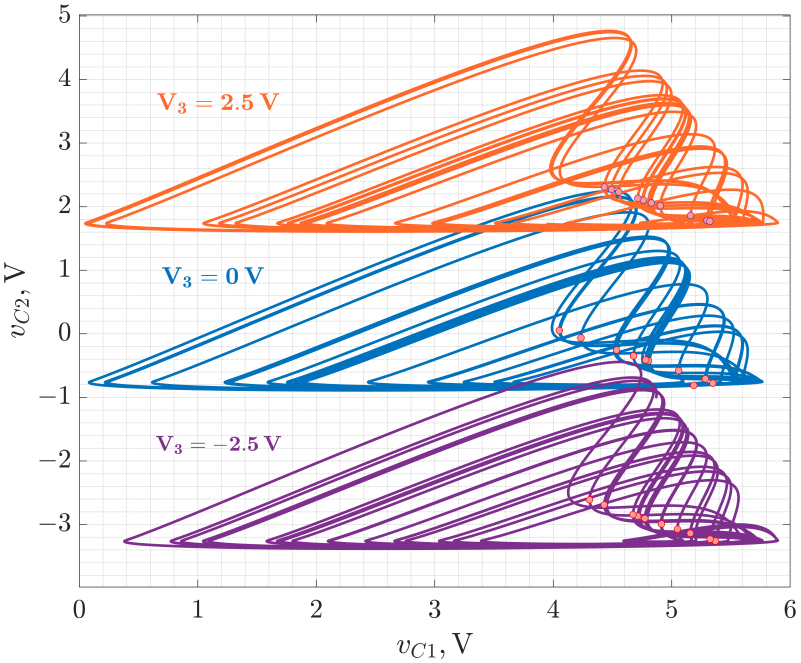


Figure 3. Phase portraits of the Colpitts oscillator with introduced biasing voltage V_3. Parameters of the system are as follows: $V_1 = V_2 = 5$ V, $R_1 = 400\,\Omega$, $\beta = 200$, $L_1 = 100\,\mu$H, $R_L = 40\,\Omega$, $C_1 = C_2 = 35$ nF, $R_{ON} = 100\,\Omega$, $V_{TH} = 0.75$ V, $V_3 = \{-2.5, 0, 2.5\}$ V.

In the piecewise-linear mode of the BJT, the introduction of an additional voltage source V_3, connected between the base and ground, does not significantly affect the system's qualitative dynamics. This could be explained by the fact that V_3 enters the model primarily through the base-emitter voltage v_{BE}. Mathematically, V_3 adds a constant offset to v_{BE}, compensating for a similar shift in the v_{C2} (corresponding to the base-emitter voltage). As long as the condition $v_{BE} > V_{TH}$ is regularly satisfied during oscillations, the circuit's switching behavior and overall nonlinear dynamics remain unchanged. Thus, V_3 acts as a vertical shift in the phase space without altering the structure of the attractor.

It has been demonstrated that the dynamics of the Colpitts oscillators are highly dependent on the values of their capacitors [13]. Thus, to consider this aspect, we obtain the bifurcation diagrams for the selected range of capacitor values $C_1 = C_2 \in [30, 60]$ nF. This analysis allows minimization of the sensitive dependence of the generated signals on the capacitor tolerances or ageing effects, selecting the values in the area of robust chaotic oscillations.

Figure 4 presents a set of bifurcation diagrams of the modified Colpitts oscillator obtained by varying the capacitors C_1 and C_2 values in the range of 30 nF to 60 nF. The results are shown for three different bias voltage values: $V_3 = \{-2.5, 0, 2.5\}$ V.

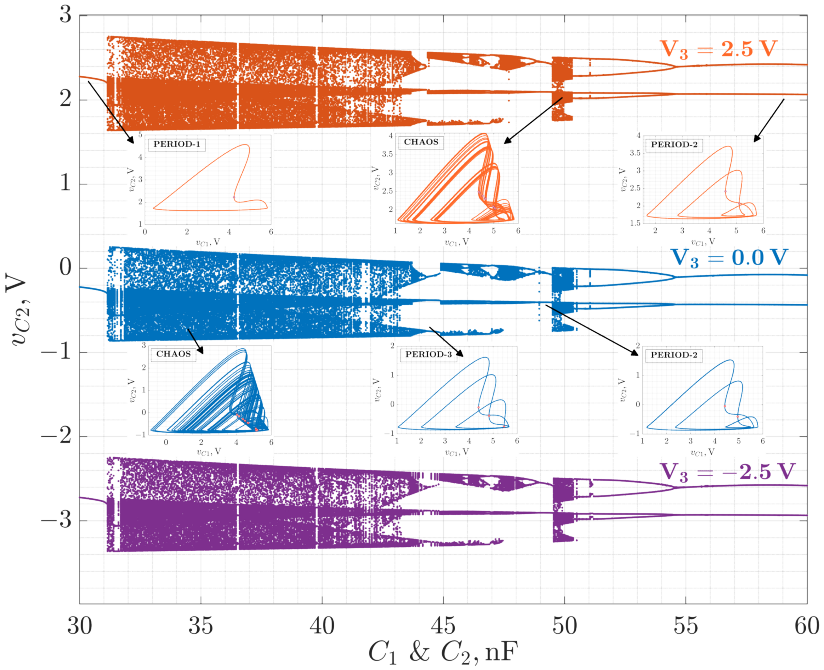


Figure 4. The bifurcation diagrams for the Colpitts chaotic oscillator with the following parameters of the system: $V_1 = V_2 = 5\,\text{V}$; $R_1 = 400\,\Omega$, $\beta = 200$, $L_1 = 100\,\mu\text{H}$, $R_L = 40\,\Omega$, $R_{ON} = 100\,\Omega$, $V_{TH} = 0.75\,\text{V}$, $V_3 = \{-2.5, 0, 2.5\}\,\text{V}$, $C_1 = C_2 \in [30, 60]\,\text{nF}$.

Diagrams presented in Figure 4 illustrate the system's long-term behavior after transients have decayed, with v_{C2} plotted as the bifurcation observable state variable.

The most prominent feature of all diagrams is that while the change in V_3 introduces a vertical shift in the voltage levels (as expected from its role as a bias source between base and ground), it does not alter the qualitative structure of the bifurcation landscape. This indicates that V_3 primarily affects the operating point of the active device (transistor), but not the underlying nonlinear dynamics, at least under the simplified transistor models employed.

In contrast, variations in C_1 and C_2 dramatically affect the oscillator's behavior. The diagrams exhibit classical period-doubling routes to chaos for higher values of capacitances and sudden jumps from period-1 to chaotic oscillations for lower values of C_1 and C_2. Within the chaotic regimes, periodic windows are clearly visible, reflecting islands, where the system temporarily stabilizes into regular oscillations. This complex interplay of order and chaos is a classical feature of low-dimensional nonlinear systems.

It should be noted that in the analysis, it is assumed that both capacitors are degrading at the same rate, which could not be the case in real circuitry. Thus, it would be valuable to identify the dependence of the system's dynamics for a wide range of C_1 and C_2 combinations. This can be represented as a two-dimensional bifurcation diagram (Figure 5), where C_1 and C_2 are chosen as bifurcation parameters and colors indicate periodic or chaotic modes of operation.

To construct the two-dimensional bifurcation maps, the system is numerically integrated using the piecewise-linear transistor model (6), (7). For each pair of C_1, C_2 values, a transient is discarded and the steady-state dynamics are sampled using a Poincare section. The resulting time series are then analyzed to detect periodicity: repeated cycles within numerical tolerance are classified as periodic orbits (up to period-9), while irregular non-repeating sequences are classified as chaos. The map is color-coded by periodicity, with the chaotic regime shown in white. This method allows for visualization of the parameter space, detection of bifurcation borders, and regions of robust chaotic oscillations.

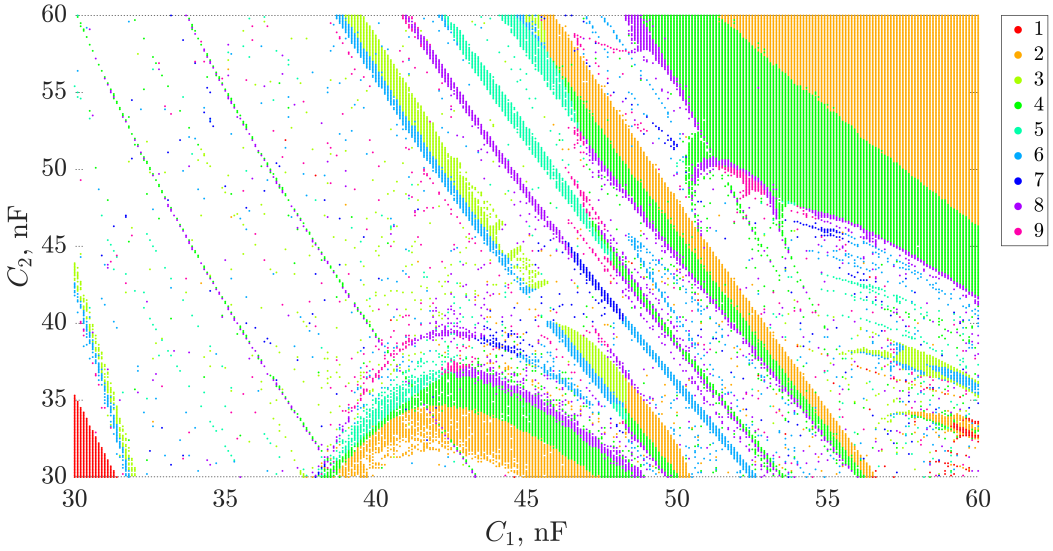


Figure 5. The bifurcation map for the Colpitts chaotic oscillator with the following parameters of the system: $V_1 = V_2 = 5\,\mathrm{V}$; $R_1 = 400\,\Omega$, $\beta = 200$, $L_1 = 100\,\mu\mathrm{H}$, $R_L = 40\,\Omega$, $R_{ON} = 100\,\Omega$, $V_{TH} = 0.75\,\mathrm{V}$, $V_3 = 0\,\mathrm{V}$, $C_1 \in [30, 60]\,\mathrm{nF}$, $C_2 \in [30, 60]\,\mathrm{nF}$.

The two-parameter bifurcation map in the C_1 and C_2 plane in Figure 5 reveals a highly sophisticated structure of the oscillator's dynamic regimes. The diagram shows the dependence of the system's behavior on simultaneous variation of both capacitances, with each color corresponding to a specific periodicity (from period-1 to period-9). The white regions indicate chaotic behavior, where no closed orbit with a low period can be identified within the tested precision.

Broad zones of chaos are observed to dominate large regions of the parameter space. Yet, they are intersected by narrow, well-organized bands of periodicity, representing classical periodic windows embedded in chaos. These periodic tongues appear in arc-like or diagonal shapes, forming Arnold tongue-like structures and showing the system's intense sensitivity to slight variations in both capacitances.

The borders between chaotic and periodic regions are sharp, suggesting the presence of bifurcations such as period-doubling, saddle-node, or crisis-induced intermittency. The observed sequence of periodicities—from period-1 up to period-9—indicates multiple routes to chaos, likely dominated by period-doubling cascades in some regions and quasi-periodic transitions in others.

From a practical standpoint, this analysis highlights the importance of precise capacitor selection. Due to the strong sensitivity of the oscillator's dynamics to capacitance values, even minor deviations arising from manufacturing tolerances or ageing can shift the system into a qualitatively different regime. Such transitions may be undesirable for applications in secure chaotic communication, where unpredictable yet reproducible behavior is desired. Therefore, the capacitor values must be chosen within well-defined intervals that correspond to robust chaotic regimes—regions where chaos persists over a range of parameters, without being interrupted by regular dynamics (e.g., $C_1 = C_2 \in [32, 40]\,\mathrm{nF}$ in the current case). These findings emphasize the necessity of careful numerical bifurcation analysis in the early design phase to ensure reliable circuit operation in the desired nonlinear regime.

It should be stressed that the results obtained through numerical studies based on simplified piecewise-linear transistor models should not be regarded as an exact design guideline. Instead, they serve as a conceptual framework that depicts the system's key dynamic behaviors and parameter dependencies under investigation. While these models help identify bifurcation scenarios and estimate chaotic or periodic operation regions,

they inherently exclude some more complicated physical interdependencies, such as the Early effect, dynamically varying current gain, parasitic elements, and manufacturing tolerances in semiconductor devices. Therefore, experimental validation remains the definitive standard for analyzing chaotic electronic circuits, as it captures the full complexity of real-world behavior beyond the reach of simplified models.

4. Colpitts Chaotic Oscillator Analog Implementation

The study proceeds with a two-fold investigation comprising SPICE-level circuit simulation and hardware prototype measurements to validate the practical feasibility of the proposed chaos-based oscillator for communication applications. While the numerical analysis in Section 3 provides insight into the system's dynamic behavior under idealized conditions, the present section focuses on a more implementation-oriented perspective. First, the oscillator is simulated in the LTspice environment using realistic device models to evaluate its performance under near-physical conditions. This is followed by the construction and testing of a laboratory prototype to experimentally verify the key dynamic features predicted by both the numerical and simulation studies.

4.1. Simulation Study

Following the numerical investigation presented in Section 3, the second stage of the analysis involves a time-domain simulation of the modified Colpitts oscillator using the LTspice simulator software version (x64) 17.1.9. This stage aims to evaluate the circuit's behavior under more realistic conditions by incorporating non-idealities present in commercially available components. While the mathematical model offers valuable insight into the system's dynamic regimes, the LTspice simulation provides a complementary perspective that bridges theoretical analysis and hardware implementation.

In contrast to the numerical approach, LTspice uses detailed SPICE-level models, particularly for active components such as the BJT. These models account for nonlinearities, parasitic effects, and temperature dependencies, yielding results that are more representative of the physical prototype. Although the simulation does not fully capture all practical factors, it serves as a crucial intermediate validation step, offering a more hardware-faithful approximation of the circuit dynamics.

All component values and operating parameters used in the simulation were consistent with those defined in Section 2. The implementation of the additional DC bias voltage V_3 was investigated to evaluate its impact on circuit operation. The effects of the bias voltage V_3 were analyzed regarding time-domain signal waveforms and reconstructed phase portraits, allowing direct comparison with the numerical model and subsequent experimental measurements.

In Figure 6, LTspice-simulated attractor projections in the v_{C1}–v_{C2} phase plane for three values of the DC bias voltage $V_3 = \{-2.5, 0, 2.5\}$ V are presented. The results illustrate both vertical translation and deformation of the attractor shape, reflecting the increased realism of the transistor model used in simulation.

To evaluate the impact of the DC bias voltage V_3 under more realistic conditions, phase portraits were reconstructed from LTspice simulation data for three representative values of V_3. As shown in Figure 6, the attractors undergo a vertical shift in the v_{C1}–v_{C2} plane, consistent with offset-boosting behavior. In addition to translation, the attractor geometry itself changes significantly with bias variation. Unlike the idealized numerical model, which predicts primarily a positional shift, the LTspice results capture more complex dynamic transformations. These differences stem from the high-fidelity transistor model used in the SPICE simulation, which accounts for nonlinear junction behavior, charge storage effects, and other parasitics typically present in hardware implementations.

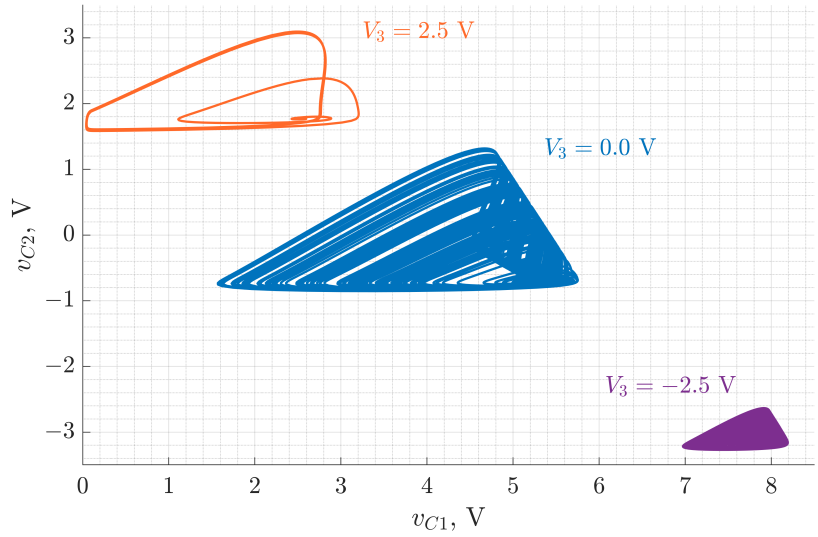


Figure 6. Phase portraits of the Colpitts oscillator with introduced biasing voltage V_3, obtained in the LTspice simulation.

A set of bifurcation diagrams was generated by launching LTspice simulations from within the MATLAB environment to investigate the influence of capacitor values on the oscillator's behavior. This approach allowed automated sweeping of C_1 and C_2 from 30 nF to 60 nF for three different DC bias voltages: $V_3 = \{-2.5, 0, 2.5\}$ V. The state variable v_{C2} was extracted from each simulation after transient effects subsided and used as the bifurcation observable. The resulting diagrams are shown in Figure 7.

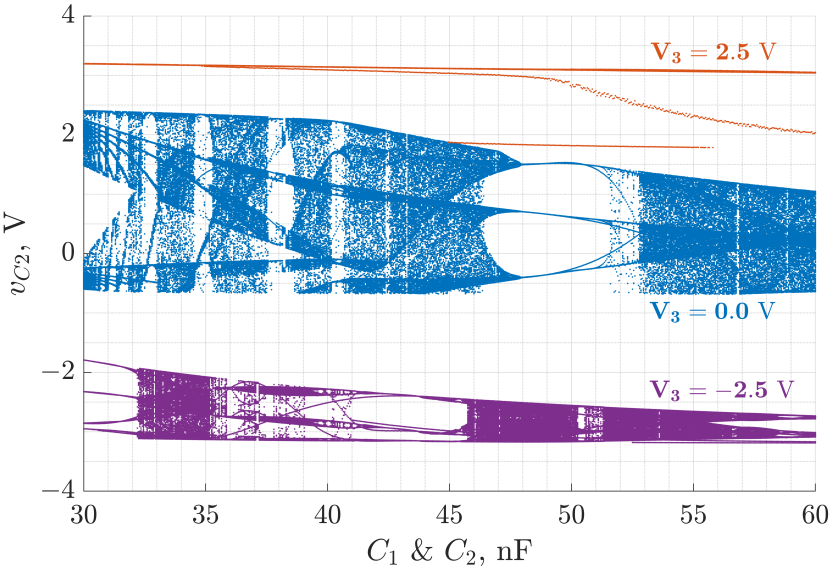


Figure 7. Bifurcation diagrams of the Colpitts oscillator obtained via MATLAB-controlled LTspice simulations for varying values of $C_1 = C_2 \in [30, 60]$ nF and three distinct bias voltages: $V_3 = \{-2.5, 0, 2.5\}$ V. The diagrams use v_{C2} as the bifurcation observable after transient decay.

As observed in Figure 7, the application of different V_3 values not only vertically shifts the bifurcation structures but also introduces clear variations in their topology and extent. In contrast to the numerically obtained bifurcation diagrams based on idealized models, the LTspice simulations indicate that the bias voltage substantially alters the qualitative nature of the system's dynamics. This can be attributed to the higher-fidelity transistor modeling in LTspice, which captures junction nonlinearities, charge storage, and region transitions.

Consequently, the dynamic response is more sensitive to biasing, resulting in bifurcation diagrams with differing chaotic bandwidths, densities, and bifurcation window structure. These findings emphasize the necessity of accounting for physical device behavior when designing chaos-based systems and highlight specific capacitor regions where robust chaotic oscillation persists under bias variation.

4.2. Prototype

A dedicated printed circuit board (PCB) prototype was developed to experimentally validate the simulation findings and assess the practical behavior of the modified Colpitts oscillator. The oscillator circuit was designed using KiCad software (version 8.0) and manufactured via PCB milling. The board includes two variable resistors, VR_1 and VR_2, which allow manual tuning of the operating point to ensure the oscillator operates within a chaotic regime. The fabricated prototype of the Colpitts chaotic oscillator is shown in Figure 8.

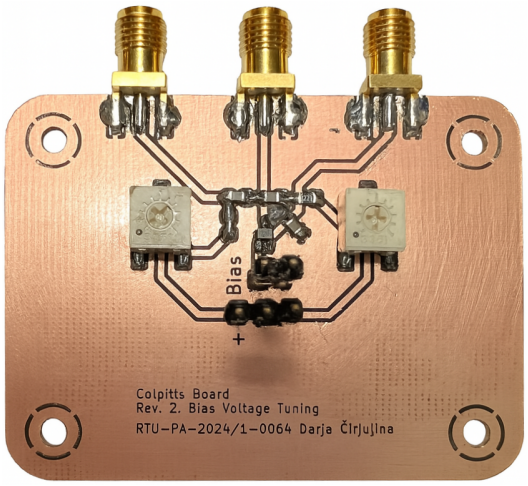


Figure 8. PCB Design of the Colpitts chaotic oscillator created in KiCad software.

To examine how the base bias voltage V_3 affects the circuit's dynamics in practice, phase portraits were measured from the prototype for five different values of $V_3 = \{-2.5, -1.0, 0, 1.0, 2.5\}$ V. For each case, the attractor was reconstructed from voltage measurements of v_{C1} and v_{C2}. Figure 9 presents the results. The blue attractors correspond to the unbiased configuration where the transistor base is directly grounded. The orange attractors represent the behavior when an external DC bias voltage is applied to the base via an additional voltage source.

Several observations emerge from Figure 9. First, the attractor exhibits uniform structure when the base is grounded (blue curves). However, once the external voltage source is connected, even when $V_3 = 0$ V, the attractor shape shifts. This behavior is attributed to parasitic capacitance and leakage currents introduced by the voltage source's physical wiring and internal impedance. These parasitics alter the local bias conditions at the transistor base, leading to measurable changes in the oscillator's state space trajectory.

As V_3 is swept across a wider range (-2.5 to 2.5 V), further changes in the attractor shape and position are observed. These variations arise due to the strong dependence of BJT operation on base-emitter voltage. Specifically, the applied bias alters the transistor's quiescent point, thereby modifying the collector current and consequently the charging dynamics of the capacitors. At higher positive values of V_3, the transistor remains more continuously in its active region. In contrast, strongly negative bias tends to push it closer to the cutoff or saturation, reducing the amplitude and complexity of the oscillations. This is reflected in the attractor compression or separation across voltage levels.

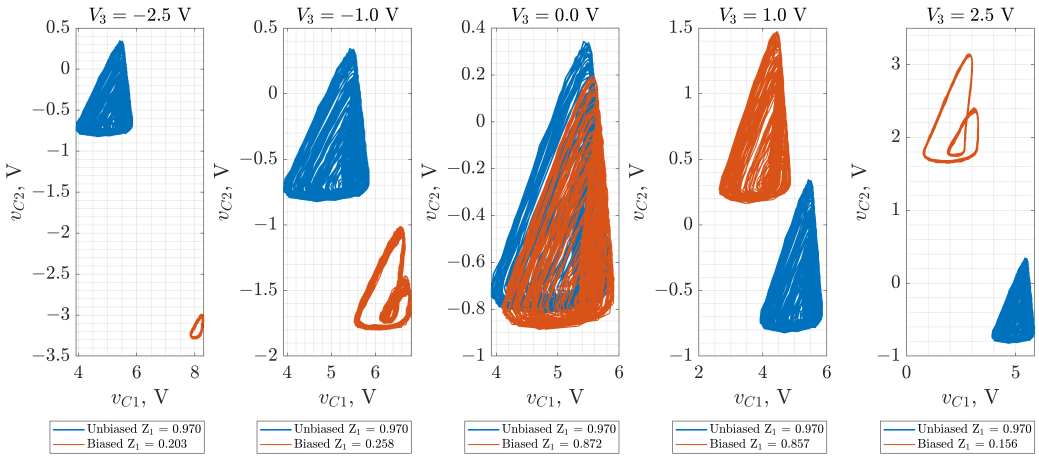


Figure 9. Experimentally measured attractors from the Colpitts chaotic oscillator prototype for various DC bias voltages V_3. Blue curves represent the unbiased configuration (base grounded); orange curves represent the biased case.

The 0–1 test for chaos (Z1TEST) was applied to the measured voltage signals to quantify these changes [25], and the resulting Z_1-values are shown in the figure legend. The test numerically evaluates the degree of chaotic behavior, with values closer to 1 indicating stronger chaotic behavior but values closer to 0 indicating periodic behavior. The results confirm that the biased configurations exhibit reduced or suppressed chaotic dynamics for extreme V_3 values, aligning with the observed attractor deformation.

While the general trends observed in the experimental results are consistent with those from LTspice simulations (see Figure 6), clear differences in attractor shape and signal characteristics emerge due to hardware parasitics and real-world component nonidealities. Both simulations and experiments demonstrate that V_3 causes not only a vertical shift in the attractor but also a transformation in shape and complexity. However, the experimental results further confirm the importance of parasitic elements and external circuit influences that are not fully captured even by SPICE-level simulations. These findings emphasize the necessity of hardware validation for chaos-based systems, particularly when operated near sensitive bifurcation boundaries.

5. Colpitts Chaotic Oscillator Digital Implementation

The current subsection is devoted to the digital implementation of the Colpitts chaotic oscillator model, breaking down the steps performed to transform the differential equations with an added base-bias V_3 voltage (5) for FPGA-based digital design. In the first transformation step, the following dimensionless variables are introduced:

$$\rho_1 = \sqrt{\frac{L_1}{C_1}}, \quad \omega_1 = \frac{1}{\sqrt{L_1 \cdot C_1}}, \quad \tau_1 = \omega_1 \cdot t \ , \tag{8}$$

where ω_1 is the characteristic frequency; ρ_1 is the characteristic impedance; τ is the dimensionless time. These parameters are then applied to normalize and simplify the equations, resulting in (10). It is important to note that in (10) V_1 is taken as 5 V, i.e., the sign is moved from the constant to the equation, for convenience. The goal of applying dimensional normalization is to express the oscillator equations in a dimensionless form suitable for digital implementation on the FPGA. This step reduces the dynamic range of variables, prevents numerical overflow in fixed-point arithmetic, and enables comparison of different oscillators on a common basis. As for the time scale of the dimensionless equations, the characteristic frequency w_1 is selected. The fundamental frequency of the Colpitts oscillator can also be used, resulting in the following dimensionless variables:

$$\rho_0 = \sqrt{\frac{L_1}{C_{eq}}}, \quad \omega_0 = \frac{1}{\sqrt{L_1 \cdot C_{eq}}}, \quad C_{eq} = \frac{C_1 \cdot C_2}{C_1 + C_2}, \quad \tau_0 = \omega_0 \cdot t \ , \tag{9}$$

where ω_0 is the fundamental frequency; ρ_0 is the equivalent characteristic impedance; τ is the dimensionless time.

It is important to note that the choice of normalization does not change the dynamics of the oscillator, only the appearance of the equations in dimensionless form. To derive the dimensionless equations, the variables in (8) are used. The fundamental frequency of the Colpitts oscillator can also be utilized, resulting in a different appearance of normalized equations (different coefficients and constants) with preserved dynamics and chaotic attractor. Appendix A elaborates in detail on the difference of normalized equations using (8) and (9) and how this affects the FPGA implementation of the equations.

$$\begin{cases} \dfrac{\mathrm{d}v_{C1}}{\mathrm{d}\tau_1} \cdot \omega_1 = \dfrac{i_L - \beta \cdot i_B}{C_1} \cdot \dfrac{\rho_1}{\rho_1} \\ \dfrac{\mathrm{d}v_{C2}}{\mathrm{d}\tau_1} \cdot \omega_1 = \dfrac{V_3 - v_{C2} - V_1}{R_1 \cdot C_2 \cdot \dfrac{\rho_1}{\rho_1}} + \dfrac{i_L + i_B}{C_2} \cdot \dfrac{\rho_1}{\rho_1} \\ \dfrac{\mathrm{d}i_L}{\mathrm{d}\tau_1} \cdot \omega_1 \cdot \dfrac{\rho_1}{\rho_1} = \dfrac{V_2 - v_{C1} + V_3 - v_{C2}}{L_1} - i_L \cdot \dfrac{R_L}{L_1} \cdot \dfrac{\rho_1}{\rho_1} \end{cases} . \tag{10}$$

The variables shown in (11) are introduced in the second transformation step, resulting in simplified normalized equations in (12):

$$\begin{aligned} & i_L \cdot \rho_1 = \tilde{i}_L, \quad i_B \cdot \rho_1 = \tilde{i}_B, \quad \frac{\omega_1}{\rho_1} = \frac{1}{L_1}, \\ & \epsilon = \frac{C_2}{C_1}, \quad \frac{R_L}{\rho_1} = \tilde{R}_L, \quad \frac{R_1}{\rho_1} = \tilde{R}_1, \\ & x = v_{C1}, \quad y = v_{C2}, \quad z = \tilde{i}_L \end{aligned} \ . \tag{11}$$

$$\begin{cases} \dfrac{\mathrm{d}x}{\mathrm{d}\tau_1} = z - \beta \cdot \tilde{i}_B \\ \dfrac{\mathrm{d}y}{\mathrm{d}\tau_1} = -\dfrac{V_3 - y - V_1}{\tilde{R}_1 \cdot \epsilon} + \dfrac{z + \tilde{i}_B}{\epsilon} \\ \dfrac{\mathrm{d}z}{\mathrm{d}\tau_1} = V_2 - x + V_3 - y - z \cdot \tilde{R}_L \end{cases} . \tag{12}$$

In the following step, the Euler–Cromer numerical integration is applied to acquire the approximate discrete solution for the integration step $\Delta\theta$ shown in (13). The Euler–Cromer method was selected as it provides a computationally efficient integrator for oscillatory systems, preserving qualitative behavior (such as amplitude and phase stability) more effectively than the standard forward Euler method [26]. The simplicity of the Euler–Cromer method makes it well suited for discrete hardware implementation. Although higher-order methods such as Runge–Kutta [27] are preferable for obtaining exact trajectories, the Euler–Cromer method preserves the attractor shape—provided that $\Delta\theta$ is chosen carefully—which is precisely the requirement for digital hardware implementation.

The piecewise-linear approximation for the base current with the introduced transformations is presented in (14). The resultant difference Equation System (13) can then be implemented in a digital system, since each next value of the state variables is acquired by adding the derivative multiplied by the integration step to the current value of the state variable:

$$\begin{cases} \underbrace{x_{n+1}}_{\text{Next value}} = \underbrace{x_n}_{\text{Current value}} + \underbrace{\left(z_n - \beta \cdot \tilde{i}_B\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{y_{n+1}}_{\text{Next value}} = \underbrace{y_n}_{\text{Current value}} + \underbrace{\left(\frac{V_3 - y_n - V_1}{\tilde{R}_1 \cdot \epsilon} + \frac{z_n + \tilde{i}_B}{\epsilon}\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{z_{n+1}}_{\text{Next value}} = \underbrace{z_n}_{\text{Current value}} + \underbrace{\left(V_2 - x_n + V_3 - y_n - z_n \cdot \tilde{R}_L\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \end{cases} . \quad (13)$$

$$\tilde{i}_B = \begin{cases} 0, & \text{if } -y_n \leq V_{TH} \\ \dfrac{V_3 - y_n - V_{TH}}{R_{ON}} \cdot \rho_1, & \text{if } -y_n > V_{TH} \end{cases} . \quad (14)$$

Figure 10 presents the digital design approach for implementing the Colpitts chaotic oscillator difference Equation System (13). The figure demonstrates the design slice for the x state variable, as the approach is identical for the other state variables. The core of the system is the register that updates the state variable x on the rising edge of the clock signal, thus acquiring the current value x_n. To acquire the next value x_{n+1}, first, the current values x_n, y_n and z_n are passed to the derivative calculation pipeline. The pipeline takes the current values and constants and performs operations labeled as "Derivative" in (13) for each state variable accordingly. Second, the output of the pipeline dx is multiplied by the integration step $\Delta\theta$. Finally, the result of the multiplication is added to x_n, thus acquiring x_{n+1}. This design is replicated to y and z state variables, with the derivative calculation pipeline being the common block. This design was first proposed in [21] for Vilnius [28] and RC [29] chaotic oscillators and is now applied to the Colpitts chaotic oscillator.

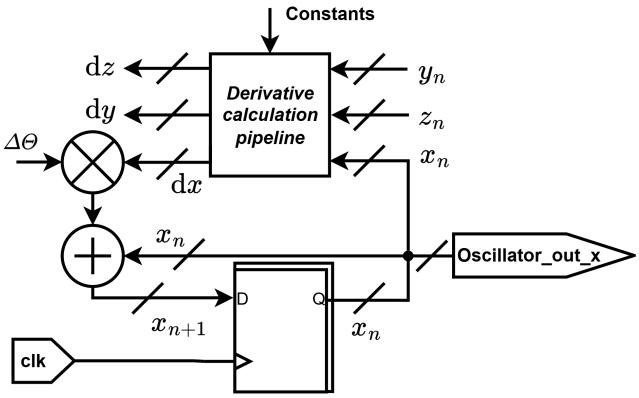


Figure 10. Digital design slice of the Colpitts oscillator for FPGA implementation.

It is important to note that in this FPGA implementation, the master clock frequency and the numerical integration step $\Delta\theta$ are not identical quantities. The FPGA system clock f_{clk} (100 MHz) determines the rate at which arithmetic operations are executed, while $\Delta\theta$ is implemented as a constant multiplier in the discretized equations to control the effective integration step size. In this way, $\Delta\theta$ can be set independently of the hardware clock, allowing the same FPGA design to emulate different step sizes by adjusting only the scaling constants, thus ensuring flexibility in digital realization. In order to match the analog chaos oscillator, the integration step must be the relation of the scaling frequency to the clock frequency (15).

$$\Delta\theta = \frac{f_1}{f_{clk}} = \frac{\omega_1}{2\pi \cdot f_{clk}} \quad (15)$$

As the system is implemented in fixed-point arithmetic, the $\Delta\theta$ is rounded with the fixed-point precision. A more detailed numerical convergence study, including step size sensitivity and the estimate of the largest Lyapunov exponent, is beyond the scope of this work and will be addressed in future investigations focused specifically on quantitative stability assessment of fixed-point chaotic models.

The derivative calculation pipeline design is addressed next. The "Derivative" part from (13) is shown in (16). The pipeline approach is set to split the mathematical operations with the help of registers. To reduce the number of operations, the nonlinearity $\tilde{i}_B$ is approximated using read-only memory (ROM). The $\tilde{i}_B$ is used in two equations and it is most convenient to form two different ROMs. The first ROM contains $\beta \cdot \tilde{i}_B$. The second ROM contains $\frac{V_3}{\tilde{R}_1 \cdot \epsilon} - \frac{y_n}{\tilde{R}_1 \cdot \epsilon} - \frac{V_1}{\tilde{R}_1 \cdot \epsilon} + \frac{\tilde{i}_B}{\epsilon}$, as the $\tilde{i}_B$ itself has y_n as input argument.

It is important to note that since the two ROMs contain the bias voltage V_3, new memory data must be created for the specific V_3. Similarly, $V_2 + V_3$ is stored as a single constant V_{23}, which must also be updates accordingly. The simplified pipeline is shown in (17).

$$\begin{cases} \mathrm{d}x = z_n - \beta \cdot \tilde{i}_B \\ \mathrm{d}y = \dfrac{V_3}{\tilde{R}_1 \cdot \epsilon} - \dfrac{y_n}{\tilde{R}_1 \cdot \epsilon} - \dfrac{V_1}{\tilde{R}_1 \cdot \epsilon} + \dfrac{z_n}{\epsilon} + \dfrac{\tilde{i}_B}{\epsilon} \\ \mathrm{d}z = V_{23} - x_n - y_n - z_n \cdot \tilde{R}_L \end{cases} . \tag{16}$$

$$\begin{cases} \mathrm{d}x = z_n - \mathrm{ROM}_1 \\ \mathrm{d}y = \dfrac{z_n}{\epsilon} + \mathrm{ROM}_2 \\ \mathrm{d}z = V_{23} - x_n - y_n - z_n \cdot \tilde{R}_L \end{cases} . \tag{17}$$

The design of the memory is depicted in Figure 11. The system is designed in fixed-point arithmetic with an 8-bit-wide integer part and a 14-bi-wide fractional part of the output state variables. The ROMs have a 12-bit address space and store 6-bit-wide integer 16-bit-wide fractional part data. The read address in both ROMs is formed from the y_n state variable by taking 6 integer bits and 6 fractional bits.

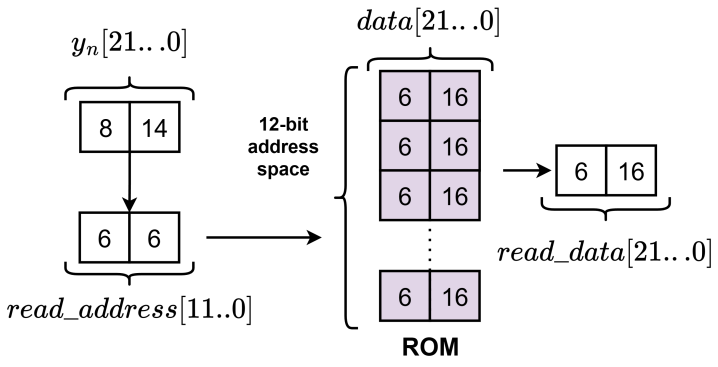


Figure 11. The ROM design for the Colpits chaotic oscillator FPGA implementation.

The digital design of the Colpitts chaotic oscillator with added base-bias V_3 voltage is verified in MATLAB 2023b. Figure 12 presents the x_n–y_n (reflects the v_{C1}–v_{C2}) phase trajectories for three values of the DC bias voltage $V_3 = \{-2.5, 0, 2.5\}$ V. The phase portrait illustrates a completely different behavior of the oscillator model with the applied V_3 compared to that shown in Figure 6. This can be attributed to the simplified mathematical model of the transistor considered initially.

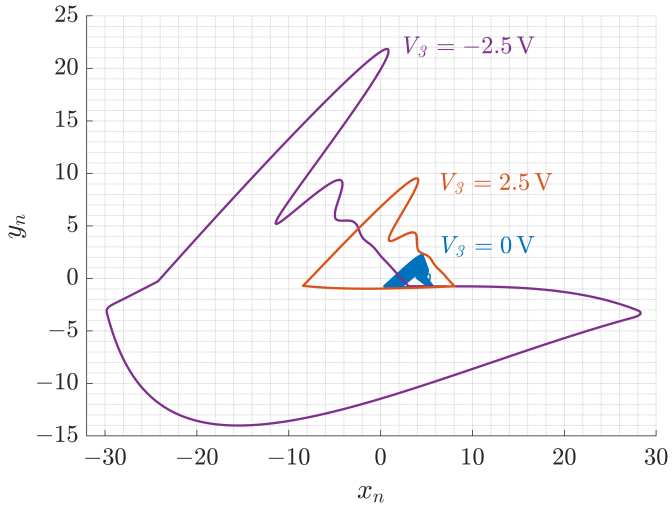


Figure 12. Phase portraits of the FPGA-based Colpitts oscillator with introduced biasing voltage V_3.

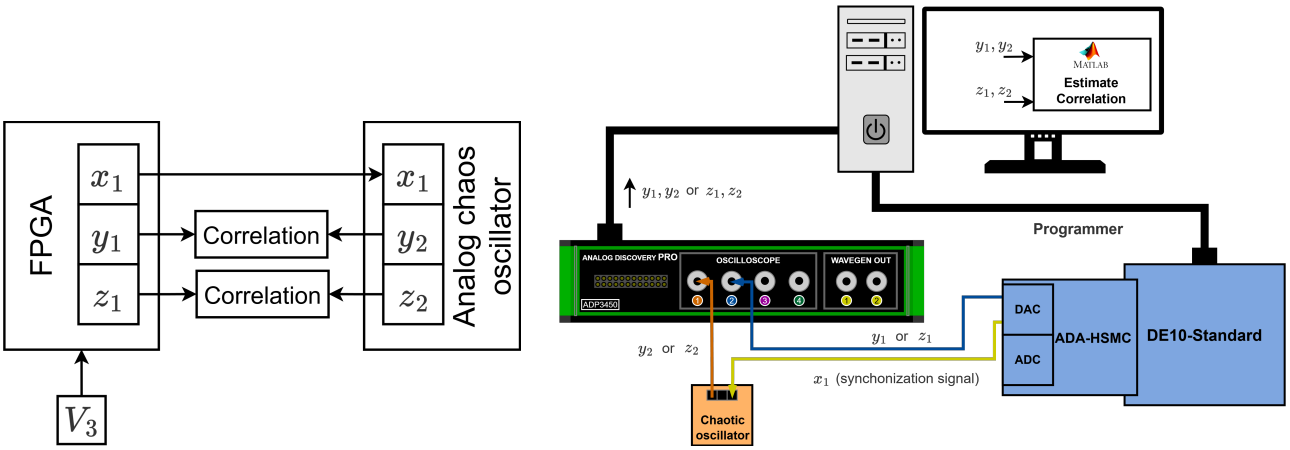
6. Analog–Discrete and Discrete–Analog Synchronization

This section is devoted to experimentally investigating the possibility of the analog–discrete and discrete–analog synchronization between the analog oscillator implemented on the PCB and the discrete oscillator implemented in an FPGA using Very-High-Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). The key investigation point is whether the synchronization can be achieved with base-bias V_3 voltage added to the analog or the discrete oscillator. As demonstrated previously, the two oscillators exhibit different responses to variations of V_3.

To achieve synchronization, we employ a Pecora–Carroll drive–response scheme in which one measured state of the drive oscillator is injected into the response oscillator each step (state replacement), while the remaining states evolve according to the model dynamics. In practice, we couple via the capacitor-voltage state x with applied normalization as in Section 5.

The discrete–analog synchronization study is presented in Figure 13. The state variables of the FPGA-based chaotic oscillator are x_1, y_1 and z_1, while the state variables of the analog oscillator are x_2, y_2 and z_2. The discrete–analog synchronization is Pecora–Carroll synchronization, as demonstrated in Figure 13a. The state variable x is chosen as a synchronization signal based on [11]. The FPGA-based oscillator with the applied V_3 is the drive system, while the analog oscillator is the response system. The synchronization is evaluated using the Pearson correlation coefficient for y_1, y_2 and z_1, z_2.

Figure 13b demonstrates the experimental setup used to perform the study. The FPGA-based chaotic oscillator runs on the Terasic DE10-Standard board with the 100 MHz clock frequency. To interface the FPGA-based oscillator, an Terasic ADA-HSMC daughter card is used, providing the two-channel analog-to-digital converter (ADC) as well as the two-channel digital-to-analog converter (DAC). The first DAC channel outputs the synchronization x_1 signal, while the other channel outputs the y_1 or the z_1 signal. The synchronization signal is passed to the analog oscillator implemented on the PCB. The Digilent's Analog Discovery Pro (ADP3450) is used to record the y_1, y_2 and z_1, z_2 signals that are then used to estimate the Pearson correlation in MATLAB. The measurements are performed for different values of $V_3 = \{-2.5, -1.0, 0, 1.0, 2.5\}$ V applied to the FPGA-based oscillator.

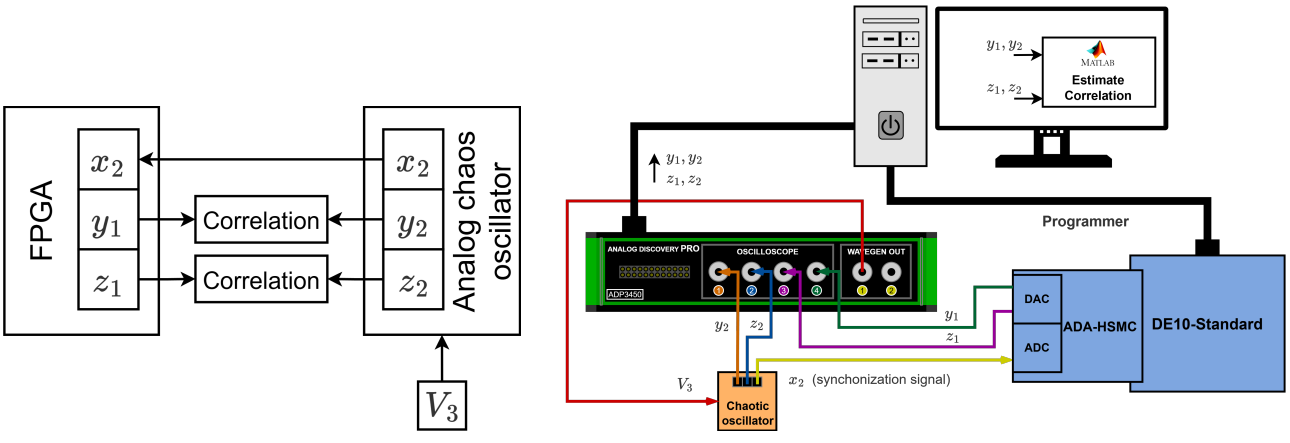


(**a**) (**b**)

Figure 13. Discrete–analog Pecora–Carroll synchronization, showing state variables used for synchronization and correlation analysis (**a**) and experimental setup for synchronization evaluation with different V_3 applied to the discrete oscillator (**b**).

The analog–discrete synchronization study is outlined in Figure 14. The general approach and setup are similar to those in Figure 13; the key difference is that the analog oscillator with the applied V_3 is the drive system, while the FPGA-based oscillator is the response system (see Figure 14a). Like in the previous study, the synchronization is evaluated using the Pearson correlation coefficient for y_1, y_2 and z_1, z_2.

Figure 14b demonstrates the experimental setup used for the study. The x_2 synchronization signal from the analog chaotic oscillator is passed to the FPGA-based oscillator via the ADC. The DACs output the y_1 and z_1 state variables of the FPGA-based oscillator. The ADP3450 records the y_1, y_2 and z_1, z_2 signals that are then used to estimate the Pearson correlation in MATLAB. The measurements are performed for different values of $V_3 = \{-2.5, -1.0, 0, 1.0, 2.5\}$ V applied to the analog chaotic oscillator using the waveform generator of the ADP3450.



(**a**) (**b**)

Figure 14. Analog-discrete Pecora–Carroll synchronization, showing state variables used for synchronization and correlation analysis (**a**) and experimental setup for synchronization evaluation with different V_3 applied to the analog oscillator (**b**).

Table 1 compiles the results of the Pearson's correlation coefficient fort fort for analog–discrete and discrete–analog synchronizationbase bias voltage V_3. The Pearson's correlation coefficient for perfectly synchronous signals equals 1, while the Pearson correlation coeffi-

cient equals 0 for completely asynchronous signals. The table demonstrates a coefficient of more than 0.9 in most cases, indicating that the chaotic synchronization is achieved despite the different behavior of the analog and FPGA-based chaos oscillators with applied V_3. It is visible that the only case that demonstrates the overall lower correlation coefficient (0.7 to 0.9) is the case of y state variables in the discrete–analog synchronization case. The likely reason for the reduced correlation coefficient lies in the model simplifications, since the discrete model was designed to reproduce the chaotic attractor rather than to precisely match the exact trajectories of the analog chaotic oscillator. Additionally, hardware nonidealities play a significant role, as imperfections in the analog oscillator directly influence its dynamics. Another observation is that applying a negative base-bias V_3 voltage results in slightly better synchronization than a positive voltage.

Table 1. Synchronization evaluation using the Pearson's correlation coefficient.

	Discrete–Analog		**Analog–Discrete**	
Bias Voltage V_3, V	**y_1 and y_2**	**z_1 and z_2**	**y_1 and y_2**	**z_1 and z_2**
−2.5	0.77	0.96	0.99	0.99
−1.0	0.87	0.97	0.99	0.99
0.0	0.93	0.97	0.91	0.96
1.0	0.79	0.90	0.91	0.94
2.5	0.72	0.90	0.99	0.98

The results highlight that synchronization is invariant to the base-bias voltage V_3. The dynamics of the drive oscillator are enforced and the generalized synchronization is achieved, thus not requiring explicit compensation of the V_3 mismatch.

7. Discussion

This work investigated the nonlinear dynamics and hybrid synchronization of a modified Colpitts chaotic oscillator with a tunable base bias voltage V_3, potentially enabling effective variation of the oscillator's behavior, affecting the offset and shape of phase space attractors. A multi-level approach was employed, including numerical bifurcation analysis, SPICE-level circuit simulations, experimental measurements using a custom-built analog prototype, and FPGA-based digital implementation. The central objective was to study the feasibility of achieving synchronization between analog and discrete realizations of the oscillator under varying conditions of base bias voltage, which acts as a control parameter for the system's dynamic behavior.

The numerical studies, relying on a simplified piecewise-linear model of the transistor, indicated that the application of a DC bias voltage primarily causes an offset in the attractor position within the phase space, without significantly altering the oscillator's qualitative dynamics. Bifurcation analysis allowed us to identify the sensitivity of the qualitative dynamics on the parameters (e.g., capacitor values) and map the robust chaotic operating regions.

SPICE simulations and practical hardware tests revealed a more dynamically rich behavior. The system's response to variations in V_3 was more complex, with observable attractor deformation and even partial suppression of chaotic behavior under extreme bias values. The observed differences highlight the limitations of idealized models and emphasize the influence of physical parasitics, realistic transistor behavior, and implementation-specific effects on the circuit's dynamics.

A digital implementation of the Colpitts oscillator was realized on an FPGA using fixed-point arithmetic and the Euler–Cromer integration scheme. While this implementation enabled precise control and reproducibility, it inevitably introduced simplifications

due to model discretization and limited numerical resolution. As a result, the discrete oscillator did not replicate the analog dynamics exactly, particularly in how it responded to changes in the base bias voltage. Despite these differences, synchronization was successfully achieved between the analog and discrete systems, both when the discrete oscillator acted as the drive system (discrete–analog case) and when it served as the response system (analog–discrete case).

This result is of particular importance. This demonstrates that exact waveform replication is not required for effective chaotic synchronization. What appears to be more critical is the preservation of the system's underlying dynamic structure. Even with the presence of quantization effects and modeling simplifications, the discrete oscillator could track the analog system with high precision, as confirmed by Pearson's correlation coefficients consistently exceeding 0.9 in most test conditions. This finding simplifies deployment in future hardware implementations, particularly in resource-constrained environments.

From an application standpoint, this work supports the potential use of hybrid analog–discrete chaotic systems in low-power secure communication networks, such as those used in the IoT. In such systems, analog chaotic circuits can serve as lightweight signal generators at the sensor node level, while digital versions can be deployed at the gateway or controller level for synchronization and decoding. The robustness of synchronization in the presence of modeling inaccuracies or hardware non-idealities is a strong enabler for real-world deployment.

These results demonstrate that hybrid synchronization between analog and discrete chaotic systems is feasible and robust, offering a promising pathway for developing secure and energy-efficient communication architectures in embedded and IoT environments. Future studies will address improving discrete models to better reflect the analog system's nonlinearities under varying bias conditions. Additionally, the impact of noise, signal quantization, sampling rate mismatches, and communication channel imperfections on synchronization quality deserves systematic investigation. More advanced synchronization schemes, such as adaptive or generalized synchronization, may also enhance the overall system's performance. Future work could also consider the use of modern physics-informed neural networks (PINNs) [30] to learn transistor nonlinearities and parasitic effects under base-bias control, constrained by the Colpitts oscillator equations. Such PINN-enhanced models could improve the accuracy of digital realizations and reduce discrepancies with hardware, thereby strengthening the robustness and stability of hybrid synchronization between analog and FPGA implementations.

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Abbreviations

The following abbreviations are used in this article:

ADC	Analog-to-Digital Converter
ADP3450	Digilent's Analog Discovery Pro
BJT	Bipolar Junction Transistor
DAC	Digital-to-Analog Converter
DC	Direct Current
FPGA	Field Programmable Gate Array
IoT	Internet of Things
PCB	Printed Circuit Board
QCSK	Quadrature Chaos Shift Keying
RF	Radio Frequency
ROM	Read-Only Memory
SNR	Signal-to-Noise Ratio
SoC	System on a Chip
VHDL	Very-High-Speed Integrated Circuit (VHSIC) Hardware Description Language
Z1TEST	0–1 Test for Chaos

Appendix A

This section elaborates on the derivation of normalized equations using the characteristic frequency ω_1 and the normalized equations using the fundamental frequency ω_0 and how this reflects the digital implementation of the oscillator. First, the characteristic frequency ω_1 and the related parameters are defined in Equation (A1).

$$\rho_1 = \sqrt{\frac{L_1}{C_1}}, \quad \omega_1 = \frac{1}{\sqrt{L_1 \cdot C_1}}, \quad \tau_1 = \omega_1 \cdot t \ . \tag{A1}$$

Deriving the normalized equations using (A1) is outlined in (A2)–(A4).

$$\begin{cases} \dfrac{\mathrm{d}v_{C1}}{\mathrm{d}\tau_1} \cdot \omega_1 = \dfrac{i_L - \beta \cdot i_B}{C_1} \cdot \dfrac{\rho_1}{\rho_1} \\ \dfrac{\mathrm{d}v_{C2}}{\mathrm{d}\tau_1} \cdot \omega_1 = \dfrac{V_3 - v_{C2} - V_1}{R_1 \cdot C_2 \cdot \dfrac{\rho_1}{\rho_1}} + \dfrac{i_L + i_B}{C_2} \cdot \dfrac{\rho_1}{\rho_1} \\ \dfrac{\mathrm{d}i_L}{\mathrm{d}\tau_1} \cdot \omega_1 \cdot \dfrac{\rho_1}{\rho_1} = \dfrac{V_2 - v_{C1} + V_3 - v_{C2}}{L_1} - i_L \cdot \dfrac{R_L}{L_1} \cdot \dfrac{\rho_1}{\rho_1} \end{cases} . \tag{A2}$$

$$\begin{gathered} i_L \cdot \rho_1 = \tilde{i}_L, \quad i_B \cdot \rho_1 = \tilde{i}_B, \quad \frac{\omega_1}{\rho_1} = \frac{1}{L_1}, \\ \epsilon = \frac{C_2}{C_1}, \qquad \frac{R_L}{\rho_1} = \tilde{R}_L, \qquad \frac{R_1}{\rho_1} = \tilde{R}_1, \\ x = v_{C1}, \qquad y = v_{C2}, \qquad z = \tilde{i}_L \end{gathered} \ . \tag{A3}$$

$$\begin{cases} \dfrac{\mathrm{d}x}{\mathrm{d}\tau_1} = z - \beta \cdot \tilde{i}_B \\ \dfrac{\mathrm{d}y}{\mathrm{d}\tau_1} = -\dfrac{V_3 - y - V_1}{\tilde{R}_1 \cdot \epsilon} + \dfrac{z + \tilde{i}_B}{\epsilon} \\ \dfrac{\mathrm{d}z}{\mathrm{d}\tau_1} = V_2 - x + V_3 - y - z \cdot \tilde{R}_L \end{cases} . \tag{A4}$$

The normalized equation of the nonlinearity in this case is

$$\tilde{i}_B = \begin{cases} 0, & \text{if } -y \le V_{TH} \\ \dfrac{V_3 - y - V_{TH}}{R_{ON}} \cdot \rho_1, & \text{if } -y > V_{TH} \end{cases} . \tag{A5}$$

Suppose that the normalization is performed using the fundamental frequency w_0 and associated parameters defined in (A6).

$$\rho_0 = \sqrt{\frac{L_1}{C_{eq}}}, \quad \omega_0 = \frac{1}{\sqrt{L_1 \cdot C_{eq}}}, \quad C_{eq} = \frac{C_1 \cdot C_2}{C_1 + C_2}, \quad \tau_0 = \omega_0 \cdot t \ . \tag{A6}$$

The first step of deriving the normalized equations in this case is outlined in (A7). The step is nearly identical to (A2).

$$\begin{cases} \dfrac{dv_{C1}}{d\tau_0} \cdot \omega_0 = \dfrac{i_L - \beta \cdot i_B}{C_1} \cdot \dfrac{\rho_0}{\rho_0} \\ \dfrac{dv_{C2}}{d\tau_0} \cdot \omega_0 = \dfrac{V_3 - v_{C2} - V_1}{R_1 \cdot C_2 \cdot \dfrac{\rho_0}{\rho_0}} + \dfrac{i_L + i_B}{C_2} \cdot \dfrac{\rho_0}{\rho_0} \\ \dfrac{di_L}{d\tau_0} \cdot \omega_0 \cdot \dfrac{\rho_0}{\rho_0} = \dfrac{V_2 - v_{C1} + V_3 - v_{C2}}{L_1} - i_L \cdot \dfrac{R_L}{L_1} \cdot \dfrac{\rho_0}{\rho_0} \end{cases} . \tag{A7}$$

In order to understand how the two normalizations relate to one another, first, it is important to derive how the new parameters in (A6) relate to parameters in (A1). This is demonstrated in (A8). The equation clearly demonstrates that the parameters relate via the multiplication with a constant $S = \sqrt{\dfrac{(C_1 + C_2)}{C_2}}$.

$$\begin{aligned} \rho_0 &= \sqrt{\frac{L_1}{C_{eq}}} = \sqrt{\frac{L \cdot (C_1 + C_2)}{C_1 \cdot C_2}} = \sqrt{\frac{L_1}{C_1}} \cdot \sqrt{\frac{(C_1 + C_2)}{C_2}} = \rho_1 \cdot S. \\ \omega_0 &= \frac{1}{\sqrt{L_1 \cdot C_{eq}}} = \frac{1}{\sqrt{L_1 \cdot \dfrac{C_1 \cdot C_2}{C_1 + C_2}}} = \frac{1}{\sqrt{L_1 \cdot C_1}} \cdot \frac{1}{\sqrt{\dfrac{C_2}{C_1 + C_2}}} = \omega_1 \cdot S. \\ \tau_0 &= \omega_0 \cdot t = \omega_1 \cdot \sqrt{\frac{(C_1 + C_2)}{C_2}} \cdot t = \tau_1 \cdot S. \end{aligned} \tag{A8}$$

Next, the parameters from (A8) are used in (A7), resulting in

$$\begin{cases} \dfrac{dv_{C1}}{d\tau_1} \cdot \omega_1 \cdot S = \dfrac{i_L - \beta \cdot i_B}{C_1} \cdot \dfrac{\rho_1 \cdot S}{\rho_1 \cdot S} \\ \dfrac{dv_{C2}}{d\tau_1} \cdot \omega_1 \cdot S = \dfrac{V_3 - v_{C2} - V_1}{R_1 \cdot C_2 \cdot \dfrac{\rho_1 \cdot S}{\rho_1 \cdot S}} + \dfrac{i_L + i_B}{C_2} \cdot \dfrac{\rho_1 \cdot S}{\rho_1 \cdot S} \\ \dfrac{di_L}{d\tau_1} \cdot \omega_1 \cdot S \cdot \dfrac{\rho_1 \cdot S}{\rho_1 \cdot S} = \dfrac{V_2 - v_{C1} + V_3 - v_{C2}}{L_1} - i_L \cdot \dfrac{R_L}{L_1} \cdot \dfrac{\rho_1 \cdot S}{\rho_1 \cdot S} \end{cases} . \tag{A9}$$

Finally, the equation is then simplified, resulting in (A10). It is clear that by comparing the equation in (A4) normalized for the characteristic frequency ω_1 and the normalized equation in (A10) normalized for the fundamental frequency ω_0 and adjusted with respect to the characteristic frequency ω_1, the only difference is the additional multiplication with the S constant.

$$\begin{cases} \dfrac{dv_{C1}}{d\tau_1} \cdot \omega_1 \cdot S = \dfrac{i_L - \beta \cdot i_B}{C_1} \cdot \dfrac{\rho_1}{\rho_1} \\ \dfrac{dv_{C2}}{d\tau_1} \cdot \omega_1 \cdot S = \dfrac{V_3 - v_{C2} - V_1}{R_1 \cdot C_2 \cdot \dfrac{\rho_1}{\rho_1}} + \dfrac{i_L + i_B}{C_2} \cdot \dfrac{\rho_1}{\rho_1} \\ \dfrac{di_L}{d\tau_1} \cdot \omega_1 \cdot S \cdot \dfrac{\rho_1}{\rho_1} = \dfrac{V_2 - v_{C1} + V_3 - v_{C2}}{L_1} - i_L \cdot \dfrac{R_L}{L_1} \cdot \dfrac{\rho_1}{\rho_1} \end{cases} . \tag{A10}$$

Next, the (A3) parameters are introduced and the final form of the normalized equations is acquired:

$$\begin{cases} \dfrac{\mathrm{d}x}{\mathrm{d}\tau_1} = \left(z - \beta \cdot \tilde{i}_B\right) \cdot \dfrac{1}{S} \\ \dfrac{\mathrm{d}y}{\mathrm{d}\tau_1} = \left(-\dfrac{V_3 - y - V_1}{\tilde{R}_1 \cdot \epsilon} + \dfrac{z + \tilde{i}_B}{\epsilon}\right) \cdot \dfrac{1}{S} \\ \dfrac{\mathrm{d}z}{\mathrm{d}\tau_1} = \left(V_2 - x + V_3 - y - z \cdot \tilde{R}_L\right) \cdot \dfrac{1}{S} \end{cases} . \tag{A11}$$

The next step compares the two normalized equations with the Euler–Cromer numerical integration applied to acquire the approximate discrete solution for the integration step $\Delta\theta$. The equation for the characteristic frequency ω_1 is in (A12), while for the fundamental frequency ω_0 is in (A13).

$$\begin{cases} \underbrace{x_{n+1}}_{\text{Next value}} = \underbrace{x_n}_{\text{Current value}} + \underbrace{\left(z_n - \beta \cdot \tilde{i}_B\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{y_{n+1}}_{\text{Next value}} = \underbrace{y_n}_{\text{Current value}} + \underbrace{\left(\dfrac{V_3 - y_n - V_1}{\tilde{R}_1 \cdot \epsilon} + \dfrac{z_n + \tilde{i}_B}{\epsilon}\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{z_{n+1}}_{\text{Next value}} = \underbrace{z_n}_{\text{Current value}} + \underbrace{\left(V_2 - x_n + V_3 - y_n - z_n \cdot \tilde{R}_L\right)}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \end{cases} . \tag{A12}$$

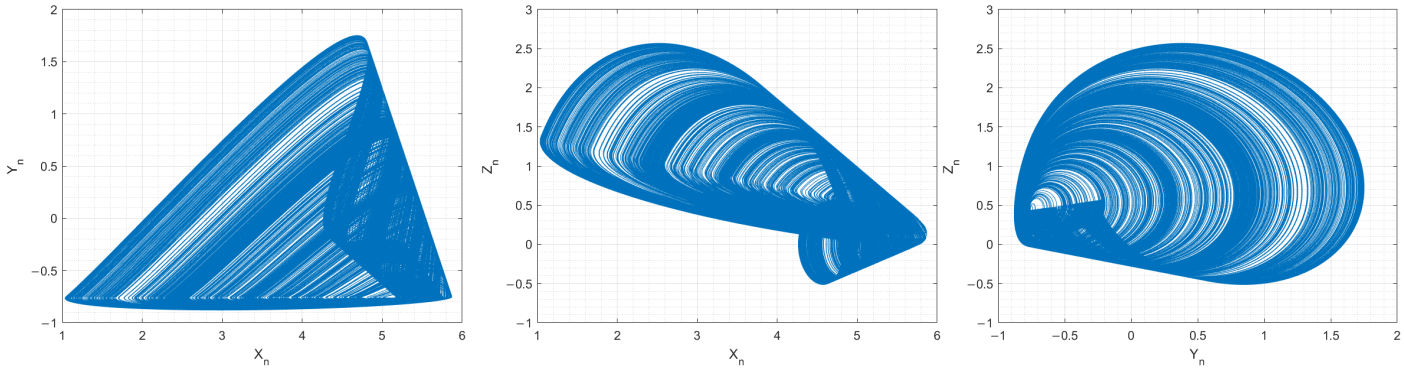
$$\begin{cases} \underbrace{x_{n+1}}_{\text{Next value}} = \underbrace{x_n}_{\text{Current value}} + \underbrace{\left(z_n - \beta \cdot \tilde{i}_B\right) \cdot \dfrac{1}{S}}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{y_{n+1}}_{\text{Next value}} = \underbrace{y_n}_{\text{Current value}} + \underbrace{\left(\dfrac{V_3 - y_n - V_1}{\tilde{R}_1 \cdot \epsilon} + \dfrac{z_n + \tilde{i}_B}{\epsilon}\right) \cdot \dfrac{1}{S}}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \\ \underbrace{z_{n+1}}_{\text{Next value}} = \underbrace{z_n}_{\text{Current value}} + \underbrace{\left(V_2 - x_n + V_3 - y_n - z_n \cdot \tilde{R}_L\right) \cdot \dfrac{1}{S}}_{\text{Derivative}} \cdot \underbrace{\Delta\theta}_{\text{Time step}} \end{cases} . \tag{A13}$$

It is clear that the change in the normalization frequency in the same discrete time yields only an additional constant. To prove that this does not affect the chaotic dynamic, a MATLAB script is created to perform numeric simulations of systems in (A12) and (A13). The chaotic attractors of the two systems are presented in Figures A1 and A2. The waveforms of the x state variable in the two cases are demonstrated in Figure A3.

From the Figures A1–A3, it is apparent that the chaotic dynamic is preserved if the normalization frequency is changed. The attractors in the two cases match and the only difference is that the signals are stretched in time relative to each other, which is expected, knowing that changing normalization frequency only affects the time scale.

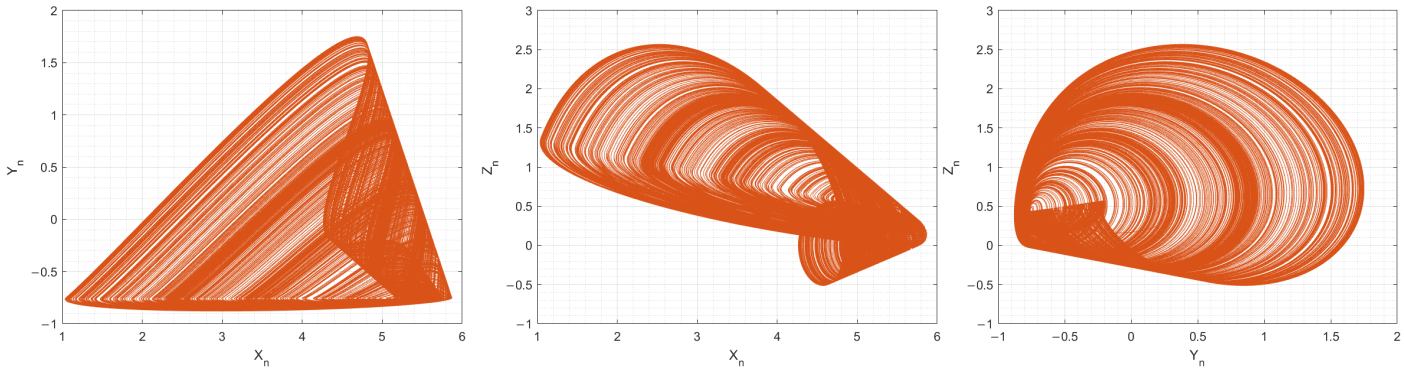
It is important to note that the end goal of such transformations in this case is implementing the discrete time model of the oscillator in a digital system (FPGA in this case) and matching the frequency of the digital oscillator to one of the analog oscillator. The digital oscillator has two time-related parameters that can be adjusted—the clock frequency f_{clk} and the time step $\Delta\theta$. If the clock frequency is set, for digital chaos oscillator to match the analog oscillator, the time step must be the relation of the frequency of normalization to the clock frequency. In the case if the characteristic frequency is used, $\Delta\theta_1 = \dfrac{f_1}{f_{clk}}$ if the fundamental frequency is used to normalized equation, then $\Delta\theta_0 = \dfrac{f_0}{f_{clk}}$ (in this case

the equation has the additional multiplication constant $\frac{1}{S}$). The relation of $\Delta\theta_1$ and $\Delta\theta_0$ is $\frac{1}{S}$. It is apparent that whether normalization is performed using ω_1 or ω_0 for the digital implementation, the time step is selected with respect to the scaling frequency, thus the frequency of the digital oscillator matches the frequency of the analog oscillator.



(**a**) (**b**) (**c**)

Figure A1. x, y (**a**), x, z (**b**) and y, z (**c**) attractor projections of the Colpitts chaos oscillator normalized for ω_1.



(**a**) (**b**) (**c**)

Figure A2. x, y (**a**), x, z (**b**) and y, z (**c**) attractor projections of the Colpitts chaos oscillator normalized for ω_0.

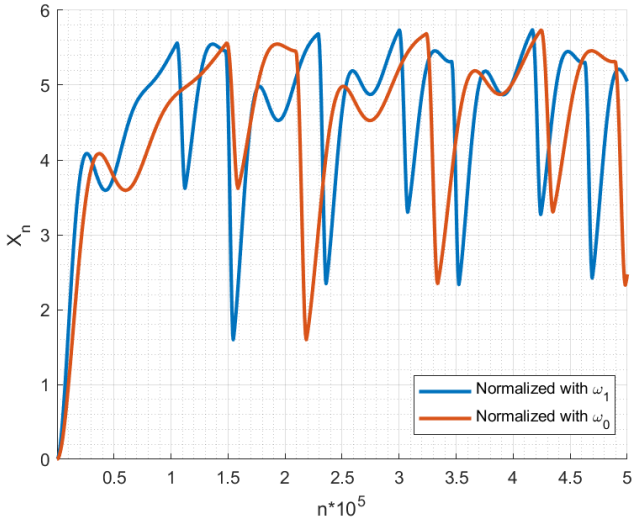


Figure A3. Normalized time diagram of x state variable in the case of ω_1 and ω_0 normalizations in discrete time.

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