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Device-Aware Test for Threshold Voltage Shifting in FeFET

Changhao Wang † §, Sicong Yuan*, Nima Kolahimahmoudi†, Hanzhi Xun*, Nicolò Bellarmino†
Danyang Chen ‡, Chujun Yin§, Mottaqiallah Taouil*, Moritz Fieback*, Xiuyan Li ‡
Lin Wang ‡, Chaobo Li §, Riccardo Cantoro†, Said Hamdioui*
† Politecnico di Torino, Torino, Italy *TUDelft, Delft, The Netherlands ‡Shanghai Jiao Tong University, Shanghai, China
§Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
Email: {changhao.wang,nima.kolahi nicolo.bellarmino, riccardo.cantoro}@polito.it { lichaobo, yinchujun}@ime.ac.cn
{S.Yuan-4, M.C.R.Fieback, H.Xun, M.Taouil, S.Hamdioui}@tudelft.nl {linwang, c19970528, xiuyanli}@sjtu.edu.cn

***Abstract*—Ferroelectric Field-Effect Transistors (FeFETs) are promising candidates for non-volatile memory (NVM) technologies, especially in embedded systems and edge computing. However, due to their physical characteristics, FeFETs exhibit unique defects—such as Threshold Voltage Shifting (TVS) caused by trap charges in the oxide layer—that are not captured by conventional defect models. This study adopts the Device-Aware Test (DAT) methodology to model these defects by incorporating their impact into the electrical parameters, calibrated using measurement data. Defect injection, circuit-level simulations, and fault analysis are performed to derive realistic fault models. Finally, the March algorithm and Design-for-Test (DfT) techniques are proposed to effectively detect these defects.**

***Index Terms*—Memory test, FeFET, device-aware test, defect modeling**

I. Introduction

Ferroelectric Field-Effect Transistors (FeFETs) are promising for next-generation non-volatile memory due to their high speed and CMOS compatibility, but their performance can be degraded by unique physical defects [1]. Traditional resistor-based defect models are insufficient for FeFETs, necessitating more accurate, device-aware test (DAT) methods that consider the impact of technological parameters on device behavior. Applying DAT enables the development of efficient, low-escape test solutions crucial for high-volume FeFET production [2, 3].

In this paper, we present the results of the characterization of some defective FeFETs showing 'Threshold Voltage Shifting' (TVS) in their behavior. We apply the DAT method to develop a specific defect model for testing. This model is calibrated using *empirical* data and is then utilized for fault modeling and test generation. The main contributions of this paper are as follows:

- Characterize defective FeFETs resulting in TVS.
- Design a device-aware defect model for such defective FeFET and calibrate it with data from real devices.
- Develop realistic fault models based on circuit-level simulations and introduce the testing solution to detect the defects.

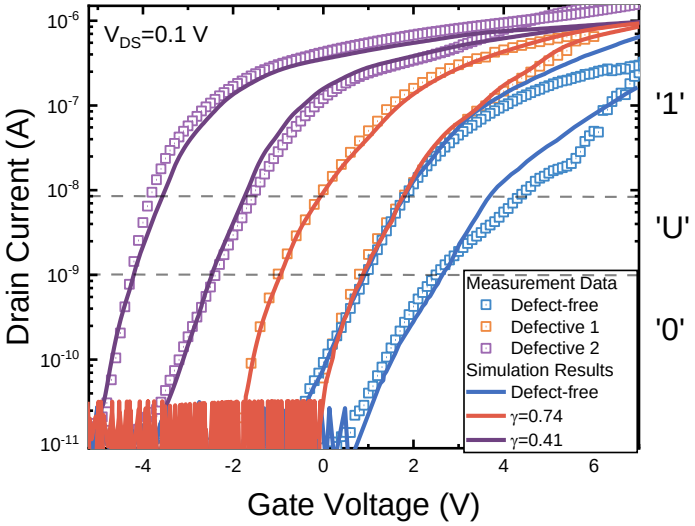


Fig. 1: Measurement and fitting of defective I_d–V_g under the same conditions. The parameter γ is introduced in Equations 5-6 and denotes a specific, time-independent defect strength for each device.

II. Defect Characterization

A. Characterization of TVS

The detailed fabrication processes of FeFET devices under evaluation are available in [4]. The I_d/V_g measurements of one defect-free and two defective FeFETs are shown in Figure 1 (the first bipolar cycling after the wake-up process), where the points represent the measurement results of the real devices. All three devices shown in Figure 1 were subjected to the same cycling and measurement conditions. The gate voltage (V_g) was swept from $-6\,\mathrm{V}$ to $6\,\mathrm{V}$ and back to $-6\,\mathrm{V}$ with a step size of $0.1\,\mathrm{V}$, while the source-drain voltage (V_{DS}) was maintained at $100\,\mathrm{mV}$. Defective devices exhibit significant threshold voltage shifts, as indicated by the orange ($-1.8\,\mathrm{V}$) and red ($-5.0\,\mathrm{V}$) curves, compared to the defect-free device (blue). Both high and low V_{th} values shift simultaneously, while the memory window (MW) remains largely unchanged. Variations in the on-state current (I_{on}) are also observed, but

due to the sufficiently large I_{on}/I_{off} ratio, these variations have minimal impact on circuit performance. This study primarily focuses on the threshold voltage shifting (TVS) phenomenon.

B. Mechanism

The defective TVS phenomenon in FeFETs primarily arises from trap states (Q_t) within the oxide and ferroelectric (FE) layers, which capture and retain electrons or holes due to crystallographic defects, impurities, or fabrication-induced imperfections [5, 6]. These traps can be located in both the oxide and FE layers, and some Q_t are unrelated to ferroelectric polarization [7]. The increased density of traps raises the surface potential, which promotes channel formation and decreases the threshold voltage in both the low threshold voltage (LVT, corresponding to the "1" state) and high threshold voltage (HTV, corresponding to the "0" state) conditions, resulting in similar shifts of the current curves and minimal change in MW [8]. However, practical devices may also exhibit traps coupled with the FE layer, leading to MW fluctuations. So this mechanism represents the dominant but not the sole cause of the TVS phenomenon [9].

III. Device-aware defect modeling of TVS

A. Defect-free FeFET model

The defect-free FeFET model is designed based on the Preisach model [10]. As illustrated in Figure 2(a), the model consists of two components: (1) the conventional MOSFET, which is described using the BSIM4 model [11], and (2) the FE layer, which is modeled as a capacitor. Given that the FE layer is incorporated into the MOSFET gate stack, it is necessary to solve both the charge conservation (Equation 1) and voltage division (Equation 2) equations concurrently [10]:

$$Q_{\text{MOS}} = Q_{\text{FE}} \tag{1}$$

$$V_g = V_{\text{FE}} + V_{\text{MOS}} \tag{2}$$

Here, Q_{FE} denotes the polarization charge in the FE layer, while Q_{MOS} represents the charge in the MOSFET channel. V_g is the externally applied gate voltage, V_{FE} is the voltage drop across the FE layer, and V_{MOS} is the voltage drop across the MOSFET structure. The detailed relationship between Q_{MOS} and V_{MOS} is provided by the BSIM4 model [11].

The two states ('0' and '1') of the FeFET are determined by the polarization direction of the FE layer. When the FE polarization is downward, the voltage drop across the FE layer (V_{FE}) becomes relatively small, resulting in a larger voltage across the MOSFET component (V_{MOS}) which is sufficient to open the channel. In this case, the FeFET operates in the LVT state. However, when the polarization reverses, V_{MOS} decreases and is insufficient to open the channel, leading to no channel current. This corresponds to the HVT state. Typically, the V_{MOS} required to activate the MOSFET channel is referred to as V_{th-MOS}, and its expression is given as follows:

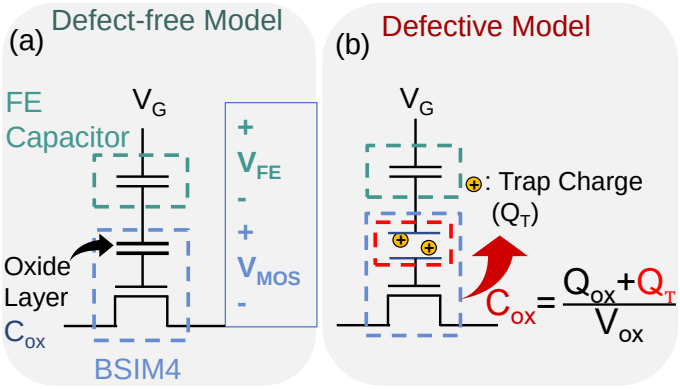


Fig. 2: (a) Defect-free model consists of two components: the FE capacitor and the BSIM4 model; (b) defective model corresponds to an increased capacitance of the oxide layer.

$$V_{th-MOS} = V_{FB} + 2 \times \phi_f + \frac{\sqrt{4 \times q_e N_a \epsilon_s \epsilon_0 \phi_f}}{C_{ox}} \tag{3}$$

TABLE I: MOSFET PARAMETERS.

V_{FB}	Flatband voltage	ϕ_s	Surface potential
C_{ox}	Oxide capacitance	V_{DS}	Drain-source voltage
ϕ_f	Fermi potential	q_e	Elementary charge
N_a	Acceptor concentration	ϵ_s	Dielectric constant
ϵ_0	Permittivity of free space		

Table I provides a comprehensive set of parameters used in Equation 3. Building on these definitions, a defect-free FeFET model was developed and programmed in Verilog-A. The model was calibrated against experimental data, as depicted in the blue curves of Figure 1.

B. Physical defect modeling

The primary factor contributing to TVS arises from traps that are independent of the FE layer. Consequently, Figure 2(b) depicts the physical defect model, wherein the traps affect channel formation. To facilitate quantitative analysis, λ is introduced to denote the relative magnitude of these traps. Because the oxide layer in a MOSFET functions as a capacitor, the expression for the defective thin-oxide capacitance is presented as follows:

$$C_{ox} = \frac{Q_{ox} + Q_T}{V_{ox}} = \frac{Q_{ox} \times (1+\lambda)}{V_{ox}}, \lambda >= 0 \tag{4}$$

In this formulation, Q_{ox} is the charge contained in the oxide layer, V_{ox} is the voltage across the oxide layer, and Q_T represents traps. The effective oxide layer capacitance increases in the presence of traps, as these defects create additional charge-storage sites and thus enhance the oxide's overall capacity. When $\lambda = 0$, the device is defect-free, whereas a λ value exceeding zero indicates a physical defect.

TABLE II: FAULT PRIMITIVE NOTATION.

⟨S/F/R⟩	Explanation	Value
S	Sensitizing sequence	0, 1, 0w0, 0w1, 1w0, 1w1, 0r0, 1r1
F	Faulty effect	L, 0, U, 1, H
R	Readout value	0, 1, ?, -

Note in 'F':			
'L'	Extreme high V_{th} state	'0'	High V_{th} state
'U'	V_{th} undefined state	'1'	Low V_{th} state
'H'	Extreme low V_{th} state		

Note in 'R':			
'0'	Readout low state	'1'	Readout high state
'?'	Readout random state	'-'	Readout not applicable

C. Electrical defect modeling

According to the analysis, trap charges increase C_{ox}, thereby affecting V_{th-MOS} as indicated by Equation 3. Because values of λ ranging from 1 to infinity are unsuitable for modeling and analyzing, γ is introduced to characterize the defect effect, with γ linked to λ through Equation 5. Consequently, the electrical defect model for V_{th} is formulated in Equation 6, which modifies Equation 3 to capture the MOSFET component's V_{th-MOS}:

$$\gamma = \frac{1}{1+\lambda}, \quad 0 < \gamma \leq 1 \tag{5}$$

$$V_{th-MOS} = V_{FB} + 2 \times \phi_f + \frac{\gamma \times \sqrt{4 \times q_e N_a \epsilon_s \epsilon_0 \phi_f}}{C_{ox}} \tag{6}$$

The first two terms in Equation 6, V_{FB} and ϕ_f, are mainly determined by material properties. In this context, γ designates the defect strength: $\gamma = 1$ indicates a defect-free FeFET. As γ decreases, it indicates an increase in oxide layer traps.

Equation 6 represents V_{th-MOS}, the threshold voltage of the MOSFET component, which corresponds to V_{MOS}. Meanwhile, V_{th} denotes the threshold voltage of the FeFET, corresponding to V_g. Besides, Equation 6 applies to both the LVT and HVT states of the FeFET.

D. Model optimization

Equation 6 is implemented in Verilog-A in conjunction with the Preisach FeFET model [10]. The fitting process for the defective FeFET model involves two steps: (1) The defect-free FeFET is fitted by setting $\gamma = 1$, ensuring an accurate baseline model. (2) The defective FeFET is fitted by adjusting the defect strength parameter (γ).

Figure 1 presents the fitting results for both defect-free and defective devices. $V_{DS} = 0.1\,\text{V}$ is applied. The points represent experimental measurements: the blue points correspond to the defect-free device, while the orange and purple points represent defective devices. The blue line depicts the simulated defect-free model with $\gamma = 1$, serving as the reference. As γ decreases, V_{th} shifts downward, causing the transfer curve to move left. Specifically, when $\gamma = 0.74$ and $\gamma = 0.41$, the simulated curves align with the experimental data of defective devices 1 and 2, respectively.

TABLE III: FAULT ANALYSIS RESULTS.

γ	**Negative** TVS Faults	Type
[1, 0.91)	Fault-free	-
[0.91, 0.73)	$< 1w0/U/- >$	HtD
	$< 0w0/U/- >$	
	$< 0r0/U/? >$	
	$< 0/U/- >$	
[0.73, 0)	$< 0/1/- >$	EtD
	$< 1w0/1/- >$	
	$< 0w0/1/- >$	
	$< 0r0/1/1 >$	

IV. Device-aware fault modeling of TVS

A. Fault space definition

Fault primitive (FP) notations are used to describe memory faults [12] (see Table II): $\langle S/F/R \rangle$, where S denotes the sensitizing sequence, F denotes the faulty effect, and R denotes the readout value. The symbol '?' indicates a random read outcome, and the symbol '$-$' denotes the case where the last performed operation in the cell is not a read operation. Based on whether the faults can be sensitized by regular write/read operations, they are categorized as *Easy-to-Detect (EtD)* or *Hard-to-Detect (HtD)* [13]. EtD faults can be guaranteed to be sensitized and detected by regular memory operations. In contrast, HtD faults lead to ambiguous readout states, making their detection more challenging.

B. Simulation set-up

Cadence Spectre is employed for circuit-level simulations. The simulation circuit consists of a 3×3 FeFET array, as illustrated in [14]. Both write and read operations use pulses of $20\,\mu\text{s}$ duration: the write pulse has an amplitude of $\pm 8\,\text{V}$, and the read pulse has an amplitude of $2\,\text{V}$. In each simulation, only one defect with a specific strength (γ value) is injected by substituting the defect-free model at the center of the array with a developed defective model. The defect strength is introduced by varying γ from 0 to 1.

C. Fault modeling and analysis

Table III summarizes the results of fault analysis. The negative TVS primarily affects the '0' state. As γ ranges from 0.73 to 0.91, write and read operations on the '0' state (e.g., $\langle 1w0 \rangle, \langle 0w0 \rangle$) can transition to an undefined state 'U', making it difficult for the reading circuitry to reliably retrieve the correct value. At this stage, the fault is classified as *HtD* because it may not be sensitized using regular read/write operations. As γ continues to decrease, the stored '0' may be erroneously read as '1', ultimately leading to complete memory failure. Once the stored value has flipped, regular operations can sensitize the fault, and such faults are then categorized as *EtD*.

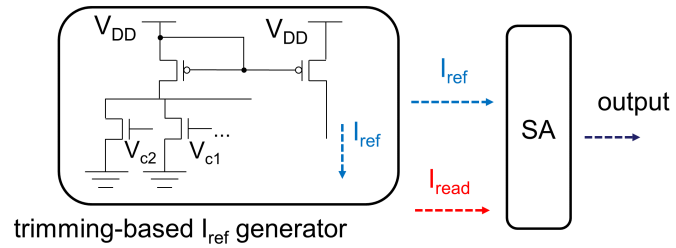


Fig. 3: DfT method for detecting TVS-induced faults. γ value remains constant for each defect strength during the test.

V. Test Generation

A. March test

From Table III, it is evident that TVS-induced faults mainly affect the '0' state. Therefore, a straightforward detection strategy is to apply the following March test algorithm, ensuring coverage of all *EtD* faults.

$$\text{March-TVS} = \{\Updownarrow (w1); \Updownarrow (w0, r0)\} \tag{7}$$

Here, $\Updownarrow$ denotes an irrelevant addressing direction. The first step in the algorithm initializes all memory cells to the '1' state. Next, a $w0$ operation is performed, followed by a read operation. *EtD* faults can be detected by the read values. However, when the defect strength is insufficient to cause a change in the readout, leaving the stored value in a 'U' state, the March algorithm does not reliably detect the fault.

B. DfT method

Given the faults outlined in Table III, the primary objective of the DfT approach is to detect the 'U' state. A commonly adopted DfT architecture for identifying specific resistance states is the trimming-based sensing circuit, as introduced in [3] and illustrated in Figure 3. This structure enables the generation of programmable reference currents (I_{ref}) by selecting different control voltages V_{ci} (where $i = 1, 2, \ldots$), which are applied to a current-generation subcircuit. Each V_{ci} corresponds to a specific I_{ref} value, allowing fine granularity in setting the detection threshold. The primary function of this architecture is to compare the read current (I_{read}), which is obtained from the FeFET during a sensing operation, against these selectable I_{ref} values. The comparison allows for an accurate determination of the FeFET channel resistance.

The DfT detection process involves a sequence of three steps to ensure reliable defect detection. In the first step, a post-fabrication calibration phase is conducted to identify the most appropriate reference current I_{ref}, which corresponds to the boundary condition between the ambiguous or undefined state ('U') and the logic '0' state. This calibration step is critical, as it defines the detection sensitivity of the system. In the second step, all FeFETs under test are initialized into the logic '0' state. Finally, as the third step, a read operation is performed wherein the actual read current I_{read} from each FeFET is measured and compared against the pre-selected I_{ref}. If the measured I_{read} exceeds the calibrated threshold, indicating that the channel resistance corresponds to the undefined 'U' state, the FeFET is flagged as defective due to TVS.

This trimming-based DfT technique offers a highly time-efficient approach, capable of achieving 100% detection coverage for TVS-related defects, owing to its precise and programmable current thresholding mechanism. However, it is important to note that the implementation of such a structure necessitates additional on-chip resources, particularly for the trimming and calibration circuitry, which can increase the overall silicon area and design complexity. In this design, a total of 27 additional transistors are introduced.

VI. Conclusion

In this work, we experimentally identified TVS-related defects in FeFETs by observing simultaneous shifts in both low and high V_{th}. We developed and calibrated a compact defect model based on these findings. Next, circuit-level simulations based on the calibrated defect model were performed, yielding realistic fault models. Finally, we proposed a comprehensive test solution, combining a March test for EtD faults and a DfT circuit for HtD faults.

References

[1] S. Hamdioui *et al.*, "An experimental analysis of spot defects in srams: Realistic fault models and tests," in *Proceedings of the Ninth Asian Test Symposium*, IEEE, 2000, pp. 131–138.

[2] D. Thapar *et al.*, "Analysis and characterization of defects in fefets," in *2023 IEEE International Test Conference (ITC)*, IEEE, 2023, pp. 256–265.

[3] S. Yuan *et al.*, "Device-aware test for anomalous charge trapping in fefets," in *30th Asia and South Pacific Design Automation Conference ASP-DAC 2025*, ACM, vol. 30, 2024.

[4] T. Cui *et al.*, "Can interface layer be really free for hf x zr 1-x o 2 based ferroelectric field-effect transistors with oxide semiconductor channel?" *IEEE Electron Device Letters*, 2024.

[5] P. Jacob *et al.*, "A comparative study of n- and p-channel FeFETs with ferroelectric HZO gate dielectric," *Solids*, vol. 4, no. 4, pp. 356–367, Dec. 1, 2023.

[6] S. Deng *et al.*, "Unraveling the dynamics of charge trapping and de-trapping in ferroelectric fets," *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 1503–1511, 2022.

[7] R. Ichihara *et al.*, "Accurate picture of cycling degradation in hfo 2-fefet based on charge trapping dynamics revealed by fast charge centroid analysis," in *2021 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2021, pp. 6–3.

[8] S. Beyer *et al.*, "Charge trapping challenges of cmos embedded complementary fefets," in *2024 IEEE International Memory Workshop (IMW)*, IEEE, 2024, pp. 1–4.

[9] Z. Chen *et al.*, "Novel design strategy for high-endurance ($>10\{10\}$) and fast-erase oxide-semiconductor channel fefet," in *2024 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2024, pp. 1–4.

[10] K. Ni *et al.*, "A Circuit Compatible Accurate Compact Model for Ferroelectric-FETs," in *2018 IEEE Symposium on VLSI Technology*, ISSN: 2158-9682, Jun. 2018, pp. 131–132.

[11] B. Shen, "Bsim: Berkeley short-channel igfet model for mos transistors," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 308–331, 1984.

[12] L. Wu *et al.*, "Electrical Modeling of STT-MRAM Defects," en, in *2018 IEEE International Test Conference (ITC)*, Phoenix, AZ, USA: IEEE, Oct. 2018, pp. 1–10.

[13] M. Fieback *et al.*, "Testing Resistive Memories: Where are We and What is Missing?" en, in *2018 IEEE International Test Conference (ITC)*, Phoenix, AZ, USA: IEEE, Oct. 2018, pp. 1–9.

[14] C. Wang *et al.*, "Defects, fault modeling, and test development framework for fefets," in *2024 IEEE International Test Conference (ITC)*, IEEE, 2024, pp. 91–95.