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Original
Susceptibility to RFI of Monolithic GaN Current Sources / Carastro, F., Lena, D., Fiori, F.. - STAMPA. - (2025), pp. 757-762. (2025 International Symposium on Electromagnetic Compatibility (EMC Europe) Parigi (Fra) 1-5 September 2025) [10.1109/EMCEurope61644.2025.11176201].

Availability:
This version is available at: 11583/3003265 since: 2025-09-23T12:09:28Z

Publisher:
IEEE

Published
DOI:10.1109/EMCEurope61644.2025.11176201

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26 November 2026

Susceptibility to RFI of Monolithic GaN Current Sources

Filippo Carastro[#], Davide Lena[$], Franco Fiori[#]
[#]Electronics and Telecommunications Dpt. (DET), Politecnico di Torino, Italy
[$]STMicroelectronics s.r.l., Italy
{filippo.carastro, franco.fiori}@polito.it, davide.lena@st.com

***Abstract*— This paper investigates the demodulation of radio-frequency interference (RFI) in two different topologies of current sources implemented in monolithic GaN technology. An analytical model is developed which relates transistor nonlinearities to circuit parasitics. It is then used to design RFI-immune current sources. Simulation results demonstrate the effectiveness of these designs, showing a significant reduction in the output offset current from approximately 10μA to 200nA when subjected to 1V amplitude, 1GHz interference signal.**

***Keywords*— DC current sources, GaN integrated circuits, Electromagnetic interference (EMI), electromagnetic susceptibility.**

I. Introduction

In recent years, the electric vehicle (EV) industry has grown exponentially, leading to a significant increase in the importance of EV power systems. Crucial components of electric vehicles are the DC-DC converters, which include analog signal processing blocks, such as operational amplifiers, voltage references, and comparator circuits. Although, these blocks are implemented in integrated circuits (ICs) using high voltage BCD (bipolar, CMOS, DMOS) technologies, they have limitations in current capability and temperature range.

On vice versa, Gallium Nitride shows higher breakdown field, good mobility and higher carrier density. These features make it suitable to build up monolithic high voltage ICs working at higher temperature. According to [1], GaN-based circuits can operate stably up to 250 °C, while the maximum operating temperature of silicon based device is limited to 150 °C.

The interest in monolithic GaN is further supported by the p-GaN solution's favorable balance between reliability and cost. The integration of high-voltage power devices and low-voltage (12 V) peripheral devices on the same substrate is a recent development in the field, although it is well established in BCD technology. A schematic cross-section of the p-GaN technology considered in this work is shown in Fig. 1.

Current sources are fundamental basic cells necessary to design the front-end of analog and digital function blocks. In particular, these circuits are essential in operational amplifier [2], [3], voltage reference [4], [5] and comparator circuits[6], [7].

This publication is part of the project PNRR-NGEU which has received funding from the MUR-DM 117/2023.

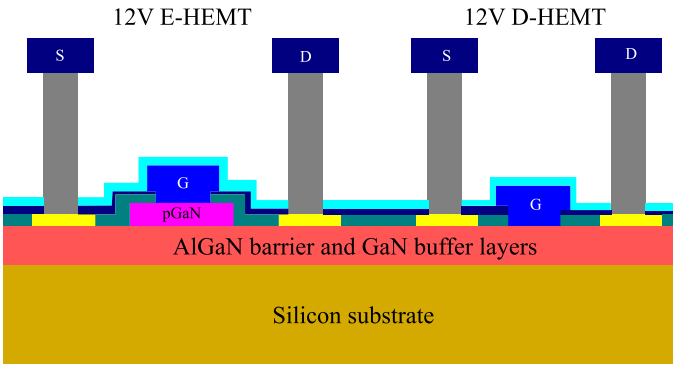


Fig. 1. Schematic of GaN monolithic cross section.

Smart power devices, widely used in electronic modules, are vulnerable to electromagnetic interference (EMI) arising from radio transmitters or commutation circuits [8]. The cables used to connect these modules to power loads act as unintended antennas, converting EMI into disturbance signals that corrupt the nominal ones. This interference can compromise the correct operation of the front-end circuits. Current sources are primarily used for biasing transistors. Therefore, if an operational amplifier's differential stage is affected by electromagnetic interference (EMI), the disturbance will be demodulated and added to nominal input signals, corrupting the nominal output signal with in-band interference. In literature, the demodulation of radio frequency interference (RFI) in electronic circuits has been widely investigated, and design techniques to mitigate RFI in CMOS and bipolar integrated circuits (ICs) has been proposed in [9], [10], [11]. However, to the authors' knowledge, the demodulation of EMI in GaN circuit has not yet been investigated.

In this paper, the demodulation of EMI in two different current source topologies is investigated, and an analytical model is proposed. In addition, some solutions to increase the immunity to RFI are evaluated.

The paper is organized as follows: Section II presents an overview of current source topologies in GaN technology. Section III provides a detailed analysis of RF signal demodulation within current sources and presents the proposed analytical model. Section IV reports the solutions designed for improving RFI immunity. Finally, Section V presents the simulation results.

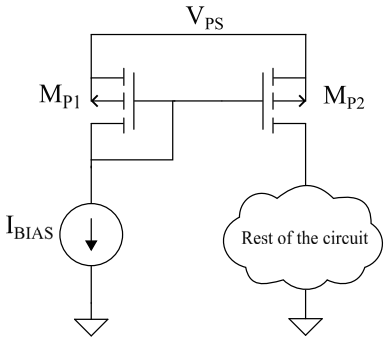


Fig. 2. Schematic of a traditional current mirror implemented with PMOS.

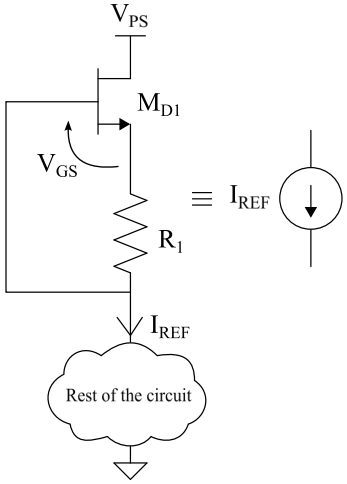


Fig. 3. Schematic of basic current generator implemented in [3].

II. Current sources in GaN technology

In CMOS technology DC current sources can be implemented by means of current mirrors. In particular, upper side mirrors, are implemented with pMOS like that shown in Fig. 2. The reference current is provided by a precise and stable current generator (I_{BIAS} in Fig. 2). At the output, the current mirror provides a bias current to the rest of the circuit. The main parameters featuring current sources are the output resistance and the output voltage swing. In particular, high output resistance and large voltage swing are useful. Unfortunately, common GaN technologies do not include a complementary device, meaning a p-GaN transistor, therefore complementary current mirrors are not available and self-biased topologies like the one shown in Fig. 3 must be used. The circuit is composed of two devices, the depletion mode GaN (d-GaN) M_{D1} and the resistor R_1. A d-GaN transistor is a normally-on device with a negative threshold voltage, whereas an enhancement mode GaN (e-GaN) has a positive threshold voltage [12]. Its drain terminal is connected to the power supply (V_{PS}), while the other terminals to the resistor.

In order to regulate drain-source current in GaN transistors, the gate-source voltage (V_{GS} in Fig. 3) is modulated. This modulation forms the core operational principle of the current source, which relies on a feedback mechanism between the

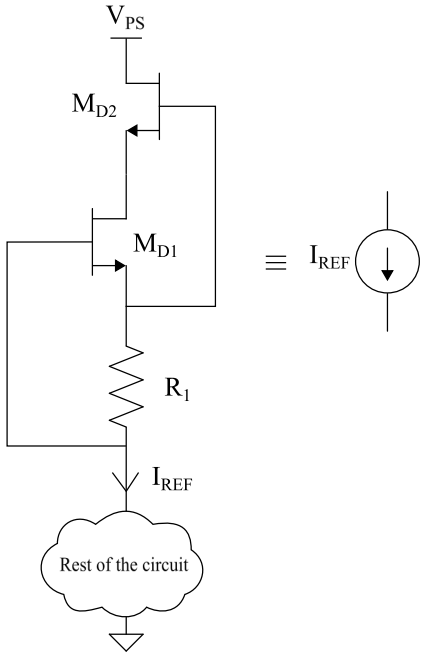


Fig. 4. Schematic of cascode current generator implemented in [2].

resistor current and V_{GS}. Specifically, the gate terminal is directly connected to the output voltage. Due to the voltage drop across resistor R_1, the source terminal is maintained at a potential higher than the output. Consequently, when channel current flows through R_1, the V_{GS} of the d-GaN becomes negative (V_{GS} < 0). This resistor provides a feedback voltage that self-biases the gate, ensuring a stable drain current despite fluctuations in the drain-source voltage. Current stability occurs as V_{GS} approaches the transistor's threshold voltage, ultimately determining the output current expressed as

$$I_{\mathrm{REF}} \approx -\frac{V_{\mathrm{TH}}}{R_1}, \tag{1}$$

where V_{TH} is the threshold voltage of the d-GaN transistor. The d-GaN uses the voltage drop across resistor (V_{GS}) to set the gate-source bias voltage and therefore the channel current.

An increase in the resistive value of R_1 will result in a reduction of the channel drain current, denoted as I_{D1}.

The output resistance obtained from the small-signal analysis of the circuit is

$$r_{\mathrm{out}} = r_{\mathrm{oD1}} + g_{\mathrm{m1}} R_1 r_{\mathrm{oD1}} - R_1 \approx g_{\mathrm{m1}} R_1 r_{\mathrm{oD1}}, \tag{2}$$

where r_{oD1} and g_{m1} is the output resistance and the transconductance of M_{D1}, respectively. The output swing of the circuit is limited by the maximum output voltage and can be expressed as

$$V_{\mathrm{OUT,MAX}} = V_{\mathrm{PS}} - V_{\mathrm{OV,M_{D1}}} - R_1 I_{\mathrm{REF}}, \tag{3}$$

where $V_{\mathrm{OV,M_{D1}}}$ is the overdrive voltage that can be written as

$$V_{\mathrm{OV,M_{D1}}} = V_{\mathrm{GS}} - V_{\mathrm{TH,D}}. \tag{4}$$

Based on that, and aiming to set a nominal current of $I_{\mathrm{REF}} = 16\,\mu\mathrm{A}$, with threshold voltage $V_{\mathrm{TH,D}} = -0.7\,\mathrm{V}$, the

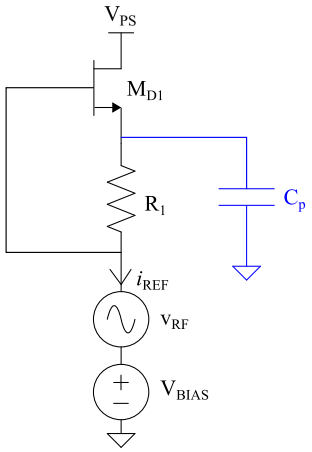


Fig. 5. Schematic diagram of the testbench circuit used to study EMI susceptibility with parasitic capacitance C_{p}.

resistance R_1 takes the value $R_1 = 40\,\mathrm{k\Omega}$. The DC current delivered by this current sources is highly affected by the fabrication tolerances, which affect R_1 and V_{TH}. Therefore, circuits comprising multiple current sources, are affected by current mismatch issues.

Better performance can be achieved by cascading two d-GaN devices, as shown in Fig. 4. Indeed, in the cascode configuration, the v_{DS} of M_{D1} is kept constant by the gate source voltage of M_{D2}, since this voltage is fixed by the drain current I_{D2}, which is the same flowing through M_{D1} and R_1. Therefore, the magnitude of the output current is controlled by R_1 and M_{D1}. The cascode circuit increases the output resistance, which can be expressed as

$$r_{\mathrm{out}} \approx g_{\mathrm{m2}} g_{\mathrm{m1}} R_1 r_{\mathrm{oD1}} (g_{\mathrm{m1}} R_1 r_{\mathrm{oD1}} + r_{\mathrm{oD2}}), \tag{5}$$

where r_{oD2} and g_{m2} is the output resistance and the transconductance of M_{D2}, respectively. The output swing of the circuit is

$$V_{\mathrm{OUT,MAX}} = V_{\mathrm{PS}} - 2v_{\mathrm{OV,M_{D1,2}}} - R_1 I_{\mathrm{REF}}. \tag{6}$$

This circuit exhibits higher output resistance, but a reduced voltage swing. However, the swing limitation is mitigated by the small $v_{\mathrm{OV,M_{D1,2}}}$.

In the following section, the susceptibility to RFI of such a circuit is discussed, and an analytical model for predicting the EMI-induced current is presented.

III. Rectification of RFI in GaN Current Source

RFI rectification in GaN current sources can be investigated referring to the test circuit in Fig. 5. The current generator is driven at the output terminal by the sinusoidal voltage source v_{RF}, which is defined as

$$v_{\mathrm{RF}} = v_{\mathrm{AC}} \cdot sin(\omega t). \tag{7}$$

v_{AC} is the voltage amplitude and $\omega = 2\pi f_0$, f_0 is the interference frequency.

The circuit parameters are listed in Table 1. In the schematic, i_{REF} is current delivered by the current source. v_{AC} is swept in the range between 0 V and 1 V. The effect of this signal

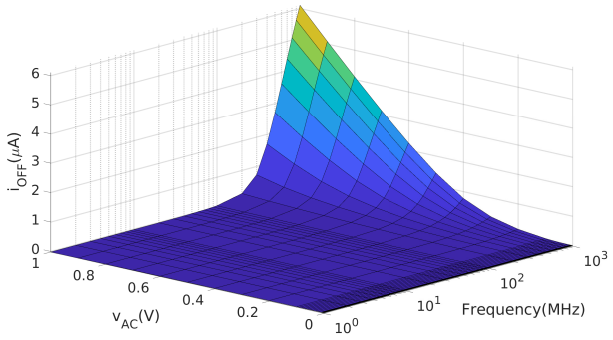


Fig. 6. Offset current of basic current generator.

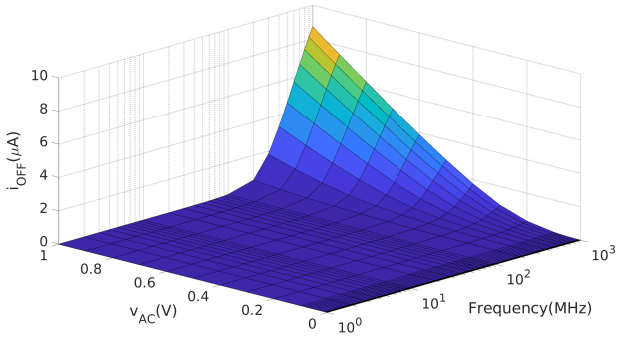


Fig. 7. Offset current of cascode current generator.

on the mean value of the output current ($\overline{i_{\mathrm{REF}}}$) is evaluated over the frequency range 1 MHz to 1 GHz. The offset current is defined as

$$i_{\mathrm{OFF}} = \overline{i_{\mathrm{REF}}} - i_{\mathrm{DC}} \tag{8}$$

where i_{DC} is the dc output current when $v_{\mathrm{AC}} = 0\,\mathrm{V}$. The results are plotted in Fig. 6.

From Fig. 6, an increase in the EMI frequency or the amplitude of the disturbance signal results in a corresponding rise in the offset current. The same analysis is performed for the cascode topology, using the circuit parameters listed in Table 1. The results for this topology are shown in Fig. 7.

For comparison, a pMOS current mirror (like that in Fig. 2) is implemented in a BCD technology, with transistors aspect ratio $W/L(M_{\mathrm{P1,2}}) = 12/2\ \mu\mathrm{m}$ and $I_{\mathrm{BIAS}} = 16\,\mu\mathrm{A}$. Finally, the susceptibility of the current mirror is evaluated and presented in Fig. 8. The maximum offset current in this case is 33 nA, significantly lower than that observed in GaN circuits.

In order to derive the relationship between $\overline{i_{\mathrm{REF}}}$ and the interaction of transistor nonlinearities with parasitic elements, an analytical model is presented. Referring to Fig. 5, M_{D1} is configured as a source follower. At low frequencies (below 1 MHz), the source voltage closely follows the gate voltage. However, at higher frequencies (above 1 MHz) the effect of the parasitic capacitance C_{p} cannot be neglected. Notably, the charge injected into C_{p} during the positive half-cycle of the sinusoidal signal V_{RF} is not equal to the charge withdrawn during the negative half-cycle. This charge imbalance causes

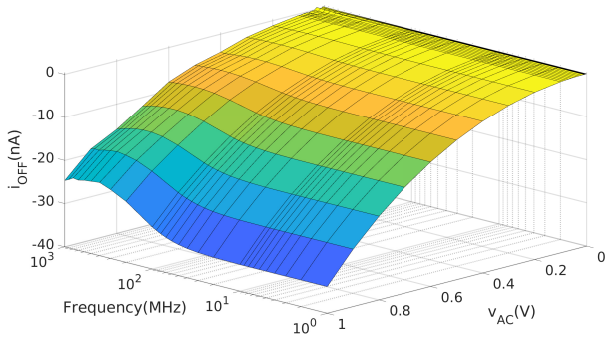


Fig. 8. Offset current of a pMOS current mirror.

Table 1. Dimensions of the current source circuits

Parameter	Value
V_{PS}	6 V
V_{BIAS}	3 V
$M_{\mathrm{D1}}(\frac{W}{L})$	$\frac{5}{0.5}$ µm
$M_{\mathrm{D2}}(\frac{W}{L})$	$\frac{5}{0.5}$ µm
R_1	40 kΩ
I_{REF}	16 µA

a shift in the mean value of the gate-source voltage. In the schematic, C_{p} represents the parasitic capacitance at this node, primarily due to the contributions of resistor capacitance, the drain-source and the source-bulk capacitances of the transistor. The value of C_{p} can be obtained performing a small-signal analysis of the nodal impedance. Assuming that the two main parasitic capacitances are C_{gs} (gate-source capacitance) of transistor and C_p, the V_{GS} can be expressed as

$$V_{\mathrm{GS}}(\omega) = \frac{j\omega R_1 C_{\mathrm{p}}}{1 + g_{\mathrm{m1}} R_1 + j\omega R_1 (C_{\mathrm{gs}} + C_{\mathrm{p}})} V_{\mathrm{RF}}(\omega). \tag{9}$$

Gate-source voltage in time domain is expressed by the following relation

$$v_{\mathrm{GS}} = \bar{v}_{\mathrm{GS}} + v_{\mathrm{gs}}(t), \tag{10}$$

where $\bar{v}_{\mathrm{GS}}$ is the mean value of the gate-source voltage, and $v_{\mathrm{gs}}(t)$ is the time-variant term, whose mean value is null. Under the hypothesis of current saturation, from (10), the mean value of the output current of transistor M_{D1}, is

$$\overline{i_{\mathrm{REF}}} \approx \bar{i}_{\mathrm{D}} = \beta[(\bar{v}_{\mathrm{GS}} - V_{\mathrm{TH}})^2 + \bar{v}_{\mathrm{gs}}^2] \tag{11}$$

in which $\beta = k_D/2 \cdot W/L$, k_{D} a technological parameter of d-GaN, W and L are respectively, the width and length of the gate area. In these equation $\bar{v}_{\mathrm{gs}}^2$ can be expressed in terms of its power spectral density (PSD) as derived from this work [9]. The mean-square value of gate-source voltage takes the form

$$\bar{v}_{\mathrm{gs}}^2 = \int_{-\infty}^{+\infty} S_{\mathrm{V_{GS}}}(\omega)\, d\omega, \tag{12}$$

where $S_{\mathrm{V_{GS}}}(\omega)$ is the PSD of the gate-source and is expressed in the following [9] as

$$S_{\mathrm{V_{GS}}}(\omega) = V_{\mathrm{GS}}(\omega) * V_{\mathrm{GS}}^*(\omega). \tag{13}$$

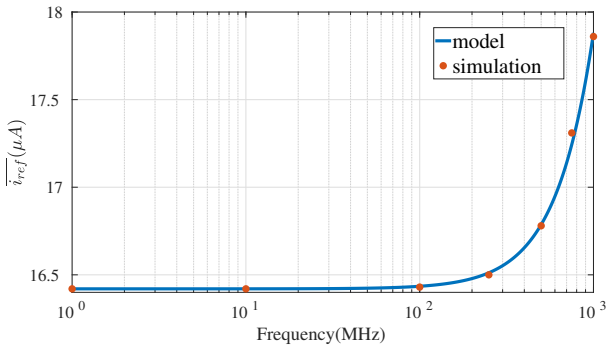


Fig. 9. $\overline{i_{\mathrm{REF}}}$ current of basic generator versus frequency, for $v_{\mathrm{AC}} = 500mV$. Continuous line and circle refer to model prediction and computer simulation respectively.

The substitution of (13),(12),(10) in (11) for CW interference gives

$$\bar{i}_{\mathrm{D}} = \beta\Bigg(\frac{g_{\mathrm{m1}}^2}{4\beta^2} + \int_{-\infty}^{+\infty} \frac{(C_{\mathrm{p}} R_1 \omega)^2}{(1 + g_{\mathrm{m1}} R_1)^2 + (C_{\mathrm{gs}} + C_{\mathrm{p}})^2 R_1^2 \omega^2} V_{\mathrm{RF}}^2 \Bigg) d\omega \tag{14}$$

that can be further simplified in case of sinusoidal input signal obtaining

$$\overline{i_{\mathrm{REF}}} = \bar{i}_{\mathrm{D}} = \beta\Bigg(\frac{g_{\mathrm{m1}}^2}{4\beta^2} + \frac{(C_{\mathrm{p}} R_1 \omega_0)^2}{(1 + g_{\mathrm{m1}} R_1)^2 + (C_{\mathrm{gs}} + C_{\mathrm{p}})^2 R_1^2 \omega_0^2} v_{\mathrm{AC}}^2 \Bigg), \tag{15}$$

where $\omega_0 = 2\pi f_0$, f_0 is the interference frequency. g_{m1} can be written as

$$g_{\mathrm{m1}} = \sqrt{4\beta I_0}, \tag{16}$$

where β is a parameter technology-dependent and I_0 is the nominal current when no RFI is applied.

This expression shows that the offset current is directly proportional to the square of both the peak disturbance signal and C_{p}. The proposed approach was validated using the circuit shown in Fig. 5, where C_{p} was accounted in the models of the resistor and transistor. Time-domain analysis was performed using Eldo, and the results are presented in Fig. 9.

This model will be employed in Section IV to design current sources with enhanced electromagnetic immunity.

IV. GaN Current Source with Enhanced Immunity to RFI

As mentioned previously, this section presents two solutions aimed at improving RFI immunity and analyzes their respective induced offset behaviors. To mitigate the RFI a low-pass filter is inserted, as illustrated in Fig. 10. The RC filter comprises the resistor R_{F}, connected between the signal source and the gate, and the capacitor C_{F}, connected between the gate and the source of M_{D1}. According to (15), an increase in gate-source capacitance reduces the output offset current. Indeed, adding C_{F} in parallel to C_{gs}, the second term of (15) reduces as well.

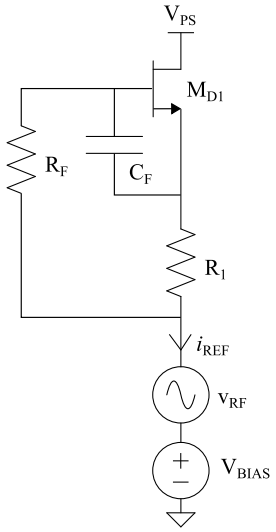


Fig. 10. Basic current generator with RC filter.

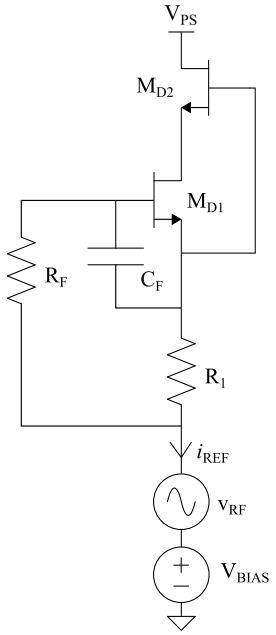


Fig. 11. Cascode current generator with RC filter.

Therefore, the cut-off frequency of the filter was set at 1 MHz. Therefore, for

$$C_{\mathrm{F}} \gg C_{\mathrm{gs}}, C_{\mathrm{p}} \tag{17}$$

and being

$$f_{\mathrm{c-o}} = \frac{1 + g_{\mathrm{m1}} R_1}{2\pi (R_1 + R_{\mathrm{F}}) C_{\mathrm{F}}}, \tag{18}$$

R_{F} and C_{F} can be defined.

Wanting to minimize the area needed for the integration of the low-pass filter, and being

$$A_{\mathrm{R_F}} = \frac{R_{\mathrm{F}}}{R_{\mathrm{S}}} \cdot W_{\mathrm{Rmin}}^2, \tag{19}$$

$$A_{\mathrm{C_F}} = \frac{C_{\mathrm{F}}}{C/A}, \tag{20}$$

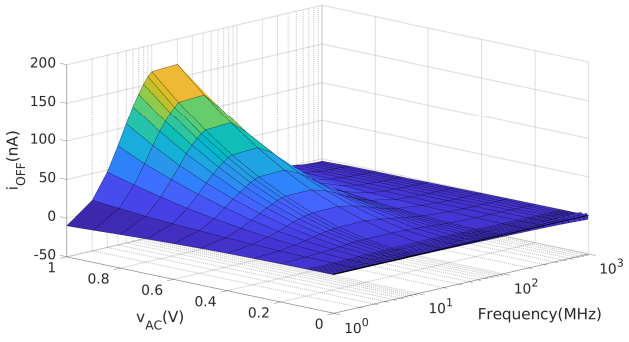


Fig. 12. Offset current of basic current generator with RC filter.

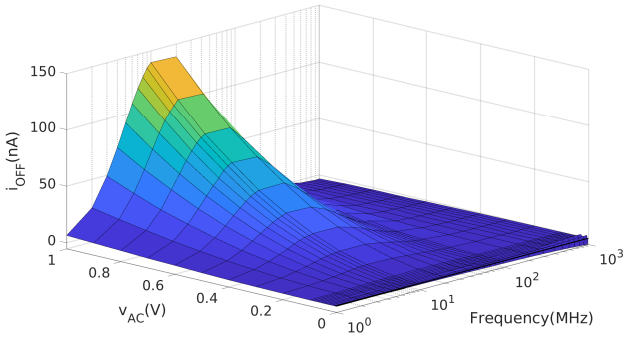


Fig. 13. Offset current of cascode current generator with RC filter.

where W_{Rmin} is the minimum width of the resistor, $R_{\mathrm{S}}(\Omega/\square)$ the sheet resistance, $C/A(nF/mm^2)$ is the capacitance per unit area, the overall area can be expressed as

$$A_{\mathrm{TOT}} = A_{\mathrm{R_F}} + A_{\mathrm{C_F}}. \tag{21}$$

Therefore, the minimum area is obtained for

$$R_{\mathrm{F}_{1,2}} = -R_1 \pm \frac{\sqrt{R_{\mathrm{S}}}}{\sqrt{2\pi C/A f_{\mathrm{c-o}}} W_{\mathrm{Rmin}}}, \tag{22}$$

which results from

$$\frac{\partial A_{\mathrm{TOT}}}{\partial R_{\mathrm{F}}} = 0. \tag{23}$$

In (22), only the positive value is physically meaningful, therefore $C_{\mathrm{F}} = 1.14\,\mathrm{pF}$ and $R_{\mathrm{F}} = 100\,\mathrm{k\Omega}$. A minimum area of $8514\,\mu\mathrm{m}^2$ is obtained. The implementation of resistance and capacitance is realized through GaN channel resistor and MiM capacitor, respectively. These components were selected to enhance performance with respect to area, voltage stability, and technology spread.

The same procedure applies to the cascode topology shown in Fig. 11, as the RFI signal primarily affects the gate of M_{D1}. In the following section simulations based on this topologies are presented.

V. Simulation Results

The proposed circuits were simulated using Eldo, a SPICE like simulator, and referring to the design kit provided by ST [13]. The transistor aspect ratios and component values used in the simulations are detailed in Table 1. To evaluate the impact

of RFI on circuits in Fig. 10 and 11, v_{AC} is swept from $0\,\mathrm{V}$ to $1\,\mathrm{V}$, with ten points per decade, and frequencies ranging from $1\,\mathrm{MHz}$ to $1\,\mathrm{GHz}$, also with ten points per decade. The cut-off frequency of the filters was set to $f_{\mathrm{c-o}} = 1\,\mathrm{MHz}$. To sense the output current i_{REF}, a sensing resistor $R_{\mathrm{SENSE}} = 1\,\mathrm{m\Omega}$ is added in series to the current source. The output offset current, as defined in (8), is evaluated by averaging over 50 periods of the current signal i_{REF} after it has reached its steady state. The 3D plots of the output offset current are shown in Fig. 12 and 13. These results point out a significant reduction in the maximum offset current: from $6\,\mu\mathrm{A}$ to $165\,\mathrm{nA}$ for the basic topology, and from $9\,\mu\mathrm{A}$ to $140\,\mathrm{nA}$ for the cascode topology. However, above $100\,\mathrm{MHz}$, the offset is null. The peak value of i_{OFF} is located between $10\,\mathrm{MHz}$ and $20\,\mathrm{MHz}$ at the maximum amplitude of the sinusoidal signal for both circuits.

Simulation results show that the proposed current sources are more immune to RFI compared to traditional ones. However, compared to traditional pMOS current mirrors implemented in mature CMOS technology, are characterized by higher offset current.

VI. Conclusion

This paper investigates the effect of radiofrequency interference on two different GaN current source topologies and develops an analytical model for predicting EMI-induced transients. The proposed model accounts for nonlinearities induced by RFI that alter the nominal behavior of the circuit. Such distortion arises from the presence of parasitic capacitances at the circuit's intermediate nodes. While existing literature models typically focus on CMOS current mirrors for susceptibility estimation, the proposed model is specifically tailored to d-GaN current source topologies. It provides an analytical formulation that captures the nonlinear interaction between RF disturbances and circuit parasitics. This makes it particularly suitable for guiding design-level mitigation strategies without the need for extensive SPICE simulations.

Furthermore, the performance of these GaN circuits was compared with that of a pMOS current mirror implemented in CMOS technology. Finally, a filtering solution to enhance RFI immunity has been proposed and validated through simulations.

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