Reduction of Common Mode Conducted EMI in GaN-Based Two-Switch Flyback Converters Using

Reduction of Common Mode Conducted EMI in GaN-Based Two-Switch Flyback Converters Using the Delay Compensation Technique

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***Abstract* — Common mode conducted EMI is a critical issue in power switching converters, particularly in automotive applications. Symmetrical topologies like two-switch flyback are effective in reducing EMI, but the delay between high-side and low-side switches can worsen the delivered EMI. This work investigates the use of the delay compensation technique in a GaN-based two-switch flyback converter. The study addresses both impedance balancing and delay effects on conducted EMI. Simulation results confirm a $25\,\mathrm{dB}$ reduction at $200\,\mathrm{kHz}$ with both delay compensation and impedance balancing compared to a traditional flyback converter.**

***Keywords* — ElectroMagnetic Interference (EMI), common mode conducted EMI, delay compensation technique, GaN transistors, dc-dc isolated converters, two-switch flyback.**

I. Introduction

In Electric Vehicles (EVs) and Hybrid Electric Vehicles (HEVs), traction inverters take DC input from a High Voltage (HV) battery and provide the required AC output to the electric motor. Control circuitry of the inverter includes isolated power supplies, called Auxiliary Power Supplies (APSs), to deliver power to the gate drivers of the inverter. The input of these isolated converter is typically connected to the Low Voltage (LV) battery, but it may also be connected to the HV battery, usually as a backup. As the power required for such APSs is typically lower than $50\,\mathrm{W}$, flyback topology is the preferred choice due to its low components count.

Regarding the power switches the APSs are comprised of, Gallium Nitride (GaN) transistors have recently gained attention, as they allow for high efficiency, power density and switching frequency [1]. With the operating frequency of GaN-based converters in the $100\,\mathrm{kHz}$-$1\,\mathrm{MHz}$ range [2], Electro Magnetic Interference (EMI) at the low frequency are expected to increase due to the presence of the fundamental switching frequency and its harmonics [3]. Additionally, GaN devices are typically limited to a maximum breakdown voltage of $650\,\mathrm{V}$, which could be insufficient when targeting high voltage applications. To overcome such issues, two-switch flyback topology could be an alternative to traditional flyback, reducing the stress on the drain-source voltage of power transistors and improving efficiency through leakage energy recovery [4].

To address Electro Magnetic Interference (EMI) delivered by such converters, passive input filters are commonly exploited. However, they are bulky and heavy thus undermining the benefits of GaN transistors. Besides filtering, which is a technique that acts along the propagation path, several EMI reduction techniques targeting the noise source have been proposed [5]. Spread Spectrum (SS) modulation, for instance, spreads harmonic energy by modulating the switching frequency, thus reducing peaks [6]. Sigma-Delta modulation has also been explored, demonstrating reduced conducted EMI at low frequencies [7]. Additionally, Active Gate Drivers (AGDs), such as [8], [9], offer a tight control of switching transients, although they are primarily effective at high frequencies.

Concerning isolated converters, several techniques have been proposed to mitigate Common Mode (CM) EMI along the propagation path [10]. Shielding, for example, reduces capacitive coupling between transformer windings. Passive cancellation techniques, which introduce compensating currents [11] or voltages [12], have also been widely studied. Additionally, symmetry can be achieved by adding components to create a complementary switching node, theoretically nullifying CM noise [13]. Two-switch flyback and two-switch forward converters feature symmetrical primary-side circuits with complementary switching nodes. CM EMI in a two-switch forward converter was studied in [14], where adding a compensating capacitor reduced noise by up to $12\,\mathrm{dB}$ at low frequencies and by up to $20\,\mathrm{dB}$ by compensating the interwinding capacitance of gate driver transformer. Similarly, [15] introduced a cancellation capacitor in a multi-winding two-switch flyback converter, achieving a $15\,\mathrm{dB}$ reduction in conducted EMI.

However, the reported studies have not addressed the delay between high-side and low-side switches or its impact on CM EMI. This delay, caused by component mismatches or driving circuit asymmetries, leads to a misalignment of the switching voltages. The Delay Compensation Technique (DCT), originally proposed for motor drive applications [16], [17], [18], is based on the fine alignment of complementary switching waveforms to cancel CM current at the source. However, the DCT effectiveness in dc-dc converters remains

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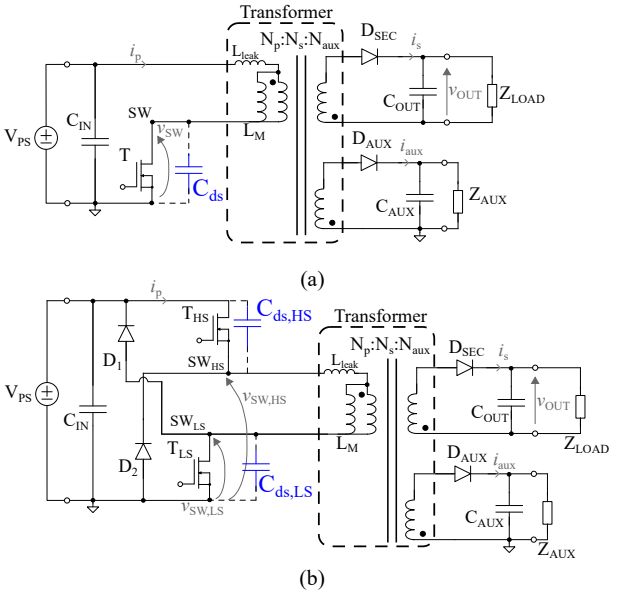

Fig. 1. Schematic of (a) one-switch flyback converter including one secondary and an auxiliary circuit, (b) two switch flyback converter.

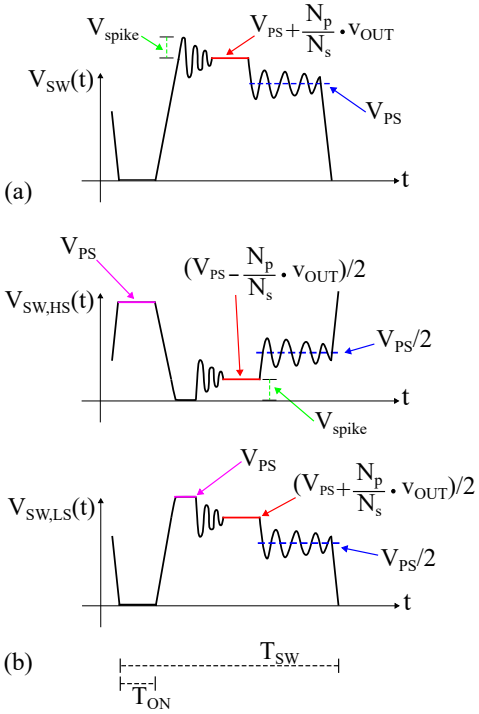

Fig. 2. Switch voltage waveform related to (a) the one-switch flyback shown in Fig. 1 at the top, and (b) high side and low side switch voltage waveforms of two-switch flyback shown in Fig. 1 at the bottom.

unexplored. This paper provides a detailed analysis of common mode EMI of a HV-LV GaN-based two switch flyback converter, taking into account both the impedance balance and the delay between the two transistors. In particular, the DCT is applied and its effectiveness in reducing CM EMI is assessed.

The paper is organized as follows. A brief description of one-switch and two-switch flybacks is provided in Sect. II. Sect. III discusses the CM EMI in a two-switch flyback, with the application of DCT and impedance balancing discussed in Sect. IV and V, respectively. Simulation results are provided in Sect. VI, with final remarks in Sect. VII.

II. One-switch and two-switch flyback

The power stage of a traditional flyback converter is shown in Fig. 1(a). This topology typically includes a low side switch T at the primary side, a transformer providing galvanic isolation and a rectifier (D_{SEC}) at the secondary side. Moreover, an auxiliary circuit is included to supply the flyback controller. When the switch T is turned on, current in the primary windings i_{p} increases linearly and energy is stored in the magnetizing inductance L_{M} of the transformer. When the switch is turned off, energy is transferred to the secondary windings, and diode D_{SEC} turns on, providing current to the Z_{LOAD}. Assuming the flyback to operate in Discontinuous Conduction Mode (DCM), the secondary winding current i_{s} decreases to zero before the next switching cycle.

A crucial aspect in HV applications is the voltage stress on the T transistor. The v_{SW} voltage of one-switch flyback is shown in Fig. 2(a). The switch turn-off causes v_{SW} to rise from 0 V to

$$V_{\mathrm{DS,MAX}} = V_{\mathrm{PS}} + \frac{N_{\mathrm{p}}}{N_{\mathrm{s}}} \cdot v_{\mathrm{OUT}} + V_{\mathrm{spike}}, \qquad (1)$$

where V_{PS} is the input voltage, N_{p} (N_{s}) is the number of primary (secondary) windings, v_{OUT} is the regulated output voltage. The term V_{spike} accounts for overshoots related to the resonance between the leakage inductance L_{leak} and the stray capacitances loading the switching node. This transition can be particularly critical, as the breakdown voltage of transistor T should be sufficiently higher than $V_{\mathrm{DS,MAX}}$.

To overcome this limitation, the two-switch flyback topology, shown in Fig. 1(b), is adopted. Compared to the one-switch flyback converter, this topology includes an extra transistor and two more diodes in the primary circuit. By inserting an additional switch T_{HS} between V_{PS} and the dotted terminal of the transformer, a second switching node (SW_{HS}) is introduced. Voltages of nodes SW_{HS} and SW_{LS} with respect to the primary ground are plotted in Fig. 2(b). The T_{LS} and T_{HS} switches turn on and off simultaneously, ensuring that the transformer works in a similar way to the one-switch flyback. It is worth noticing that, when the switches turn off, the additional diodes D_1 and D_2 provide a path for the leakage inductance current to circulate back into the input source. This allows for improved efficiency, as well as the clamp of $v_{\mathrm{SW,HS-LS}}$ to 0 V and V_{PS}, respectively, thereby limiting the voltage stress on the transistors.

III. CM EMI of two switch flyback converter

From an EMC perspective, switching node voltage behavior is a major source of EMI in switching converters. This occurs due to capacitive coupling between the switching node and the reference plane, leading to common mode EMI. In particular, the heatsink of the switching transistor is typically connected to the reference plane for safety reasons, resulting in

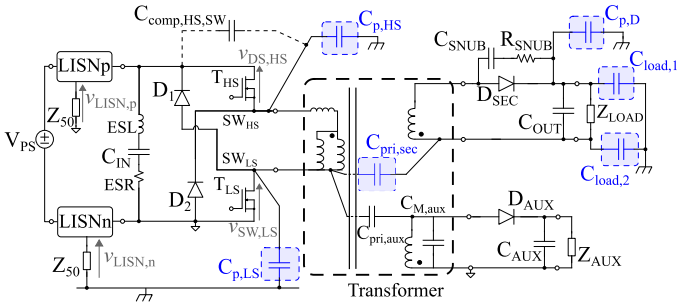

Fig. 3. Setup for measurement of conducted EMI generated by the two-switch flyback converter topology. The main parasitic elements related to CM noise have been surrounded by a dashed box.

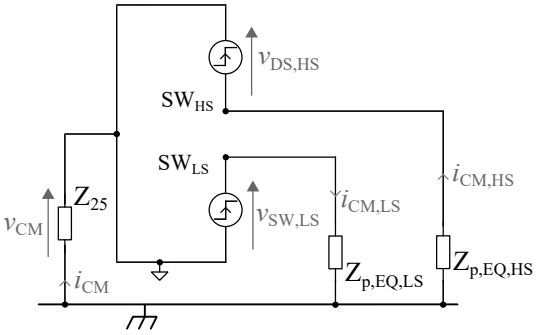

Fig. 4. Simplified equivalent common mode model of two switch flyback converter.

an unintentional parasitic capacitance. Fast switching transients generate displacement currents through this capacitance, which in turn may cause the converter to exceed regulatory EMC limits.

As described in Sect. II, two-switch flyback differs from one-switch one due to the presence of two switching nodes. In ideal conditions, the switching voltages shown in Fig. 2(b) have same magnitude but opposite dv/dt. In principle, this allows for the elimination of common mode EMI [13]. However, in practice, a delay between the high-side and low-side switches can misalign the switching voltages. The Delay Compensation Technique can be used to address such a delay [16]. Moreover, an imbalance of CM parasitic impedances loading the switching nodes can exist, worsening the CM EMI reduction. To thoroughly investigate the effects of DCT and impedance unbalance in a two-switch flyback converter, the setup shown in Fig. 3 is considered.

According to CISPR-25 standard [19], two Line Impedance Stabilization Networks (LISNs) are placed between the input source and the Device Under Test (DUT). Conducted EMI measurements are performed across Z_{50}, which model the input impedance of the measuring instrument. Conducted EMI can be separated into common mode and differential mode; however, the focus of this work is on the common mode, which is defined as

$$v_{\mathrm{LISN,CM}}(t) \triangleq \frac{v_{\mathrm{LISN,P}}(t) + v_{\mathrm{LISN,N}}(t)}{2}. \tag{2}$$

In the circuit shown in Fig. 3, the parasitic capacitances related to CM EMI have been enclosed in a dashed box to be found at a glance. The main contributors, $C_{\mathrm{p,HS}}$, $C_{\mathrm{p,LS}}$ and $C_{\mathrm{pri,sec}}$, can be identified. $C_{\mathrm{p,HS}}$ and $C_{\mathrm{p,LS}}$ are the parasitic capacitances of the thermal pads of the high side MOSFET source and the low side MOSFET drain towards the reference plane through the heatsink. $C_{\mathrm{pri,sec}}$ is the interwinding capacitance between primary and secondary windings of the transformer. In a real transformer, such capacitance is distributed, hence, a lumped model is needed to ease circuit analysis. The complete transformer model considered in this study is that presented in [20]. The presence of the interwinding capacitance causes a coupling path for CM between primary side and secondary side, thereby allowing $C_{\mathrm{p,D}}$ and $C_{\mathrm{load},1-2}$ parasitics on the secondary side to affect common-mode EMI at the input. $C_{\mathrm{p,D}}$ is the parasitic capacitance between the thermal pad of the cathode of the diode towards the reference through the heatsink. $C_{\mathrm{load},1-2}$ are the parasitic capacitances of the load towards the reference plane. The impact of $C_{\mathrm{comp,REF,HS}}$ and of $C_{\mathrm{comp,HS,SW}}$ is explained in Sect. V.

IV. DCT Application in Two-Switch Flyback

The switching voltages of a two-switch flyback, which are shown in Fig. 2(b), are ideally perfectly complementary. As a result, the parasitic currents induced by the turn-on of the transistors through the capacitive coupling of SW_{HS} and SW_{LS} to the reference plane, are equal in magnitude but opposite in direction, leading to their cancellation. Nevertheless, in a real circuit, a misalignment of the turn-on transients occurs, due to mismatches in the two transistors. Parasitic capacitance mismatches in MOSFETs may occur, while temperature variations can cause variations in the threshold voltage. Asymmetries in the gate drivers circuits can further contribute to this misalignment. As a result, currents flowing through the parasitic capacitances may not longer be equal, preventing their complete cancellation. This may cause an increase in common mode EMI. In this context, the DCT is investigated in order to understand its impact on common mode EMI of the two-switch flyback converter.

The schematic of Fig. 3 has been simplified into the CM equivalent circuit of Fig. 4. LISNs are modeled as two $50\,\Omega$ impedances Z_{50} in parallel (Z_{25}), whereas the input capacitor C_{IN} can be approximated as a short circuit. MOSFETs are replaced by two independent voltage sources $v_{\mathrm{DS,HS}}$ and $v_{\mathrm{SW,LS}}$, i.e., the drain-source voltages of the two transistors. The effect of D_1, D_2 and D_{SEC} is neglected, since they are turned off during the turn-on transient of the transistors. $Z_{\mathrm{p,EQ,LS}}$ and $Z_{\mathrm{p,EQ,HS}}$ represent the total CM impedances loading the SW_{LS} and SW_{HS} nodes to the reference plane.

By assuming $v_{\mathrm{SW,LS}} = v_{\mathrm{DS,HS}}$ except for a delay τ_{D}, and $Z_{\mathrm{p,EQ,LS}} = Z_{\mathrm{p,EQ,HS}} = Z_{\mathrm{p,EQ}} = 1/j\omega C_{\mathrm{p}}$, the CM voltage across Z_{25} can be derived in the complex frequency domain by exploiting the superposition principle, resulting in

$$V_{\mathrm{CM},2-\mathrm{sw}}(j\omega) = H_{2-\mathrm{sw}}(j\omega)V_{\mathrm{SW,HS}}(j\omega)(1 - e^{-j\omega\tau_{\mathrm{D}}}), \tag{3}$$

where $H_{2-\mathrm{sw}}(j\omega)$ is a high pass filter function

$$H_{2-\mathrm{sw}}(j\omega) = \frac{j\omega Z_{25} C_{\mathrm{p}}}{1 + j\omega 2 Z_{25} C_{\mathrm{p}}}. \tag{4}$$

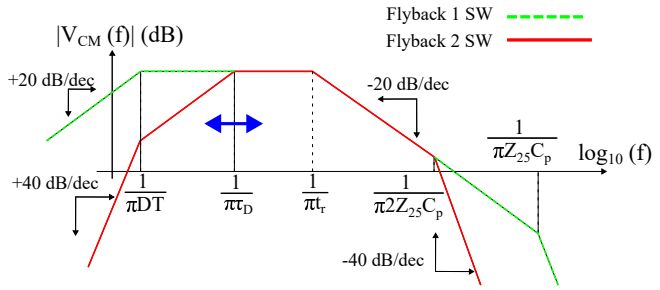

Fig. 5. Envelope of common mode voltage in case of two-switch (solid) and one-switch flyback (dashed line). The complementary commutations of the two transistors results in lower CM conducted EMI at low frequency.

The term $(1-e^{-j\omega\tau_{\mathrm{D}}})$ represents the effect of the delay [18]. Concerning the one-switch flyback, an expression similar to (3) can be derived

$$V_{\mathrm{CM},1-\mathrm{sw}}(j\omega)=\frac{j\omega Z_{25}C_{\mathrm{p}}}{1+j\omega Z_{25}C_{\mathrm{p}}}V_{\mathrm{SW}}(j\omega). \tag{5}$$

Approximating the $v_{\mathrm{SW,HS}}$ and v_{SW} voltages as trapezoidal waveforms with a 50 % duty cycle and equal rise and fall times ($t_{\mathrm{r}}=t_{\mathrm{f}}$), the envelopes of $|V_{\mathrm{CM},2-\mathrm{sw}}(j\omega)|$ and $|V_{\mathrm{CM},1-\mathrm{sw}}(j\omega)|$ are shown in Fig. 5. Referring to the one-switch flyback (dashed line), the breakpoint frequencies are those of the high-pass transfer function and of the V_{SW} spectrum. Conversely, in case of a two-switch converter (solid line), the delay contribution adds a breakpoint at frequency $1/\pi\tau_{\mathrm{D}}$. As τ_{D} decreases, the pole moves towards higher frequencies, allowing for increased attenuation in the low-frequency range of the common mode voltage spectrum.

V. Impedance Balance

In the analysis presented in Section IV, the impedances between the switching nodes and the reference plane, $Z_{\mathrm{p,EQ,HS}}$ and $Z_{\mathrm{p,EQ,LS}}$, have been assumed to be equal; however, this assumption may not always hold. In particular, referring to the circuit shown in Fig. 3, the actual values of $Z_{\mathrm{p,EQ,HS}}$ and $Z_{\mathrm{p,EQ,LS}}$ are

$$Z_{\mathrm{p,EQ,HS}}=\frac{1}{j\omega C_{\mathrm{p,EQ,HS}}}=\frac{1}{j\omega C_{\mathrm{p,HS}}}, \tag{6}$$

$$Z_{\mathrm{p,EQ,LS}}=\frac{1}{j\omega C_{\mathrm{p,EQ,LS}}} \tag{7}$$

where

$$C_{\mathrm{p,EQ,LS}}=\frac{(C_{\mathrm{p,D}}+C_{\mathrm{load},1}+C_{\mathrm{load},2})C_{\mathrm{pri,sec}}}{C_{\mathrm{p,D}}+C_{\mathrm{load},1}+C_{\mathrm{load},2}+C_{\mathrm{pri,sec}}}+C_{\mathrm{p,LS}}. \tag{8}$$

Eqn.s (6) and (7) have been obtained neglecting $C_{\mathrm{pri,aux}}$, $C_{\mathrm{sec,aux}}$, $C_{\mathrm{M,pri}}$, $C_{\mathrm{M,sec}}$ and $C_{\mathrm{M,aux}}$. Transformer interwinding capacitance introduces a mismatch between $Z_{\mathrm{p,EQ,HS}}$ and $Z_{\mathrm{p,EQ,LS}}$, requiring the modification of (3) as follows

$$\begin{aligned}V_{\mathrm{CM}}(j\omega)=&\frac{Z_{25}\oplus Z_{\mathrm{p,EQ,LS}}}{Z_{25}\oplus Z_{\mathrm{p,EQ,LS}}+Z_{\mathrm{p,EQ,HS}}}V_{\mathrm{DS,HS}}(j\omega)+\\&-\frac{Z_{25}\oplus Z_{\mathrm{p,EQ,HS}}}{Z_{25}\oplus Z_{\mathrm{p,EQ,HS}}+Z_{\mathrm{p,EQ,LS}}}V_{\mathrm{SW,LS}}(j\omega)e^{-jn\omega_0\tau_{\mathrm{D}}}\end{aligned} \tag{9}$$

Table 1. Two-switch and one-switch flyback converters parameters.

Parameter	Value	Parameter	Value	Parameter	Value
V_{PS}	400 V	D_1, D_2	[21]	V_{OUT}	15 V
P_{OUT}	40 W	C_{OUT}	2 mF	C_{IN}	360 nF
$T_{\mathrm{LS}}, T_{\mathrm{HS}}$	[22]	$D_{\mathrm{SEC}}, D_{\mathrm{AUX}}$	[23]	f_{SW}	200 kHz
ESL	6 nH	C_{SNUB}	150 pF	$C_{\mathrm{load},1-2}$	3 pF
R_{SNUB}	20 Ω	$C_{\mathrm{p}}, C_{\mathrm{p,HS}}, C_{\mathrm{p,HS}}$	7 pF	$C_{\mathrm{p,D}}$	9 pF

To mitigate the effect of the mismatch, impedance balance technique can be applied [14]. Considering (6) and (7), a compensating capacitor defined as $C_{\mathrm{comp,REF,HS}}$ can be placed between the switching node with lower equivalent capacitance and the reference plane. In Fig. 3 $C_{\mathrm{comp,REF,HS}}$ has been added, assuming that $Z_{\mathrm{p,EQ,HS}}$ is lower than $Z_{\mathrm{p,EQ,LS}}$.

Moreover, the impedance mismatch between the two switching nodes does not only impact (3), but also affects the turn-on transients of the transistors, making the assumption of equal switch voltages no longer valid. This unbalance is further exacerbated by the presence of $C_{\mathrm{pri,aux}}$ and $C_{\mathrm{M,aux}}$, which, although negligible in terms of common-mode generation, effectively appear in parallel to T_{LS}. This results in an additional asymmetry between the switching nodes. To counteract this effect, a compensating capacitor denoted as $C_{\mathrm{comp,HS,SW}}$ (Fig. 3 (a)) equal to the sum of $C_{\mathrm{pri,aux}}$ and $C_{\mathrm{M,aux}}$, can be inserted in parallel to T_{HS}.

VI. Circuit Analysis

In order to assess the efficacy of the DCT, conducted EMI of the two-switch flyback converter shown in Fig. 3 and one-switch flyback, have been assessed through time-domain simulations using a Spice-like simulator [24]. More precisely, voltages across the LISNs measurement ports ($v_{\mathrm{LISN,p}}$ and $v_{\mathrm{LISN,n}}$) have been considered and $v_{\mathrm{CM}}(t)$ obtained as (2). The derived waveform has been processed using the virtual EMI receiver described in [25]. The resolution bandwidth (RBW) has been set to 9 kHz for the 150 kHz–30 MHz range and 120 kHz for the 30 MHz–108 MHz range, as prescribed by the standard [19]. Parameters and components values of Fig. 3 are those reported in [20] and listed in Table 1 for reference.

The values of $C_{\mathrm{comp,REF,HS}}$ and $C_{\mathrm{comp,HS,SW}}$ have been determined based on (6) and (7)

$$C_{\mathrm{p,EQ,HS}}=C_{\mathrm{p,HS}}=7\mathrm{pF} \tag{10}$$

$$C_{\mathrm{p,EQ,LS}}\approx 19\mathrm{pF}, \tag{11}$$

hence, to have $C_{\mathrm{p,EQ,LS}}$ and $C_{\mathrm{p,EQ,HS}}$ equal, $C_{\mathrm{comp,REF,HS}}$ should be added in parallel to $C_{\mathrm{p,EQ,HS}}$ and its value should be around 12 pF. Regarding $C_{\mathrm{comp,HS,SW}}$, its value is estimated to be approximately 38 pF, i.e., $C_{\mathrm{pri,aux}}+C_{\mathrm{M,aux}}$.

Fig. 6 shows the comparison of CM EMI spectra of two-switch flyback in the following conditions: without both compensating capacitors and τ_{D} equal to 0 ns (green spectrum), with both capacitors and τ_{D} equal to 0 ns (red) and 20 ns (purple spectrum). The case of one-switch flyback is also reported as a reference in black. To perform the simulation, τ_{D} has been implemented by delaying the gate signal of T_{HS}

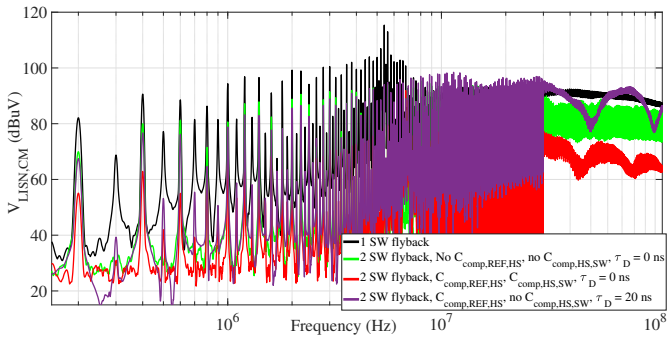

Fig. 6. CM EMI frequency spectrum comparison: one-switch flyback and two-switch flyback with and without compensating capacitors. The effect of τ_D is also reported.

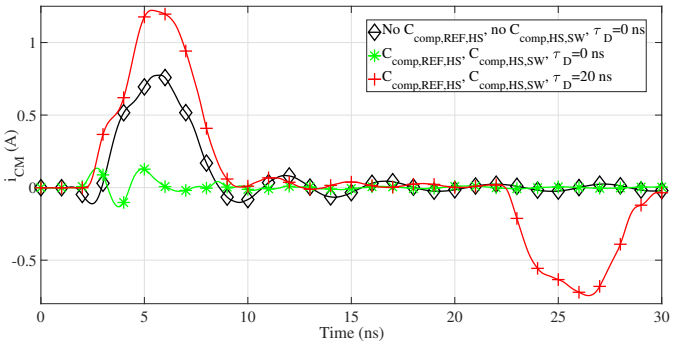

Fig. 7. Time-domain comparison of CM current: case without compensating capacitors and τ_D applied to T_{HS} at 0 ns, and case with both compensating capacitors and τ_D applied to T_{HS} at 0 ns and 20 ns.

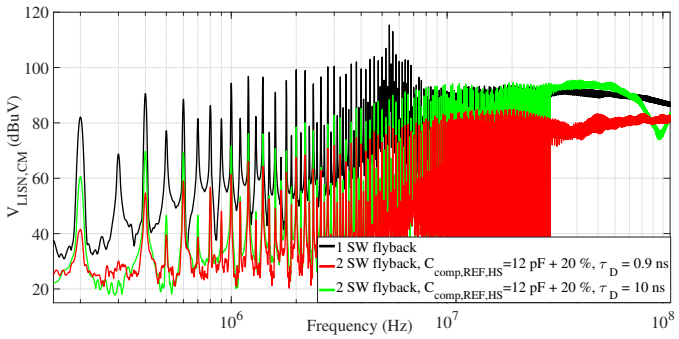

Fig. 8. Comparison of the CM EMI frequency spectrum between the one-switch flyback and the two-switch flyback with $C_{\mathrm{comp,HS,ref}}$ set to 12 pF +20 %, and τ_{D} applied to T_{HS} at 0.9 ns and 10 ns.

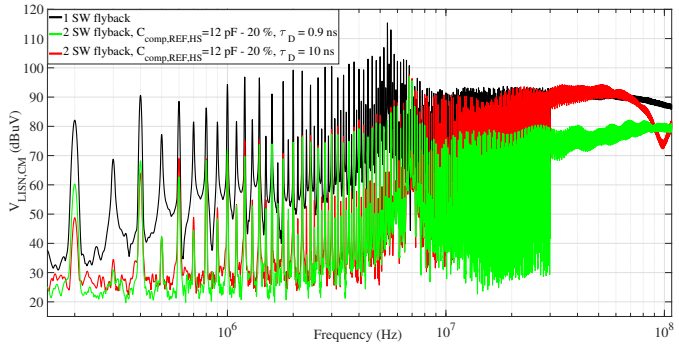

Fig. 9. Comparison of the CM EMI frequency spectrum between the one-switch flyback and the two-switch flyback with $C_{\mathrm{comp,HS,ref}}$ set to 12 pF −20 %, and τ_{D} applied to T_{LS} at 0.9 ns and 10 ns.

relative to the gate signal of T_{LS}. Considering τ_{D} equal to 0 ns, the addition of the compensating capacitors is effective since an improvement from 10 dB to 20 dB can be observed. However, with τ_{D} equal to 20 ns, a degradation of around 15 dB can be depicted, making the addition of $C_{\mathrm{comp,REF,HS}}$ and $C_{\mathrm{comp,HS,SW}}$ substantially ineffective. The impact of the delay on common mode current (i_{CM}) in time domain is shown in Fig. 7, where the same conditions of Fig. 6 have been considered. The waveform representing the case with both compensating capacitors and τ_{D} equal to 20 ns (plus marker), shows two peaks characterized by opposite direction and delayed one with respect to the other of 20 ns.

Added compensating capacitors suffer from tolerances, thus, it is worth studying CM EMI spectra considering both variations of the added capacitors and the delay. In particular, a relative variation of $\pm 20\%$ and $\pm 10\%$ of $C_{\mathrm{comp,HS,ref}}$ has been considered, while delay has been added to the HS and LS switch for positive and negative variations of $C_{\mathrm{comp,HS,ref}}$, respectively. The Relative Amplitude (RA) figure of merit has been defined to facilitate the comparison.

$$RA = V_{\mathrm{CM,FLY,1SW}} - V_{\mathrm{CM,FLY,2SW,C_{comp,HS,ref}\pm k\%}}, \quad (12)$$

where $V_{\mathrm{CM,FLY,1SW}}$ is the amplitude of the CM spectrum of the one-switch flyback, and $V_{\mathrm{CM,FLY,2SW,C_{comp,HS,ref}\pm k\%}}$ is the amplitude of the CM spectrum of the two-switch flyback with a k relative variation of $C_{\mathrm{comp,HS,ref}}$. In Table 2, the values of RA for τ_{D} equal to 0 ns are listed, along with the difference between the maximum RA and the RA for τ_{D} equal to 0 ns at the peak frequencies located at the fundamental (200 kHz), and the first two harmonics (400 kHz and 600 kHz), considering all the tested values of k. Also included is the value of τ_{D} where the optimum occurs. All the reported values of RA are positive, meaning that two-switch flyback is effective in reducing CM EMI with respect to one-switch flyback. On the other hand, it can be observed that the maximum value of RA almost always takes place with a τ_{D} different from 0 ns. In Fig. 8 the comparison between the CM EMI in case of one-switch and of two-switch flyback with $k = +20\,\%$ and τ_{D} applied to T_{HS} equal to 0.9 ns and 10 ns is shown. In Fig. 9 the same comparison is shown except for k, which is equal to $-20\,\%$ and τ_{D} is applied to T_{LS}. It is interesting to notice that in the frequency range from 150 kHz to about 7 MHz, the effect of the increased delay with $k = +20\,\%$ is more pronounced with respect to $k = -20\%$.

VII. Conclusion

In this work, the performance of a GaN-based two-switch flyback converter in terms of common-mode EMI has been analyzed. It has been demonstrated that the Delay Compensation Technique is effective in reducing common mode noise, provided that the parasitic capacitances loading the switching nodes are equal. It has also been found that depending on the tolerance of the compensating capacitor, an

Table 2. Values of RA for $\tau_{\mathrm{D}} = 0\,\mathrm{ns}$, along with the difference between the maximum RA and the RA at $\tau_{\mathrm{D}} = 0\,\mathrm{ns}$ at the fundamental frequency (200 kHz) and the first two harmonics (400 kHz, 600 kHz). The value of τ_{D} corresponding to the optimum RA is also reported.

k	$RA_{\tau_{\mathrm{D}}=0\,\mathrm{ns}}$, $RA_{\mathrm{MAX}} - RA_{\tau_{\mathrm{D}}=0\,\mathrm{ns}}(\tau_{\mathrm{D,MAX}})$		
	200 kHz	400 kHz	600 kHz
+20 %	33.8 dB, 6.8 dB (0.9 ns)	31.2 dB, 7 dB (1.6 ns)	25.7 dB, 10.9 dB (2.9 ns)
-20 %	20.4 dB, 12.9 dB (10 ns)	20.8 dB, 9.8 dB (5 ns)	22.8 dB, 10.4 dB (3 ns)
+10 %	34.3 dB, 0 dB (0 ns)	35.5 dB, 0 dB (0 ns)	32.5 dB, 6.3 dB (0.7 ns)
-10 %	23 dB, 13.6 dB (5 ns)	23.6 dB, 9.9 dB (5 ns)	26.7 dB, 21.1 dB (2.4 ns)

optimal reduction of CM EMI for each of the harmonics may take place with a delay different from zero.

REFERENCES

[1] T. Garg and S. Kale, "Recent developments, reliability issues, challenges and applications of gan hemt technology," *IEEE Electron Devices Reviews*, vol. 1, pp. 16–30, 2024. DOI: 10.1109/EDR.2024.3491716.

[2] C.-T. Ma and Z.-H. Gu, "Review of gan hemt applications in power converters over 500 w," *Electronics*, vol. 8, no. 12, 2019, ISSN: 2079-9292. DOI: 10.3390/electronics8121401.

[3] B. Zhang and S. Wang, "A survey of EMI research in power electronics systems with wide-bandgap semiconductor devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 626–643, 2020. DOI: 10.1109/JESTPE.2019.2953730.

[4] D. Murthy-Bellur and M. K. Kazimierczuk, "Two-switch flyback pwm dc–dc converter in discontinuous-conduction mode," *International Journal of Circuit Theory and Applications*, vol. 39, no. 8, pp. 849–864, 2011. DOI: https://doi.org/10.1002/cta.672.

[5] J. Imaoka, M. Sasaki, Y. Omoto, M. Noah, K. Shigematsu, and M. Yamamoto, "Common mode noise reduction methods used for high power density dc/dc converters," in *2024 14th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2024, pp. 1–6. DOI: 10.1109/EMCCompo61192.2024.10742027.

[6] F. Pareschi, R. Rovatti, and G. Setti, "EMI reduction via spread spectrum in dc/dc converters: State of the art, optimization, and tradeoffs," *IEEE Access*, vol. 3, pp. 2857–2874, 2015. DOI: 10.1109/ACCESS.2015.2512383.

[7] A. Barbaro, M. Fishta, E. Raviola, and F. Fiori, "A comparison of spread spectrum and sigma delta modulations to mitigate conducted EMI in gan-based dc-dc converters," in *2024 14th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2024, pp. 1–6. DOI: 10.1109/EMCCompo61192.2024.10742065.

[8] E. Raviola and F. Fiori, "A critical assessment of open-loop active gate drivers under variable operating conditions," in *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, 2021, pp. 94–99. DOI: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559173.

[9] E. Raviola and F. Fiori, "An adaptive method to reduce undershoots and overshoots in power switching transistors through a low-complexity active gate driver," *IEEE Transactions on Power Electronics*, vol. 38, no. 3, pp. 3235–3245, 2023. DOI: 10.1109/TPEL.2022.3221187.

[10] Q. Huang, Y. Yang, Y. Lai, Z. Ma, and S. Wang, "A survey of cm EMI modeling and reduction technique of transformer for isolated converters," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 1484–1490. DOI: 10.1109/APEC48139.2024.10509196.

[11] D. Cochrane, D. Chen, and D. Boroyevic, "Passive cancellation of common-mode noise in power electronic circuits," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 756–763, 2003. DOI: 10.1109/TPEL.2003.810858.

[12] L. Xie and X. Yuan, "Non-isolated dc-dc converters with low common-mode noise by using split-winding configuration," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 452–461, 2022. DOI: 10.1109/TPEL.2021.3095106.

[13] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 6, pp. 1095–1099, 2003. DOI: 10.1109/TIE.2003.819677.

[14] P. Kong, S. Wang, F. C. Lee, and Z. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1522–1533, 2011. DOI: 10.1109/TPEL.2010.2082566.

[15] D. Zhao, X. Pei, Y. Yu, and J. Yan, "Cm noise modeling and reduction for multi-output dual-switch flyback auxiliary power supplies," *IEEE Transactions on Industry Applications*, vol. 61, no. 1, pp. 429–438, 2025. DOI: 10.1109/TIA.2024.3476246.

[16] M. Perotti and F. Fiori, "Investigating the EMI mitigation in power inverters using delay compensation," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4270–4278, 2019. DOI: 10.1109/TPEL.2018.2858015.

[17] E. Raviola, M. Roman, L. Zai, and F. Fiori, "Reduction of cm conducted emission with a small dummy leg and the delay compensation technique," in *2023 IEEE Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMC+SIPI)*, 2023, pp. 542–547. DOI: 10.1109/EMCSIPI50001.2023.10241590.

[18] M. Fishta, E. Raviola, and F. Fiori, "EMI reduction at the source in wbg inverters: A comparative study of spread-spectrum modulation and auxiliary switching leg techniques," *IEEE Transactions on Electromagnetic Compatibility*, vol. 66, no. 5, pp. 1412–1419, 2024. DOI: 10.1109/TEMC.2024.3436577.

[19] *CISPR 25:2021 - Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers*, International Standard, Dec. 2021.

[20] H. Hackl, J. R. Lopera, D. Klien, M. Gholizadeh, S. Sadeghi, and B. Auinger, "On the simulation of conducted emission of a flyback converter using ltspice," in *2024 International Symposium on Electromagnetic Compatibility – EMC Europe*, 2024, pp. 682–687. DOI: 10.1109/EMCEurope59828.2024.10722256.

[21] "Stth208-y automotive 800 v, 2 a ultrafast diode. "[Online]. Available: https://www.st.com/en/diodes-and-rectifiers/stth208-y.html.

[22] "Gs-065-004-1-l 650v enhancement mode gan transistor. "[Online]. Available: https://gansystems.com/gan-transistors/gs-065-004-1-l/.

[23] "Stth3002 200 v, 30 a ultrafast diode. "[Online]. Available: https://www.st.com/en/diodes-and-rectifiers/stth3002.html.

[24] Analog Devices, Inc., *LTspice XVII – SPICE Simulation Software*, Accessed: 2024-02-23, 2024. [Online]. Available: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html.

[25] T. K. C. F. S. Bendicks Andreas; Dörlemann, "MATLAB/Octave function to evaluate time-domain signals according to the measurement bandwidth and average/peak detector of EMI test receivers," in *Proceedings Conference Electromagnetic Compatibility, Cologne, Germany*, Jul. 2022, pp. 459–466. DOI: https://doi.org/10.15488/12605.