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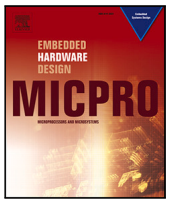

Extended design and linearity analysis of a 6-bit low-area hybrid ADC design for local system-on-chip measurements

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ABSTRACT

The low observability of analog signals inside modern low-area system-on-chips (SoCs) results in an increasing need for Design for Testability (DfT) solutions. These solutions demand an optimal circuit design in terms of area, power consumption, and precision, with a focus on minimizing area overhead per SoC circuit blocks. To address this demand, we present a 6-bit, low-area Hybrid Analog-to-Digital Converter (ADC) that measures analog voltage inside SoCs locally. The proposed Hybrid ADC consists of two sub-ADCs: A 3-bit SAR ADC for coarse measurements and a 3-bit Flash ADC for fine measurements.

The advantage of the proposed ADC design is its low additional area cost to each IP of SoCs due to its specific design. It can also have a shared fine Flash part, which has the dominant area in the design. This ADC design converts the analog signals, which are difficult to read from SoC pins, to the digital domain, where they are easy to route and observe.

The suggested ADC is designed and analyzed using the 130 nm technology of Infineon, and it has a total area of 0.007 mm^2. The areas of the fine Flash and coarse SAR parts are 0.0015 mm^2 and 0.0042 mm^2 respectively. The Signal-to-Noise Distortion Ratio (SNDR) of the design is 37 dB, and the Figure of Merit (FoM) is 2.15 pJ/conv.

1. Introduction

The latest developments in the automotive field have led to a rising interest in automotive System-on-Chips (SoCs). These automotive SoCs are widely used in applications such as robotics, aerospace, and electric cars. The shrinking dimensions and increasing speed of the transistors mean they are more prone to physical defects. These physical defects cause errors, and the propagation of these errors results in failure in the final application. In safety-critical applications where failure is unacceptable, it is necessary to have robust mechanisms to test the circuit blocks inside SoCs [1].

Every SoC consists of several analog, digital, and analog/mixed-signal circuit blocks; for each block type, there are techniques to test them [2]. In order to test the analog circuit blocks inside SoCs, one of the commonly used solutions in industry is the Analog Test Bus (ATB) [3–5]. More innovative methods leverage the same scan chain concept for the analog circuits [6,7]. Some other methods propose a Built-in Self-Test (BIST) for self-testing of the Analog circuits, such as Analog to Digital Converters (ADCs) or Phase-Locked Loops (PLLs) [2]. Moreover, there are some attempts to use design for testability (DfT) methods by adding hardware to test the analog circuits [8,9]. In order to test the digital circuits, there are many methods, such as scan chains [10] or the functional test used for testing different parts of the CPUs [11,12]. The presented works are summarized in Fig. 1.

However, the available methods for testing analog circuit blocks face challenges such as controllability and observability over analog signals [13]. ATB architecture has multiple long analog routings, and due to the shrinking transistor dimensions and overall chip die area, routing analog signals around the chip is more demanding. This problem stems from the susceptibility of these analog signals to noise and cross-talk [14].

In our previous work [15], a preliminary design of a low-area hybrid ADC architecture was introduced. In this work, we added extensive analysis to the proposed ADC. The proposed ADC has a very low die area so that it can be used efficiently inside SoCs close to the analog circuit blocks. This novel ADC design is a hybrid ADC made of two small ADCs to perform coarse and fine measurements using SAR and flash ADCs, respectively, inside the chip. The main advantage of this design is the low area overhead for circuit blocks inside SoCs. This low area overhead per IP is because when it is added to SoCs, we can insert a small 3-bit SAR ADC per IP, which has a very low area, then share the 3-bit Flash ADC used for fine measurement among the IPs because of its dominant contribution to the area of the proposed design.

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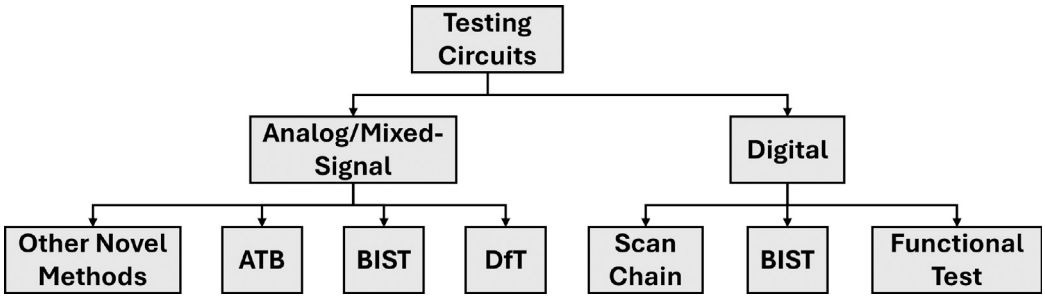

Fig. 1. The State-of-the-art for Testing.

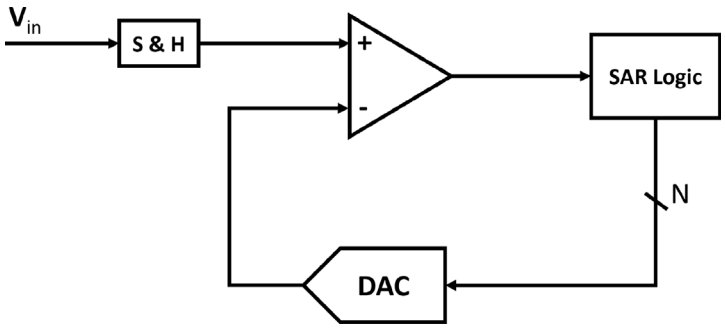

Fig. 2. Schematic presentation of the SAR ADC architecture.

In this design, analog signals are considerably shorter than the ATB approach. Moreover, converted values are in the digital domain, which makes them easier to route. The result of the conversion can be used by the user or Automated Test Equipment (ATE) to test the analog circuit blocks. The main contributions of this work are:

- Design a low-area hybrid ADC with a shareable fine part feature for local digitalization of the analog signals inside SoCs.
- Propose an efficient methodology for optimal placement of the proposed ADC inside SoC with a minimal area overhead per IP. The proposed approach will have a minimal area overhead of a 3-bit SAR ADC with the area of $0.0015\,mm^2$.
- Extend the analysis of the proposed hybrid ADC to a possible application on SoCs in terms of area, and analyze INL and DNL metrics.

The rest of the article outlines the fundamentals of the SAR and flash ADCs and ATB in Section 2. After explaining the basic concepts in Section 3, we present the proposed ADC design in detail. Then, in Section 4, the proposed approach's performance is evaluated and compared with the available designs in the state-of-the-art. Lastly, we conclude the work in Section 5.

2. Background

This part of the work provides the essential groundwork required to identify the different ADCs and ATB circuits and critically examine their respective limitations and advantages. By exploring these constraints, we are better positioned to suggest innovative strategies to alleviate or completely resolve the identified issues.

2.1. Successive approximation register (SAR) ADC

Fig. 2 provides the fundamental architecture of a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) circuit. This circuit comprises four integral subcircuits:

1. **Sample and Hold (S/H) Unit:** This module takes in the analog voltage, holds it constant, and forwards this stable input to the comparator for evaluation.
2. **Digital-to-Analog Converter (DAC):** The DAC is crucial for converting the tentative digital output of the SAR logic back into an analog signal for comparison against the held sample.
3. **Comparator:** Acting as the decision-maker, the comparator receives the held analog voltage at its positive terminal and the analog output from the DAC at its negative terminal, comparing the two voltages.
4. **SAR Logic Circuit:** As shown in Fig. 3, it is the digital brain of the operation, which controls the DAC and interprets the comparator's results to refine the digital output iteratively.

The SAR ADC employs the binary search method to narrow down possible values for the digital output. This process results in the correct representation bit by bit until the conversion is complete. Each step refines the approximation, leading to a precise digital equivalent of the input analog signal.

The output voltage is generated through the algorithm depicted in Fig. 4. This approach obtains digital output following the steps below:

1. **Initialization:** Firstly, we set the most significant bit (MSB) in the digital code to one. This is done by setting the RST signal of the SAR logic circuit presented in Fig. 3.
2. **Comparator Decision:** Output of the comparator decides to retain the MSB at its current value (one) or to reset it to zero. The comparator output is the COMP pin in SAR logic.
3. **Subsequent Approximations:** The algorithm estimates the next significant bit once the MSB is set. This estimation is done by assigning a value of one to the MSB-1 bit and observing the comparator's response.
4. **Bitwise Iteration:** The bitwise iteration happens thanks to the ring counterpart of the SAR logic. (4 flip-flops on top in Fig. 3)
5. **Finalization of Conversion:** This iterative process ends with evaluating the least significant bit (LSB). Determining the LSB's value marks the end of the conversion cycle, and we obtain the final digital code that represents the original analog input voltage.

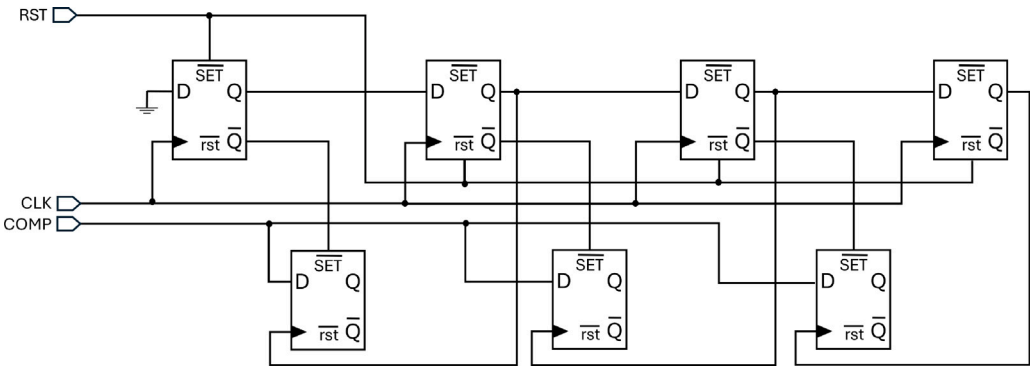

Fig. 3. SAR logic circuit design.

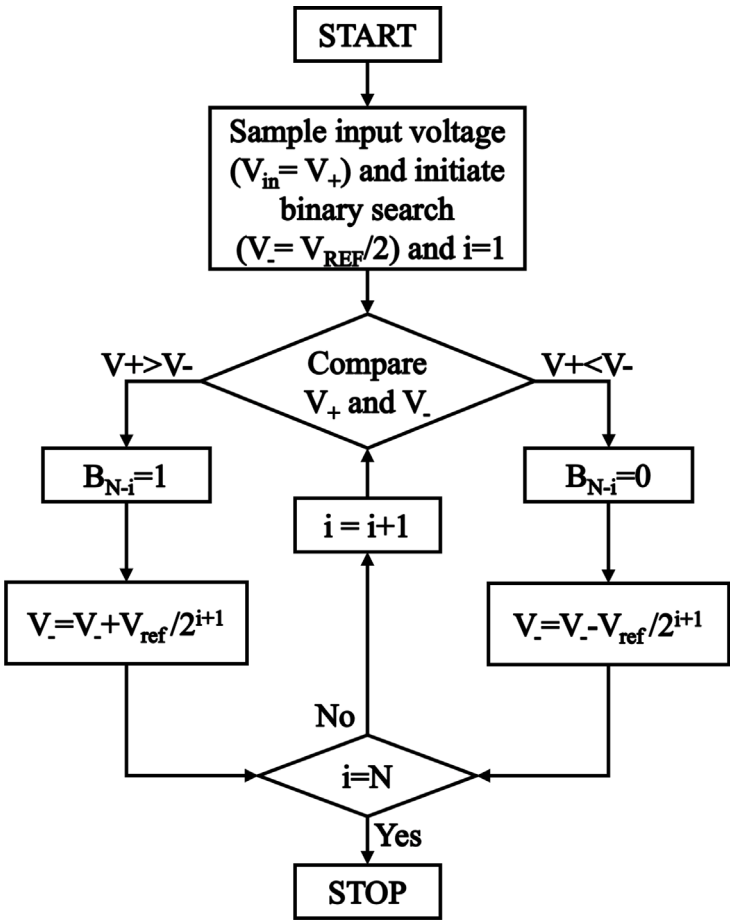

Fig. 4. Algorithm of SAR ADC.

The main advantage of the SAR ADC is its low area with relatively fast conversion speed. However, SAR ADCs have limitations when the number of output bits and the sampling frequency increase. One of the error sources is related to the comparators used in ADC circuits. Works like [16,17] put effort into mitigating this error source and lowering power consumption as much as possible. Another error source is the quantization error in the DAC circuit and its saturation when input codes are close to the high maximum code. To address the errors related to DAC accuracy, it is necessary to establish calibration mechanisms and mitigate process variation effects. Implementation of these calibration mechanisms mentioned in [18,19] results in higher area overhead. This high area prevents the precision of the output code from growing more than 10,12 bits.

2.2. Flash ADC

The flash ADC is another type of ADC architecture. The circuit schematic of the classic flash ADC is provided in Fig. 5. A flash ADC consists of a linear voltage divider, numerous comparators, and a decoder circuit. For each generated voltage by the voltage divider, there is a comparator that compares the input voltage with the generated voltage levels [20,21]. There are comparators and voltage levels. The voltage divider is based on the voltage division based on a ladder made by resistors or capacitors. Once all the comparisons are done, the comparator outputs go to a decoder circuit, which generates the output code.

The delay of this circuit is only one clock cycle, and the area increases exponentially with output bit number. This exponential increase

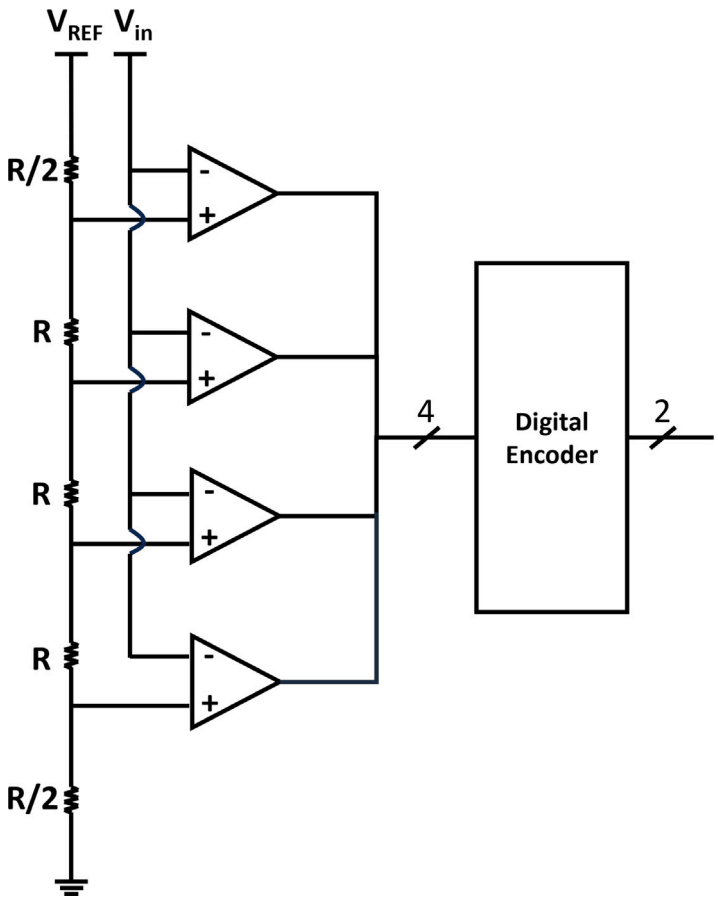

Fig. 5. Flash ADC circuit schematic.

in the area results in limiting the number of output bits in the SoCs, and the extra cost of the area is not acceptable.

2.3. Analog test bus (ATB)

The ATB design facilitates connecting analog blocks within SoCs for testing purposes. The Fig. 6 provides a visual guide to a general view of the ATB architecture. ATB architecture includes analog switches, known as Analog Test Points (ATPs), which select the analog signal and its direction from each block. Moreover, the internal connections that carry these signals and a central unit that controls the entire operation.

At the heart of ATBs, a comprehensive unit houses the necessary switches to choose the proper analog signal, a control module. This unit also guides the AMUX selection for the desired intellectual property (IP) signal. Also, an Analog-to-Digital Converter (ADC) translates analog signals into their digital counterparts. The digital signals are accessible from the SoCs' test pins, making them available from external Automatic Test Equipment (ATE).

Within the layout of the ATB, the analog routings are especially susceptible to noise. This noise often arises from the signal traces' inherent parasitic capacitance and inductance. This susceptibility to interference is observed when specific IPs, such as switching regulators and phase-locked loops (PLLs), generate high-frequency voltage spikes.

This noise affects the efficacy of the ATB and leads to a degradation in the overall performance of the ATBs [13]. Implementing strategies for digitization at a local level is essential to mitigate these performance issues. Furthermore, adopting alternative approaches, such as using voltage buffers across the SoC, could prove beneficial. However, these solutions demand a considerable trade-off concerning the chip's area.

2.4. Related work

One of the pioneer works in designing BIST circuits for detecting jitter and delays in PLLs was done by [22]. Another BIST design is proposed by [23] for testing integrated operational amplifiers. This work proposed the vectorless test solution, which is known as the oscillation test, and they used this method to test op amps. In [23], the authors treated the op amp as an oscillator circuit, and based on the oscillation frequency, they monitored the faults.

Works like [3,24] have been the works that developed ATB design and gradually improved the design to be used for every component in SoCs. Their proposed method increases the testability and enables debug/diagnosis facilities. Also, the proposed ATB architecture enables an automated test development flow. Recently, there has been a focus on digitalization of the whole testing process and using the methodologies for testing digital circuit blocks, such as scan [7]. In [7] work, the authors applied the tests using the digital ATE and IEEE 1687 (IJTAG) networks.

Another inspiring attempt to improve the ATB design was made by [25] authors. The authors aimed at splitting the SAR ADC architecture in order to perform the local digitalization following the IEEE 1687 standard. In order to use a proper SAR ADC circuit in [25], there are works mentioned in [26] alongside novel works like [27,28].

3. Proposed approach

This section presents the proposed hybrid ADC design and explains its functionality. The proposed circuit, depicted in Fig. 7, shows the schematic of the hybrid ADC circuit. The hybrid ADC in this work is for local measurement of the analog signals inside SoCs.

The proposed circuit can be split into two elements:

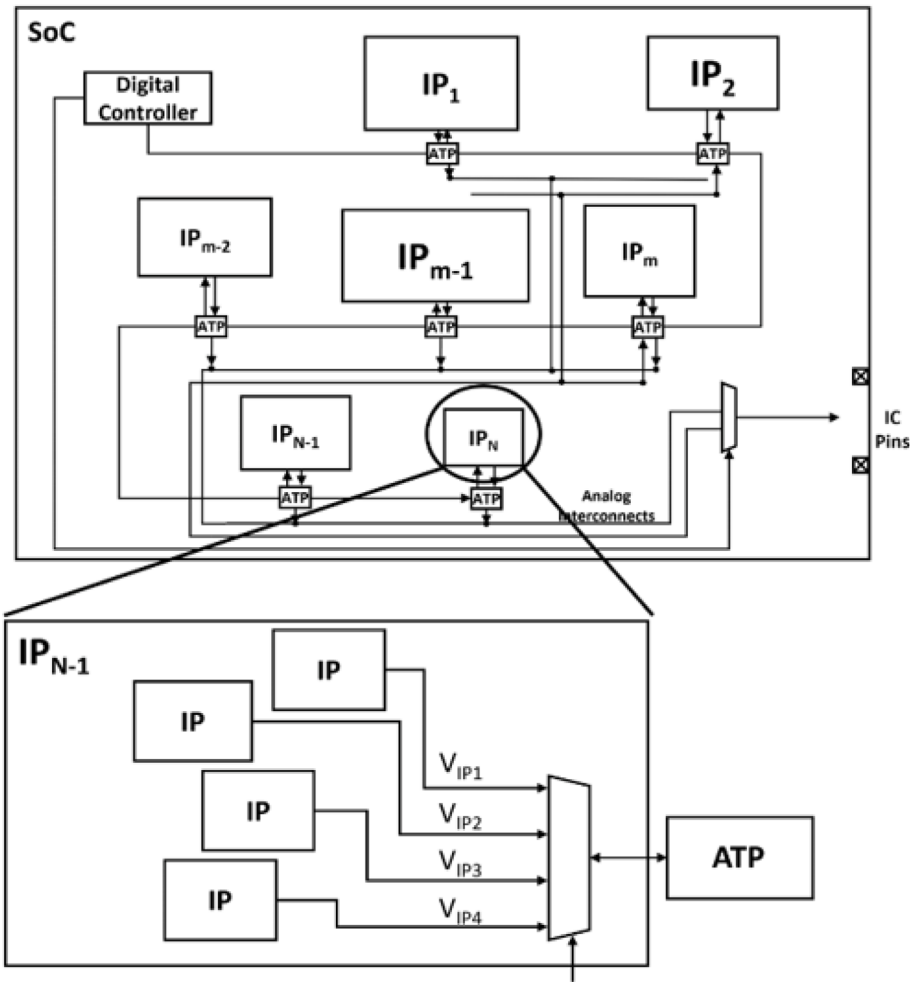

Fig. 6. A simple schematic of the ATB.

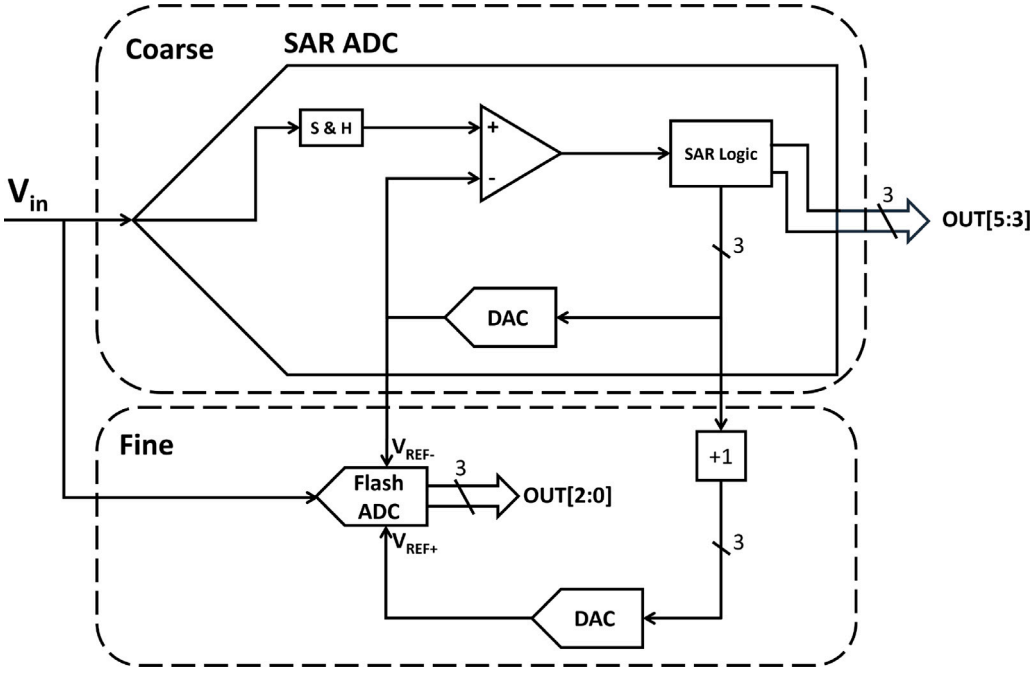

Fig. 7. The proposed hybrid ADC circuit schematic.

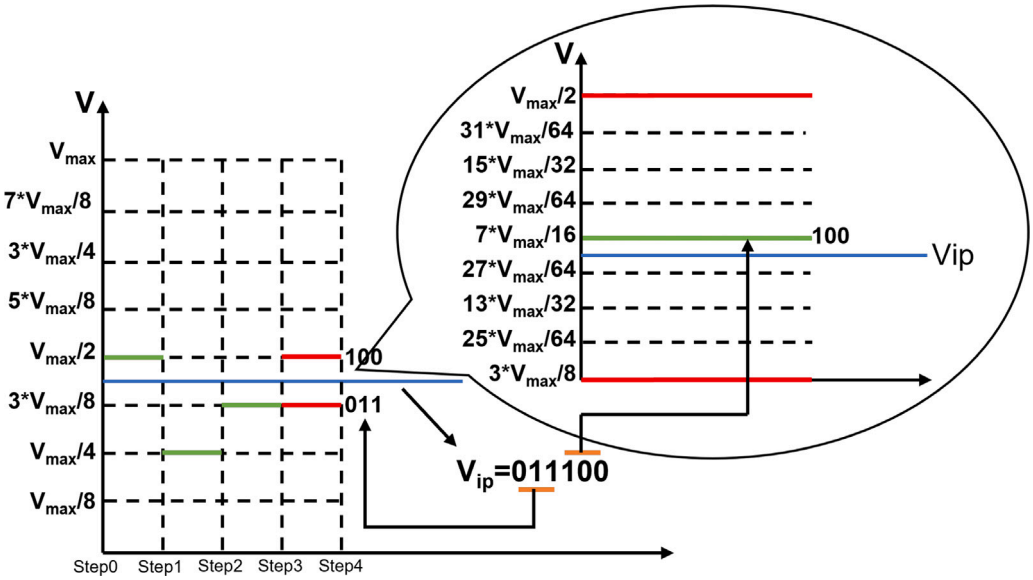

Fig. 8. An example of the measurement in the proposed hybrid ADC.

1. **The SAR ADC:** This circuit is used for the coarse measurement of the DC signal. This circuit provides the Most Significant Bits (MSBs).
2. **The flash ADC:** This circuit is used for the fine measurement. The flash circuit provides the Least Significant Bits (LSBs).

Inside an SoC, this circuit can be divided into two parts. As provided in Fig. 7, each IP can have a low area SAR ADC for coarse measurement and a shared Flash ADC for fine measurements. This section provides more details about the proposed circuit and then explains how to split the proposed hybrid ADC circuit for SoC measurements.

3.1. Hybrid ADC

The design of the proposed ADC converts analog voltages from analog circuit blocks inside SoCs through a two-step process consisting of coarse and fine measurements. The SAR and flash ADCs are used to measure the 3 MSBs and 3 LSBs, respectively. The reason behind choosing six bits for the ADC design is because of the limitations on additional area per IP and the required accuracy. Considering the area overhead limitation per IP, we decided to keep the resolution of the SAR ADC limited to 3 bits. This decision also addresses the accuracy drop in SAR ADCs that occurs with increasing the number of output bits. On the other hand, the area in Flash ADC increases exponentially with the number of bits. Thus, we decided to limit the output bit number for the flash ADC to 3 bits, besides leveraging the fast conversion of the flash ADC. Besides, having 6-bit accuracy given a voltage range of 1.5 V provides an acceptable precision.

The conversion happens following these steps:

- In the coarse conversion, as detailed in Fig. 8, the SAR ADC is responsible for generating the three MSBs of the digital output.
- Subsequently, the coarse conversion output, which are 3 MSBs of the final digital output, are incremented by ‘001’ (equivalent to “+1” as visualized in Fig. 7). By incrementing the digital output of the coarse SAR ADC, we establish the positive and negative reference values for the next phase.
- The incremented reference values go into two separate Digital-to-Analog Converters (DACs), as indicated in Fig. 7. These DACs set the positive and negative reference voltages for the final conversion stage.
- The fine conversion occurs with the Flash ADC taking the positive and negative reference voltages defined by the DACs to compute the three LSBs precisely.
- Once the Flash ADC has resolved the 3 LSBs, the digital conversion is deemed complete, ending in the full digital representation of the original analog input.

Typically, the number of bits in a SAR ADC is limited to 10,12 bits with a low hardware cost. This limitation is because of the need for a high-precision reference voltage. Moreover, we have an additional area due to the calibration of the DAC.

The area of the flash ADC is higher than the SAR ADC, based on the dominant contribution of the comparators to the area of the ADC circuits. In a flash ADC, the number of comparators is exponential to the power of two of the number of bits, but the SAR ADC has the same number of comparators for any number of bits.

One advantage of the proposed hybrid approach is that it enables the fast generation of the pass/fail signal, which can be used to test the analog signals inside each IP. Generally, there is a pass range for the analog signals inside IPs. Using the coarse conversion of the hybrid architecture enables pass/fail signal generation by comparing the coarse conversion value with the pass range value.

3.2. Shared flash ADC

In order to have the proposed hybrid ADC functioning in SoCs, one idea is to use the entire ADC circuit inside IPs. However, this idea will have an enormous area overhead for each IP and generally for the whole SoC design. This area overhead in SoCs has a high cost, which is not affordable. In order to address this challenge, we propose to share the flash part of the proposed hybrid ADC. The fine part in this design is the Flash ADC, which has a higher area with respect to the coarse part, which is a SAR ADC. Therefore, in terms of additional area per IP, we can limit it only to a 3-bit SAR ADC.

As shown in Fig. 9, the proposed design for sharing the flash part of the ADC is slightly different from the proposed hybrid ADC in Fig. 7. In Fig. 7, the negative reference voltage comes directly from the DAC inside the SAR ADC. This signal is analog, and the main effort is to reduce the analog routing as much as possible. Thus, in Fig. 9, instead of passing the DAC output through an analog multiplexer, the digital output of the coarse SAR ADCs is passed to a digital multiplexer. In this case, with the cost of an extra DAC, we reduce the analog routings

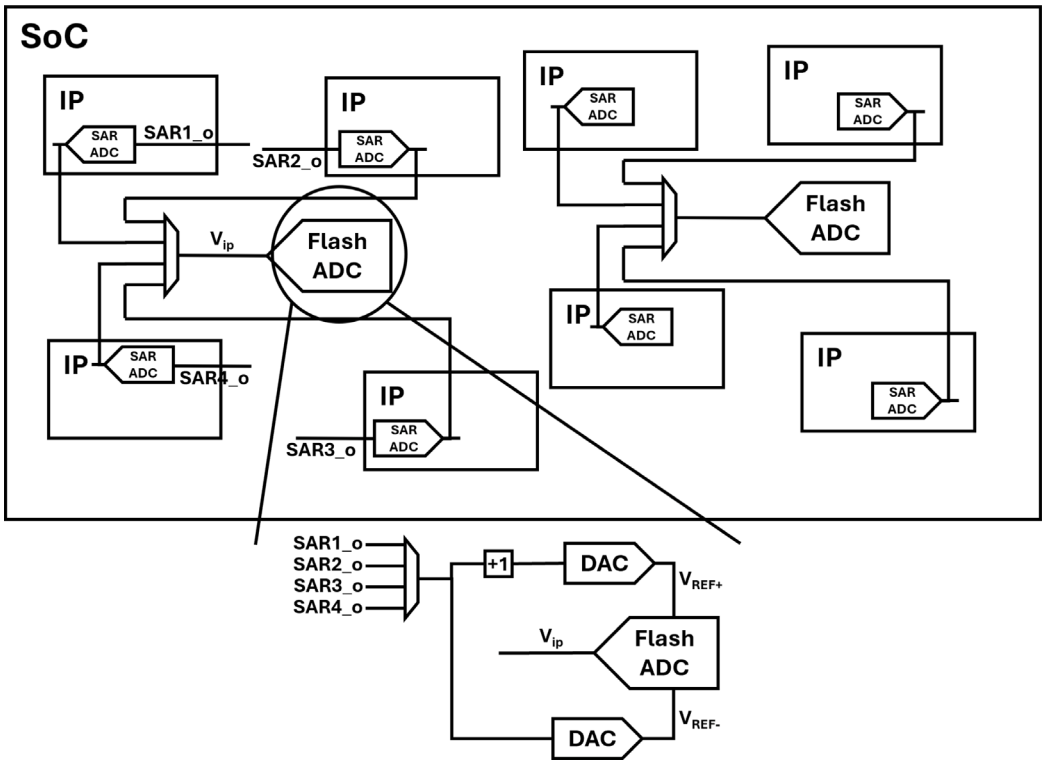

Fig. 9. Schematic of the sharing fine part of the hybrid ADC.

and provide a more stable reference voltage for the fine conversion. Therefore, we can use this architecture to measure the analog signals inside SoCs instead of the classical ATB approach.

In the proposed design, it is possible to schedule the analog signals to be measured by controlling the select signal of the multiplexers presented in Fig. 9. The most straightforward solution is to have a round robin approach and measure the analog signals periodically. However, this scheduling methodology can be modified based on the importance of the analog signals inside SoCs. The modified scheduling can prioritize the more crucial analog signals more frequently and before the other analog signals.

It is notable that, using this approach, we do not eliminate the analog routings completely from SoCs, but we decrease the length of analog routings significantly by local digitalization.

Table 1
Performance analysis of the proposed ADC.

Technology	130 nm
Total Area	0.007 mm^2
Coarse part area (Area per IP)	0.0015 mm^2
Fine part area	0.0042 mm^2
Sampling frequency	10 MHz
# Bits	6
Supply voltage	1.5 V
Total Power consumption	1.12 mW
Flash Power consumption	0.85 mW
SAR Power consumption	0.27 mW
FoM	2.15 pJ/conv
SNDR	37 dB
DNL	+0.50/−0.45 LSB
INL	+0.85/−0.67 LSB

4. Experimental results

This section reports the essential characteristics of the hybrid ADC design proposed in this work. These characteristics are area, number of bits, integration technology, etc. Then, we compare the proposed design with the other state-of-the-art designs.

4.1. Performance evaluation

The proposed hybrid ADC design is implemented using the Infineon 130 nm CMOS technology. The supply voltage of the ADC architecture is 1.5 V, and the accuracy of the ADC is 20 mV. The total area of this design is 0.007 mm^2, and the area occupied by the SAR part of the ADC is 0.0015 mm^2. Meanwhile, the area occupied by the flash ADC is 0.0042 mm^2. The rest of the area is occupied by the +1, and the DAC circuit is used to provide the high and low supplies of the flash ADC. This ADC has a power consumption of 1.12 mW and a Figure-of-Merit(FoM) of 2.15 pJ/conv.

The FoM is an important parameter when we want to compare different ADC architectures to each other [26]. This parameter combines the power consumption(P), sampling frequency(f_s), and accuracy as the main parameters needed in real-world applications. The formula used for FoM computation is presented in (1).

$$FoM = \frac{P}{2^{ENOB}.f_s} \tag{1}$$

In order to show the accuracy and linearity of the proposed hybrid ADC, we present Differential-Non-Linearity (DNL) in Fig. 11 and Integral-Non-Linearity (INL) in Fig. 10. According to the maximum and minimum results of the DNL and INL, which are +0.50/−0.45 LSB and +0.85/−0.67 LSB, respectively. We can conclude that the resulting converter is guaranteed to be monotonic.

The brief of performance analysis of the proposed ADC circuit is provided in Table 1.

4.2. Comparison with state-of-the-art

In this section, in order to have a clearer idea about the presented ADC's performance, we compare the ADC in this work with similar architectures in terms of precision and topology found in the state-of-the-art. In Table 2, the proposed hybrid ADC is compared in parameters

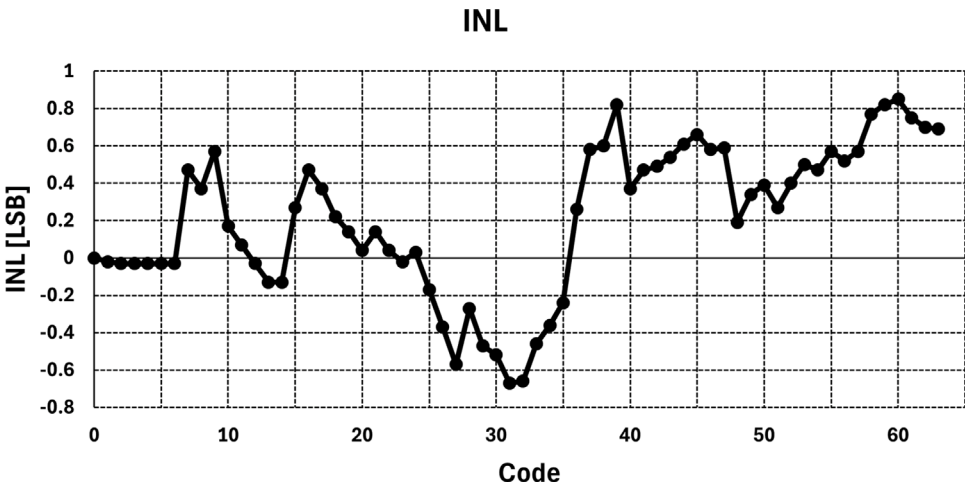

Fig. 10. Integral Non-Linearity of the proposed ADC design.

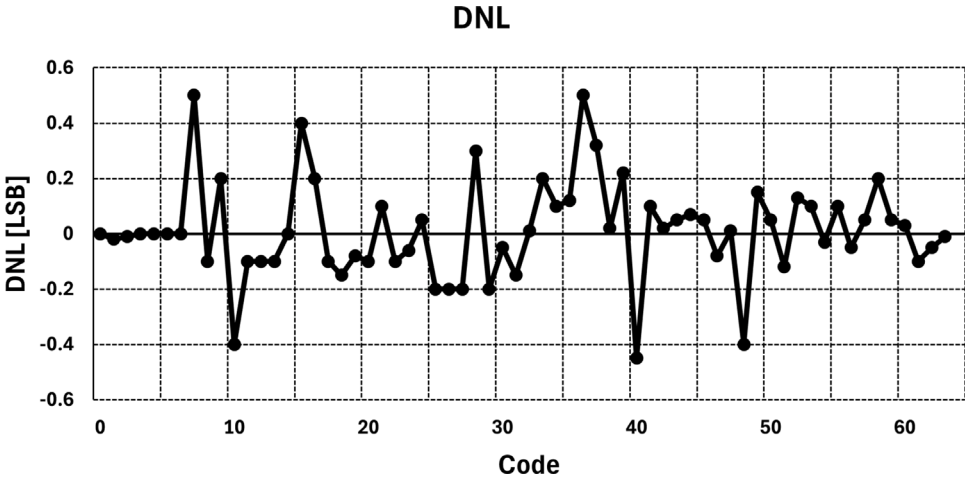

Fig. 11. Dynamic Non-Linearity of the proposed ADC design.

such as area, Signal-to-Noise Distortion Ratio (SNDR), Figure of Merit (FoM), power consumption, INL, DNL, and number of bits.

To more accurately evaluate the ADC area efficiency, we tried to have all of the ADCs use the same integration technology. Generally, the area does not scale linearly with the integration technology in mixed-signal circuits. Regarding the area, the proposed ADC design has a remarkable area efficiency with a total area of $0.007\,mm^2$. The closest competitor to the proposed design is the design of the [29] with a die area of $0.03\,mm^2$, considering that it is implemented in 28 nm integration technology.

The Table 2 indicates a standardization at 6 bits for most ADCs, including the proposed work, which is adequate for applications that do not require high-resolution conversions. Two ADCs [30,31] offer higher resolution at 10 bits, catering to applications necessitating greater precision.

The proposed ADC achieves an SNDR of 38 dB, outperforming several counterparts like those referenced in [29,30,34] and showing a moderate improvement. It is, however, surpassed by ADCs [27,33,34], which present exceptionally high SNDR values above 47 dB, indicative of superior noise performance and precision. The proposed ADC reports a competitive FoM of 2.15 pJ/conv, which measures energy efficiency per conversion. It is on par with some other designs but is outclassed by ADCs [27,29,31,33,34]. This performance demonstrates exceedingly low power consumption per conversion, with [27] having an impressive FoM of 0.015 pJ/conv.

In terms of power, the proposed ADC is highly efficient, consuming only 1.12 mW, which is significantly lower than most of the compared works, except for [27,31,33]. These two ADCs exhibit ultra-low power consumption, but at the expense of higher area and lower technology nodes.

One important feature reported in Table 2 is the splitability of the presented designs. Except for the presented design, none of the other designs have this characteristic. Therefore, to use the other designs provided in Table 2, it is necessary to insert one ADC per IP. This insertion results in a high area overhead in SoCs with a lot of IPs, which makes it extremely costly and inefficient. As presented in Fig. 12, the area overhead in all of the ADCs available in the state-of-the-art, in case of adding one ADC per IP, comes with a minimum additional area of $3\,mm^2$. However, the splitability of the proposed ADC design optimizes the additional area to SoCs overwhelmingly by at least 10 times.

In summary, the proposed ADC offers an excellent balance between size, power consumption, and performance, with a particular advantage in its compactness. The proposed design does not lead in every category, such as SNDR or FoM, where the 10-bit ADCs outperform it. However, the overall specifications suggest that we proposed a competitive design in the context of low-power and space-efficient applications. This analysis underscores the trade-offs inherent in ADC design, highlighting that the best choice of ADC architecture depends on the specific requirements of the intended application.

Table 2
Comparison of the proposed ADC with the state-of-the art.

	[32]	[30]	[33]	[31]	[34]	[29]	[27]	This work
Architecture	Flash	Flash	Hybrid ***ST	Hybrid **SF	Hybrid SAR	*TI Hybrid	SAR	Hybrid SAR
F_s (MHz)	1200	1600	0.25	1000	0.2	2400	0.1	10
Area (mm^2)	0.12	0.13	0.04	N/A	0.097	0.03	N/A	0.007
#Bits	6	6	10	6	10	6	8	6
SNDR (dB)	35.5	30	53.7	35.56	56.91	34.8	47.11	38
Technology (nm)	130	130	90	28	180	28	130	130
FoM# (pJ/conv)	2.2	2.6	0.002	0.048	0.015	0.021	1.66e−3	2.15
ENOB	5.92	5.44	8.63	5.61	9.16	5.50	7.05	5.70
Power (mW)	160	180	0.0002	2.33	0.002	23	22e−6	1.12
DNL (LSB)	< 0.4	+0.49/−0.49	0.43	+0.47/−0.38	+0.27/−0.21	+0.25/−0.19	N/A	+0.50/−0.45
INL (LSB)	< 0.6	+0.42/−0.42	0.63	+1.10/−0.75	+0.43/−0.45	+0.18/−0.22	N/A	+0.85/−0.67
Splitability	No	No	No	No	No	No	No	Yes

*TI: Time-Interleaved, **SF: SAR Flash, ***ST: SAR Time-domain, F_s: Sampling Frequency, #:FoM = $\frac{Power}{2^{ENOB}.f_{sample}}$.

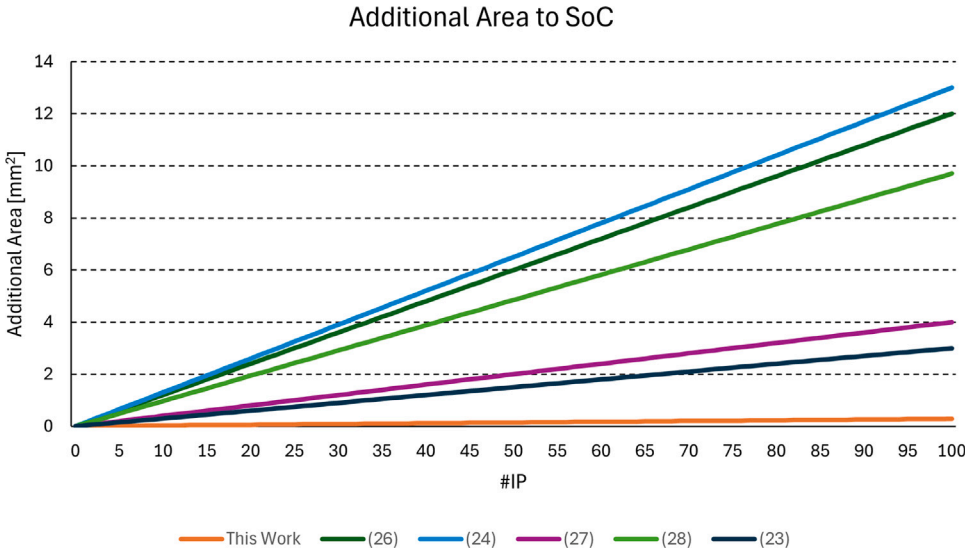

Fig. 12. Comparison of the additional area based on the number of the IPs in SoCs.

4.3. Discussion

In order to have a higher precision, it is possible to increase the number of bit in the SAR or flash ADC parts of the proposed approach. However, considering the trade-off between area, power consumption, and precision, increasing the number of bits up to 10 bits would result in a very high area overhead. Increasing the number of SAR ADC bits requires an excessive area per IP, which depends on the requirements of producers of SoCs. On the other hand, increasing the number of flash ADC bits results in an exponential area increment, which is often not practical.

Another aspect to be discussed is the usage of the proposed approach. The initial idea is to have this design used during the production test. Moreover, the proposed hybrid ADC can also be used for in-field applications. But, to use the proposed design for in-field applications, it is necessary to consider how aging would affect the ADC circuit behavior over time. Characterizing the behavior of the ADC architecture under the aging effect requires extensive analysis of the component. Probably reducing the sampling frequency to mitigate the aging effect. Also, how the process variation should be tolerated to have more reliable on-chip measurements. For this reason, it is possible to calibrate the voltage supply of the proposed ADC by trimming the reference voltage generators available on SoCs.

5. Conclusion

This work presented a new hybrid ADC design to measure the analog voltages inside the circuit blocks of SoCs. This design is implemented in the 130 nm CMOS technology. The total area of the ADC is 0.007 mm^2, and the additional area per peripheral is 0.0015 mm^2. The presented design has a DNL and INL of +0.50/−0.45 LSB, +0.85/−0.67 LSB, respectively. The total area of this design is close to that of similar ADCs available in the state of the art. However, because of its unique feature, which is the shareability of the flash ADC part of the ADC, there is a low area overhead per peripheral, and the provided area evaluation was in line with the estimated outcome.

The proposed ADC design reduces the length of analog routings significantly, combining the local digitalization and sharing the flash ADC part of the ADC concepts; however, it does not eliminate the analog routing on SoCs entirely.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: The work presented in DTTIS 2024 has been extended without support from Infineon Technology AG, and we decided to remove their names from the extended article. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

References

[1] P. Bernardi, L. Bolzani, M. Rebaudengo, M. Reorda, F. Vargas, M. Violante, A new hybrid fault detection technique for systems-on-a-chip, IEEE Trans. Comput. 55 (2) (2006) 185–198, http://dx.doi.org/10.1109/TC.2006.15.

[2] A. Pavlidis, M.-M. Louërat, E. Faehn, A. Kumar, H.-G. Stratigopoulos, SymBIST: Symmetry-based analog and mixed-signal built-in self-test for functional safety, IEEE Trans. Circuits Syst. I. Regul. Pap. 68 (6) (2021) 2580–2593, http://dx.doi.org/10.1109/TCSI.2021.3067180.

[3] S. Sunter, A low cost 100 MHz analog test bus, in: Proceedings 13th IEEE VLSI Test Symposium, 1995, pp. 60–65, http://dx.doi.org/10.1109/VTEST.1995.512618.

[4] S. Sunter, The P1149.4 mixed signal test bus: costs and benefits, in: Proceedings of 1995 IEEE International Test Conference, ITC, 1995, pp. 444–450, http://dx.doi.org/10.1109/TEST.1995.529871.

[5] E.R. da Silva, F. Costa, F.H. Behrens, R.S. Kickhofel, R. Maltione, Analog test bus architecture for small die size and limited pin count devices with internal IPs testability emphasis, in: 2009 10th Latin American Test Workshop, 2009, pp. 1–6, http://dx.doi.org/10.1109/LATW.2009.4813800.

[6] R. Vasudevamurthy, P.K. Das, B. Amrutur, A mostly-digital analog scan-out chain for low bandwidth voltage measurement for analog IP test, in: 2011 IEEE International Symposium of Circuits and Systems, ISCAS, 2011, pp. 2035–2038, http://dx.doi.org/10.1109/ISCAS.2011.5937996.

[7] S. Sunter, K. Jurga, Digital scan and ATPG for analog circuits, in: 2024 IEEE International Test Conference, ITC, 2024, pp. 339–347, http://dx.doi.org/10.1109/ITC51657.2024.00055.

[8] S. Mosin, An approach to design-for-testability automation of analogue integrated circuits using OBIST strategy, in: 2016 5th Mediterranean Conference on Embedded Computing, MECO, 2016, pp. 211–214, http://dx.doi.org/10.1109/MECO.2016.7525742.

[9] M. Ince, B. Bilgic, S. Ozev, Digital fault-based built-in self-test and evaluation of low dropout voltage regulators, J. Emerg. Technol. Comput. Syst. 18 (3) (2022) http://dx.doi.org/10.1145/3510852.

[10] R. Gupta, M. Breuer, Ordering storage elements in a single scan chain, in: 1991 IEEE International Conference on Computer-Aided Design Digest of Technical Papers, 1991, pp. 408–411, http://dx.doi.org/10.1109/ICCAD.1991.185289.

[11] A. Touati, A. Bosio, P. Girard, A. Virazel, P. Bernardi, M. Sonza Reorda, Microprocessor testing: Functional meets structural test, J. Circuits Syst. Comput. 26 (08) (2017) 1740007, http://dx.doi.org/10.1142/S0218126617400072.

[12] R. Cantoro, F. Garau, P. Girard, N. Kolahimahmoudi, S. Sartoni, M.S. Reorda, A. Virazel, Effective techniques for automatically improving the transition delay fault coverage of self-test libraries, in: 2022 IEEE European Test Symposium, ETS, 2022, pp. 1–2, http://dx.doi.org/10.1109/ETS54262.2022.9810392.

[13] N. Liu, S.K. Chaganti, Z. Liu, D. Chen, A. Majumdar, Concurrent sampling with local digitization — An alternative to analog test bus, in: 2018 IEEE International Symposium on Circuits and Systems, ISCAS, 2018, pp. 1–5, http://dx.doi.org/10.1109/ISCAS.2018.8351555.

[14] R.M.F. Martins, N.C.C. Lourenço, Analog integrated circuit routing techniques: An extensive review, IEEE Access 11 (2023) 35965–35983, http://dx.doi.org/10.1109/ACCESS.2023.3265481.

[15] N. Kolahimahmoudi, G. Insinga, S. Roggi, J. Niederl, P. Bernardi, A 6-bit low-area hybrid ADC design for system-on-chip measurements, in: 2024 IEEE International Conference on Design, Test and Technology of Integrated Systems, DTTIS, 2024, pp. 1–6, http://dx.doi.org/10.1109/DTTIS62212.2024.10780233.

[16] K.M. Abozeid, M.M. Aboudina, A. Khalil, Different configurations for dynamic latched comparators used in ultra low power analog to digital converters, in: 2014 International Conference on Engineering and Technology, ICET, 2014, pp. 1–6, http://dx.doi.org/10.1109/ICEngTechnol.2014.7016771.

[17] A. Khorami, M.B. Dastjerdi, A.F. Ahmadi, A low-power high-speed comparator for analog to digital converters, in: 2016 IEEE International Symposium on Circuits and Systems, ISCAS, 2016, pp. 2010–2013, http://dx.doi.org/10.1109/ISCAS.2016.7538971.

[18] A. Karanicolas, H.-S. Lee, K. Barcrania, A 15-b 1-msample/s digitally self-calibrated pipeline ADC, IEEE J. Solid-State Circuits 28 (12) (1993) 1207–1215, http://dx.doi.org/10.1109/4.261994.

[19] B. Murmann, B. Boser, A 12-bit 75-ms/s pipelined ADC using open-loop residue amplification, IEEE J. Solid-State Circuits 38 (12) (2003) 2040–2050, http://dx.doi.org/10.1109/JSSC.2003.819167.

[20] S. Weaver, B. Hershberg, U.-K. Moon, Digitally synthesized stochastic flash ADC using only standard digital cells, IEEE Trans. Circuits Syst. I. Regul. Pap. 61 (1) (2014) 84–91, http://dx.doi.org/10.1109/TCSI.2013.2268571.

[21] K. Uyttenhove, M. Steyaert, A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25-µm CMOS, IEEE J. Solid-State Circuits 38 (7) (2003) 1115–1122, http://dx.doi.org/10.1109/JSSC.2003.813244.

[22] S. Sunter, A. Roy, A mixed-signal test bus and analog BIST with 'unlimited' time and voltage resolution, in: 2011 Sixteenth IEEE European Test Symposium, 2011, pp. 81–86, http://dx.doi.org/10.1109/ETS.2011.22.

[23] K. Arabi, B. Kaminska, Design for testability of embedded integrated operational amplifiers, IEEE J. Solid-State Circuits 33 (4) (1998) 573–581, http://dx.doi.org/10.1109/4.663562.

[24] V.A. Zivkovic, F. van der Heyden, G. Gronthoud, F. de Jong, Analog test bus infrastructure for RF/AMS modules in core-based design, in: 2008 13th European Test Symposium, 2008, pp. 27–32, http://dx.doi.org/10.1109/ETS.2008.18.

[25] J. Pathrose, L. van de Logt, H.G. Kerkhoff, Analog test interface for IEEE 1687 employing split SAR architecture to support embedded instrument dependability applications, in: 2019 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, DFT, 2019, pp. 1–4, http://dx.doi.org/10.1109/DFT.2019.8875372.

[26] R. Walden, Analog-to-digital converter survey and analysis, IEEE J. Sel. Areas Commun. 17 (4) (1999) 539–550, http://dx.doi.org/10.1109/49.761034.

[27] K.M. Abozeid, M.M. Aboudina, A. Khalil, 8-bit 22nW SAR ADC using output offset cancellation technique, in: 2015 11th International Computer Engineering Conference, ICENCO, 2015, pp. 76–79, http://dx.doi.org/10.1109/ICENCO.2015.7416328.

[28] Y. Zhu, C.-H. Chan, U.-F. Chio, S.-W. Sin, S.-P. U, R.P. Martins, F. Maloberti, A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS, IEEE J. Solid-State Circuits 45 (6) (2010) 1111–1121, http://dx.doi.org/10.1109/JSSC.2010.2048498.

[29] B. Xu, Y. Zhou, Y. Chiu, A 23-mW 24-GS/s 6-bit voltage-time hybrid time-interleaved ADC in 28-nm CMOS, IEEE J. Solid-State Circuits 52 (4) (2017) 1091–1100, http://dx.doi.org/10.1109/JSSC.2016.2642204.

[30] A. Ismail, M. Elmasry, A 6-bit 1.6-GS/s low-power wideband flash ADC converter in 0.13-µm CMOS technology, IEEE J. Solid-State Circuits 43 (9) (2008) 1982–1990, http://dx.doi.org/10.1109/JSSC.2008.2001936.

[31] B.D. Kumar, H. Shrimali, N. Gupta, A 6-bit, 29.56 fj/conv-step, voltage scalable flash-SAR hybrid ADC in 28 nm CMOS, in: 2019 IEEE International Symposium on Circuits and Systems, ISCAS, 2019, pp. 1–5, http://dx.doi.org/10.1109/ISCAS.2019.8702482.

[32] C. Sandner, M. Clara, A. Santner, T. Hartig, F. Kuttner, A 6-bit 1.2-GS/s low-power flash-ADC in 0.13-/spl mu/m digital CMOS, IEEE J. Solid-State Circuits 40 (7) (2005) 1499–1505, http://dx.doi.org/10.1109/JSSC.2005.847215.

[33] Y.-J. Chen, C.-C. Hsieh, A 0.4V 2.02fJ/conversion-step 10-bit hybrid SAR ADC with time-domain quantizer in 90nm CMOS, in: 2014 Symposium on VLSI Circuits Digest of Technical Papers, IEEE, Honolulu, HI, USA, 2014, pp. 1–2, http://dx.doi.org/10.1109/VLSIC.2014.6858372.

[34] H. Zhang, H. Zhang, Y. Song, R. Zhang, A 10-bit 200-ks/s 1.76- µw SAR adc with hybrid CAP-mos DAC for energy-limited applications, IEEE Trans. Circuits Syst. I. Regul. Pap. 66 (5) (2019) 1716–1727, http://dx.doi.org/10.1109/TCSI.2019.2899162.

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