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Digital Control of Multilevel Interleaved GaN DC-DC Converter for Fuel Cell Electric Powertrains

Stefano Savio, *Graduate Student Member, IEEE,* Simone Giuffrida, *Graduate Student Member, IEEE,* Fabio Mandrile, *Member, IEEE,* Fausto Stella, *Member, IEEE,* Eric Giacomo Armando, *Senior Member, IEEE,* Radu Bojoi, *Fellow, IEEE*

***Abstract*—Fuel cells are increasingly recognized as a viable alternative to traditional battery packs in electric vehicles, particularly for long-distance transport requiring reduced weight and extended range. Despite their advantages, the low and load-dependent output voltage of fuel cell stacks (typically below 200 V) requires the use of high-efficiency boost DC-DC converters to achieve the required voltage (400-800V) for electric powertrains. In this context, gallium nitride (GaN) technology enables switching frequencies exceeding 100 kHz, making it a prime candidate for high-power, high-density DC-DC converters. The main focus of this paper is the development and implementation of an advanced digital control solution tailored to a high-power, multilevel interleaved GaN-based DC-DC converter operating at a 100 kHz switching frequency. The high switching frequency, while beneficial for reducing passive component sizes and improving transient response, introduces significant challenges in synchronization, sampling, and the precise control of multiple interleaved cells. Analog control systems struggle to handle these requirements effectively, motivating the adoption of a digital control strategy that ensures high performance and flexibility. Experimental validation is performed on a reduced-scale prototype, demonstrating the robustness of the control scheme under dynamic conditions, including voltage step changes and load transients. The results confirm the effectiveness of the proposed digital control strategy in maintaining accurate voltage regulation, current sharing, and capacitor balancing, even under the demanding operating conditions imposed by high switching frequencies.**

***Index Terms*—Fuel cells, digital control, DC-DC converters, Gallium Nitride (GaN), Multilevel converters.**

I. Introduction

Fuel cells (FCs) have gained considerable attention as a viable alternative to heavy and bulky battery packs in electric powertrains for trucks, buses, and commercial vehicles [1]–[5]. Thanks to their high energy density, FCs can address critical challenges associated with energy consumption in long-distance transportation. Unlike conventional battery systems, FCs offer a more sustainable and efficient solution, aligning with global efforts to reduce greenhouse gas emissions and dependency on fossil fuels [6]–[9]. Despite these advantages, the direct replacement of battery packs with fuel cell stacks is not straightforward due to the non-linear and inherently low voltage characteristics of FCs. Therefore, to enable their integration into electric vehicles, a boost DC-DC converter is typically employed as an electronic interface between the FC stack and the traction inverter [10], [11]. This configuration often integrates a smaller battery storage system, which manages peak power demands and enables regenerative braking, as illustrated in Fig. 1.

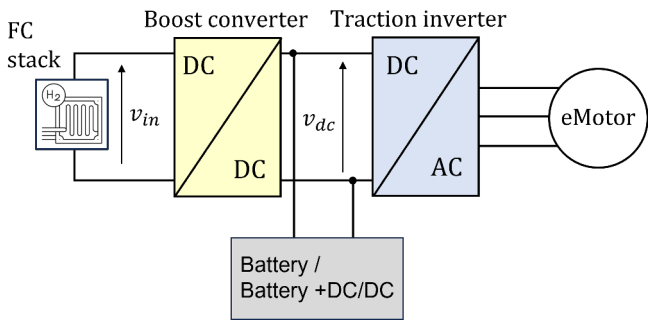


Fig. 1: FC powered electrical powertrain.

Traditional DC-DC boost converters are widely adopted due to their simplicity and cost-effectiveness. However, their performance becomes increasingly constrained as power and voltage requirements increase [12], [13]. With higher demands for power density and system efficiency, conventional boost converters suffer from reduced efficiency and reliability, especially in high-power applications. These limitations necessitate the exploration of advanced converter topologies capable of meeting stringent performance criteria while maintaining manageable levels of complexity.

One promising solution to overcome these challenges is the adoption of interleaved converter structures. Interleaving involves parallelizing multiple power conversion modules, resulting in several advantages: reduced input and output current ripples, higher effective switching frequency, and improved dynamic response [14]–[17]. Furthermore, this approach distributes the thermal load across multiple modules, enhancing the thermal management and overall reliability of the system. Consequently, interleaved configurations are increasingly regarded as a key enabler for achieving high power densities in FC-based powertrains.

In parallel with the introduction of new converter topologies, the introduction of wideband gap (WBG) devices to overcome the limitations of traditional silicon-based technology has opened new perspectives for improving overall performance [18]. Silicon devices, with their lower breakdown voltage and higher conduction and switching losses, struggle to meet the demands of high-power, high-frequency applications. Wide

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bandgap technologies, such as gallium-nitride (GaN), offer superior performance, enabling higher switching frequencies and reduced losses [19]. GaN-based devices are particularly attractive for high-frequency DC-DC converters for unprecedented switching performance leading to enhanced efficiency. However, commercially available high-power GaN devices are typically rated for voltages up to 650 V, posing challenges for applications requiring higher output voltages. To address these constraints, multilevel topologies are often adopted, albeit at the cost of increased system complexity [19].

Another critical aspect of high-frequency converter design are the magnetic elements. The elevated switching frequencies associated with WBG devices demand particular care in the design of the magnetic elements to mitigate losses and maintain efficiency. Coupled inductors, for instance, have emerged as a valuable solution to enhance power density and reduce costs [20]. However, these designs introduce additional challenges, particularly in the control and interleaved structure synchronization, as the converters operate above 100 kHz. Managing multiple interleaved cells requires precise digital control strategies, which must account for synchronization, low sampling time, and implementation of multiple cascaded control loops. While substantial research has focused on developing interleaved multilevel topologies for DC-DC converters [16], [17], [21]–[27], fewer studies have addressed the digital control of these advanced systems [28]. Effective control is essential to fully leverage the advantages of interleaved and multilevel structures, ensuring reliable and efficient operation in demanding applications.

Different control routines have been proposed for three-level boost converters (3LBC) in recent years, each targeting various applications and performance improvements. A notable control scheme for ultracapacitor applications is presented in [29], where a 25 kHz switching frequency with IGBT devices is achieved and validated through a 5.5 kW prototype. This control scheme features two control loops: a primary ultracapacitor current control loop and a secondary DC bus voltage balancing loop to ensure that the voltage across the split DC-link remains balanced. The voltage balancing loop is designed to compensate for any imbalances caused by capacitor leakage currents and to maintain system stability, especially when using electrolytic capacitors.

Later, a 3LBC was controlled with a Model-Based Control (MBC) scheme [30] based on the flatness theory, which transforms a nonlinear system into a simpler parameterization. However, the flatness-based control method is not always achievable and can be computationally intensive.

A model predictive control (MPC) scheme was proposed [31], but it was only validated through simulations. This approach can potentially simplify the tuning of the control significantly. However, for more complex systems like the Multilevel Interleaved Boost Converter (MIBC), solving the complex optimization problem at each control step can be computationally demanding. Besides, a detailed model of the converter is required to achieve good performance with an MPC controller, as it is highly sensitive to system parameters [31]. Furthermore, with the presence of non linear components, the implementation can represent a real challenge. The literature presents also solutions based on the Takagi-Sugeno Fuzzy (TSF) approach, which has been extensively used in the past years [32], [33]. In addition, a voltage control method utilizing both PI and TSF was proposed in 2019 [34]. This approach aims to extend the stability of a normal controller region by managing the non-linearities of the model through a TSF approach.

Looking further at the complexity of a three-level interleaved converter, a significant effort should also be invested in the control of the current sharing of the differential inductors, to avoid undesired imbalance between the legs and avoid inductor saturation. Indeed, an ideal switching condition would make useless the implementation of an additional control scheme. However, the interleaving of modulation applied between the legs [35], added with nonlinearities of the circuits and unbalanced dead time may represent the failure of the converter [36], [37]. Several solutions to reduce the converter cost and complexity have been proposed in the literature. As example, [38] presents a sensorless current-sharing technique based on an estimation of the parasitic resistance, avoiding the sampling of each current and ensuring an adjusted duty cycle to each leg, while [39] describes a parameter-independent, sensorless current-sharing algorithm based on gradient estimation via low-frequency perturbation of duty cycles. This solution avoids using current sensors and, consequently, is suitable for digital controllers, avoiding also multiple ADCs. Unfortunately, the proposed algorithm is not feasible for high dynamic responses, as mentioned by the authors.

Several solutions have been proposed in the literature to reduce the converter cost and complexity. [40]. To maximize the noise immunity and reduce the sampling inaccuracy, the sampling point is synchronized with the PWM signal on the falling edge. Despite the simplicity of implementation, this kind of control is sensitive to the current ripple. Due to that, high transient dynamics can be impaired by a significant error in the current sampling.

Despite the wide range of existing solutions, configurations and modulation strategies proposed in the literature, most papers deal with new topologies while offering only high-level or partially implemented control strategies. For instance, some approaches, such as in [35], only introduce basic dual-loop control concepts without providing detailed insight into aspects like DC-link voltage balancing or coordinated current sharing. Others focus on sensorless methods [36] that, although reducing hardware complexity, increases the control complexity due to the presence of observers in the control scheme.

Therefore, the primary objective of this work is to propose a full-digital control scheme to a multilevel, interleaved GaN-based DC-DC converter operating at a switching frequency of 100 kHz. This article expands [41], where the preliminary results of the proposed control solution have been presented. The added value of this article consists of including the following:

- A complete analysis of the power converter structure is provided.
- Analytical and simulated Bode plot comparison and validation of the implemented control schemes.

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- Full experimental validation is provided, including voltage balancing control through the testing performed through a reduced-scale prototype.

II. DC-DC Converter Control

As depicted in Fig. 2, the proposed DC-DC converter architecture comprises two cascaded units, labeled as P and N. This cascaded configuration offers several advantages over the conventional H-bridge structure, primarily due to its enhanced efficiency. The increased efficiency can be attributed to the reduced stress on the passive components, leading to a lower power dissipation and consequently, improved thermal management. Moreover, the cascaded design results in a reduction in current harmonics stress for the inductors, allowing the reduction of the required filter inductance with direct consequence on the converter size. These benefits are particularly significant in high-power applications, where the ability to manage heat and minimize losses is crucial for reliable operation [42].

Each individual cell within the converter consists of two interleaved switching cells. These cells are connected through coupled inductors, denoted as L_{dm}, which are used to achieve better current distribution between the cells. Additionally, the converter uses input single inductors, L_{cm}, to ensure proper regulation of the input current. The utilization of coupled inductors plays a central role in the performance of the system, as it not only influences the sizing of the inductors and the converter itself, but also contributes to a significant reduction in current ripple. This reduction is particularly important in minimizing the switching losses, which are a common issue in high-frequency switching power supplies [43]. Furthermore, the use of coupled inductors helps in optimizing the overall system efficiency by mitigating the adverse effects of parasitic elements in the inductor windings [44].

The proposed digital DC-DC control scheme is presented in Fig. 3. Common-mode and differential mode controllers are implemented in a cascaded configuration with an outer voltage control loop. The presence of a voltage control loop balancing is mandatory due to the split DC-Link of the cascaded structure. Furthermore, an inner common mode and a differential mode current control loops are implemented.

Five control loops have been implemented to ensure optimal performance and stability:

- Two main control loops, specifically a voltage control loop and a current control loop. These external loops stabilize the output voltage and achieve the desired load current.
- Three supplementary control loops have been incorporated, each serving a distinct purpose in maintaining the overall balance of the system, i.e. two differential current balancing schemes and one differential voltage balance scheme. These schemes are crucial for regulating the voltage balancing of the capacitors and for ensuring proper current balancing in the system. Their main function is to prevent issues such as inductor saturation, which can significantly affect the converter's efficiency and operation.

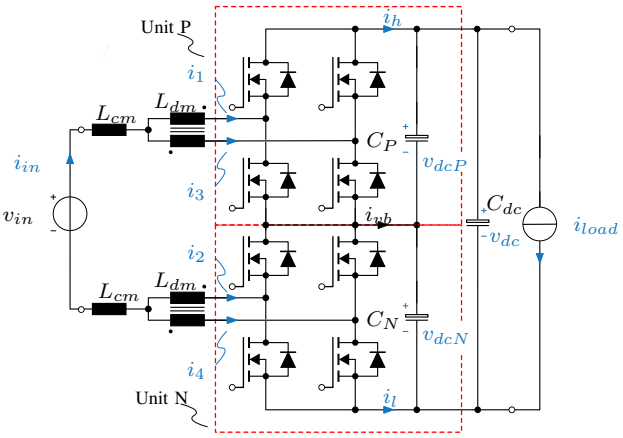


Fig. 2: Considered DC-DC converter structure.

With reference to Fig. 2 and Fig. 3:

- The output voltage control loop generates a current reference $i_{in}*$ for its internal current loop. The output of the current loop is a duty cycle d_i that is the same for all converter legs. Afterwards, the differential voltage balancing scheme adjusts this duty cycle d_i through an additive contribution d_{vb}. This correction action provides two duty cycles, d_{iP}, d_{iN}, which are applied to the two sections of the converter.
  Finally, the two duty cycles are adjusted with an additional current balancing loop by a quantity $d_{ib,P}$ and $d_{ib,N}$ respectively.
- The measured quantities are: currents flowing through the differential inductors (i_1, i_3, i_2, i_4), input voltage v_{in} the output capacitors voltages, v_{dcP}, and v_{dcN}. These voltage and current measurements are critical for the precise operation of the control loops and for ensuring that the system remains within its operating limits.

To evaluate the input current i_{in}, the sum of the currents in the differential inductors can be calculated as (1).

$$i_{in} = i_1 + i_3 = i_2 + i_4 \tag{1}$$

Furthermore, v_{dc} is estimated as the sum of the voltages v_{dcP} and v_{dcN}.

In order to evaluate the control parameters, the small signal model of the converter is obtained as in [45]. The small signal model is a linear approximation that is needed to analyze the behaviour of a system or circuit around an operating point, typically in the presence of small perturbations or deviations from the steady-state condition. This is particularly useful for studying the dynamic response of converters to variations in input or control signals. By linearizing the system's nonlinear equations, the small signal model simplifies the analysis of the system's stability, frequency response, and transient behaviour.

Based on the simplified models shown in Fig. 4, the

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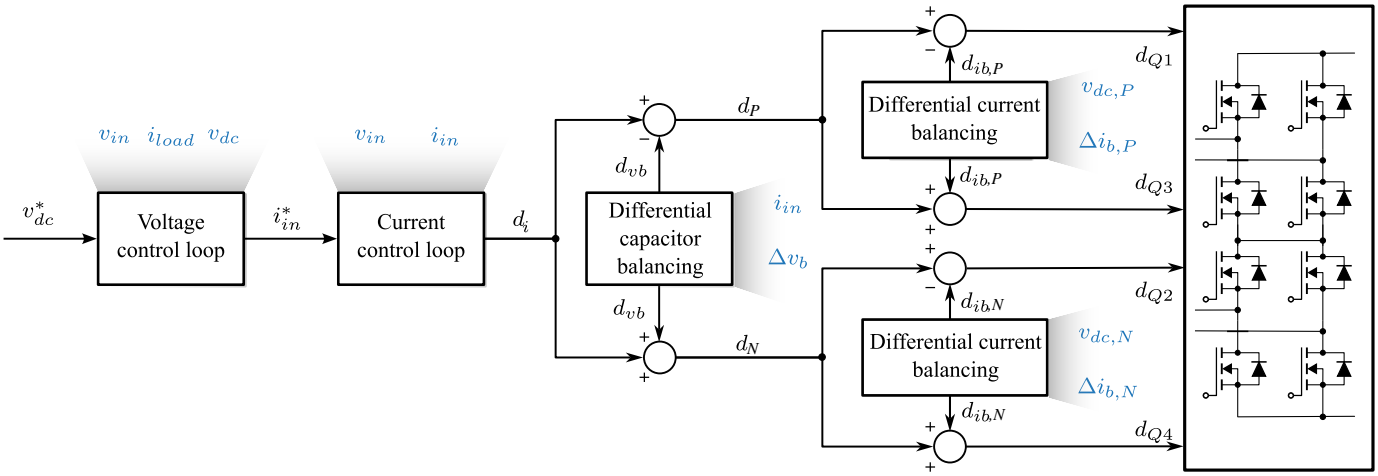


Fig. 3: Proposed DC-DC converter control loop.

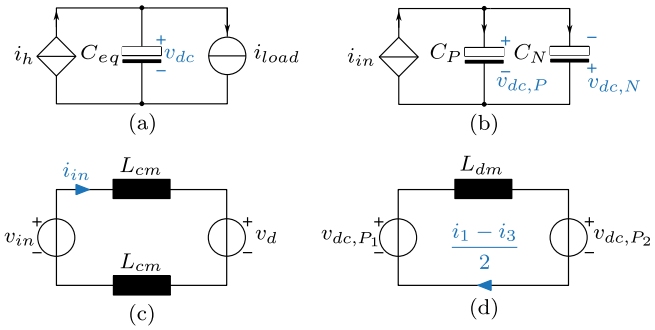


Fig. 4: Equivalent circuit representation of the system state-space equations: **(a)** Voltage loop, **(b)** Voltage capacitor balancing, **(c)** Current loop, **(d)** Differential inductor current balancing.

following state space equations are derived:

$$\begin{cases} 2L_{cm}\dfrac{di_{in}}{dt} = v_{in} - v_d \\ C_{eq}\dfrac{dv_{dc}}{dt} = i_h - i_{load} \\ C_P\dfrac{dv_{dc,P}}{dt} - C_N\dfrac{dv_{dc,N}}{dt} = i_{vb} \\ L_{dm}\dfrac{di_{ib}}{dt} = v_{dc,P1} - v_{dc,P2} \end{cases} \tag{2}$$

where C_{eq} is the equivalent capacitor at the converter output, v_d is the average voltage at the midpoint of a converter leg, i_h is the sampled high side current, the i_{vb} is the DC-Link midpoint current and i_{ib} is the differential current recirculating in high side and low side of the converter, as reported in (3).

$$\begin{cases} C_{eq} = \left(\dfrac{C_P C_N}{(C_P + C_N)} + C_{dc}\right) \\ v_d = d_i v_{dc} \\ i_{vb} = i_{in} 2 d_{vb} \\ i_{ib_{P,N}} = \dfrac{i_1 - i_3}{2} \end{cases} \tag{3}$$

A. Current control loop

The external current control, shown in Fig. 5, is implemented to achieve zero steady-state tracking error between the desired input current and the feedback one evaluated through (1).

The voltage to current plant transfer function is evaluated through the state space equations (2).

$$G_{p,i} = \frac{i_{in}(s)}{v_d(s)} = \frac{1}{s2L_{cm}} \tag{4}$$

Disturbance components are disregarded in the plant evaluation and compensated by a suitable feed-forward term in the control loop routine. Furthermore, the digital implementation of the control loop introduces delays that affects negatively the control scheme [46]. In particular, a first contribution is related to the digital processing and one due to the PWM modulator that introduced a zero-order hold (ZOH) effect over the sampling period. As a result, the delay transfer function is evaluated as:

$$G_{d,i} = e^{-sT_s}\frac{1 - e^{-sT_s}}{sT_s} \tag{5}$$

The current control is implemented with a simple Proportional-Integral (PI) current regulator whose transfer function is

$$G_{c,i}(s) = k_{P,i} + \frac{k_{I,i}}{s} \tag{6}$$

$k_{P,i}$ and $k_{I,i}$ are the proportional and integral gains.

The open loop transfer function can be written as:

$$G_{ol,i}(s) = G_{p,i}(s)G_{d,i}(s)G_{c,i}(s) \tag{7}$$

The PI regulator tuning is performed using the open-loop transfer function approach. A cross-over frequency $\omega_{c,i}$ is chosen and a 0 dB magnitude crossing is achieved. The integral coefficient k_i is chosen ten times smaller than k_p for stability reasons [47]. The parameters are consequently evaluated through (8):

$$\begin{cases} k_{P,i} \approx w_{c,i} 2L_{cm} \\ k_{I,i} = \dfrac{w_{c,i}}{10} k_{P,i} \end{cases} \tag{8}$$

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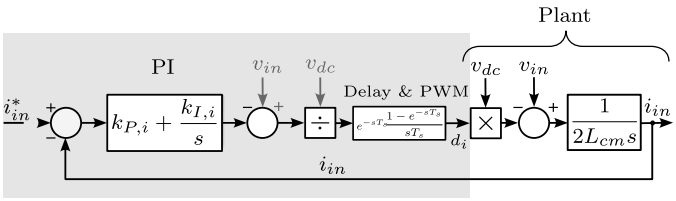


Fig. 5: Detailed block diagram of the main current control loop.

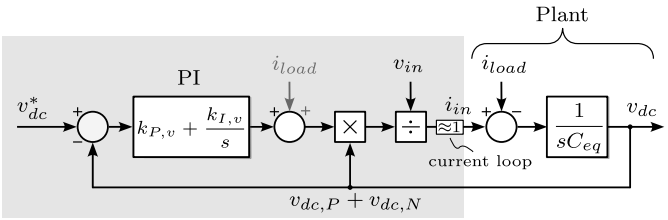


Fig. 7: Detailed block diagram of the main voltage control loop.

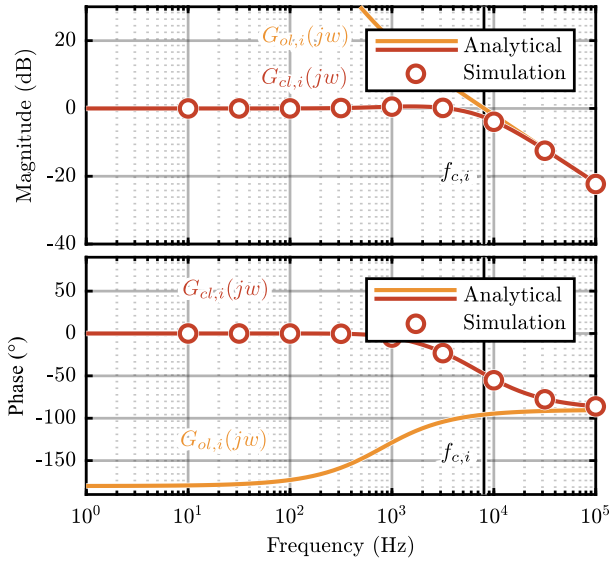


Fig. 6: Bode plots of the external current control loop. Open loop magnitude and phase (orange), closed loop magnitude and phase (red).

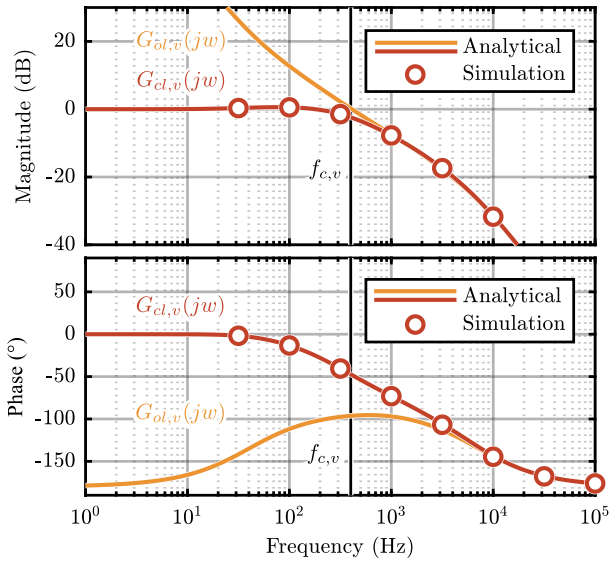


Fig. 8: Bode plots of the external voltage control loop. Open loop magnitude and phase (orange), closed loop magnitude and phase (red).

For the considered system, a crossover frequency of $f_{c,i} = 8kHz$ is chosen. Fig.6 presents the Bode plots extraction of the current loop control scheme. Both transfer functions of the open loop and closed loop control are presented.

B. Voltage control loop

The voltage control loop consist of a PI regulator, a feed-forward contribution, a gain-adjustment block and the plant transfer function. The block scheme is shown in Fig. 7.

As the DC-DC stage input power is known accurately, the load current i_{load} is estimated and fed forward in the control scheme. Indeed, the plant transfer function of the studied control loop routine can be evaluated through equation presented in (2) from the small signal model shown in Fig. 4(a) as:

$$G_{p,v} = \frac{v_{dc}(s)}{i_h(s)} = \frac{1}{sC_{eq}} \tag{9}$$

The controller transfer function is

$$G_{c,v}(s) = k_{P,v} + \frac{k_{I,v}}{s} \tag{10}$$

where $k_{P,v}$ and $k_{I,v}$ are the proportional and integral gains of the regulator.

Since the current inner loop has a much faster dynamics, in this analysis it can be considered as ideal (i.e. unitary gain block). As a result, the transfer function of the system become:

$$G_{ol,v}(s) = G_{p,v}(s)G_{c,v}(s) \tag{11}$$

The PI controller tuning is performed as described in the previous section:

$$\begin{cases} k_{P,v} \approx w_{c,v}C_{eq} \\ k_{I,v} = \dfrac{w_{c,v}}{10}K_{P,v} \end{cases} \tag{12}$$

Fig.8 presents the Bode plots extraction of the voltage loop control scheme. A crossover frequency of $f_{c,v} = 400Hz$ is chosen.

C. Voltage capacitor balancing

Multilevel converters are characterized by a split DC-Link. Due to the known variability of capacitance values related to specific working conditions [48], an additional voltage balancing control loop is implemented in order to balance capacitors in the upper and lower side. This control scheme is achieved by performing a zero steady-state differential voltage

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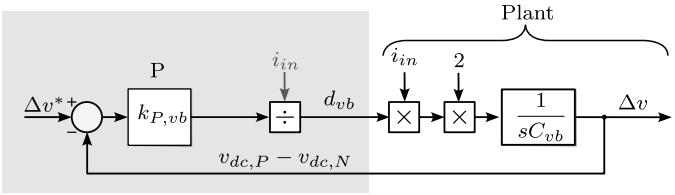


Fig. 9: Detailed block diagram of the voltage balancing control loop.

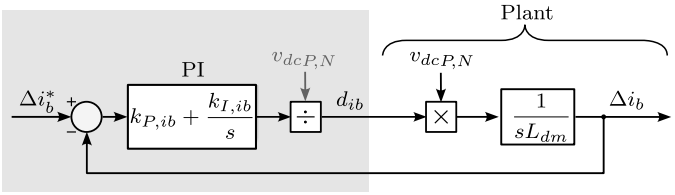


Fig. 11: Detailed block diagram of the current balancing control loop.

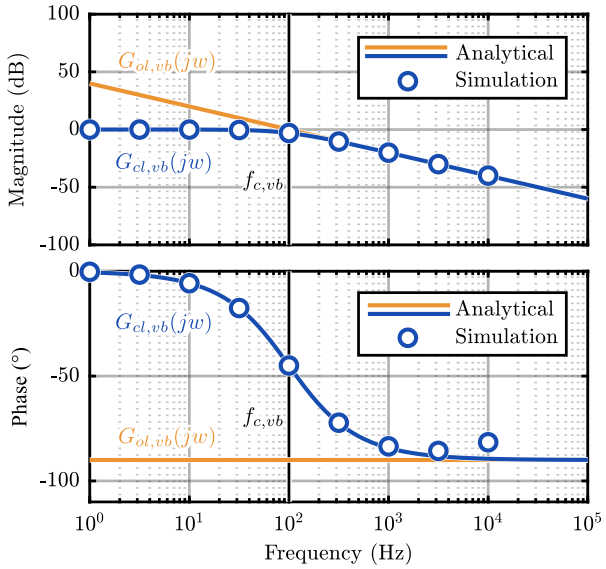


Fig. 10: Bode plots of the internal voltage balance control loop. Open loop magnitude and phase (orange), closed loop magnitude and phase (blue).

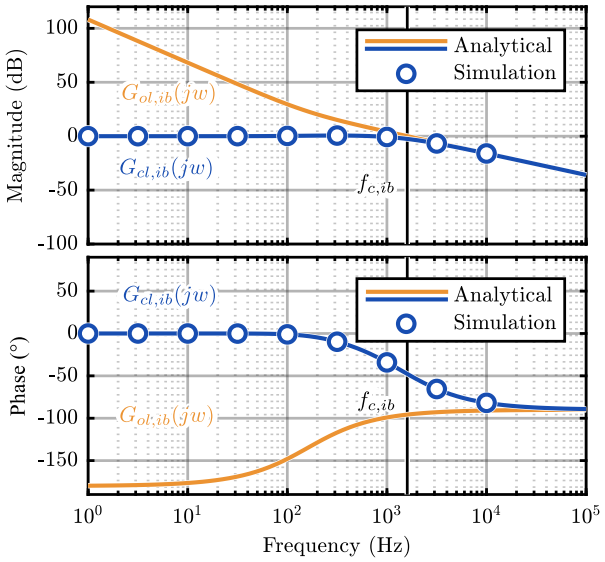


Fig. 12: Bode plots of the internal current balance control loop. Open loop magnitude and phase (orange), closed loop magnitude and phase (blue).

balance, presented in Fig. 9. A proportional stage regulator is evaluated from (2) as:

$$k_{P,vb} = w_{c,vb} C_{vb} \tag{13}$$

where

$$C_{vb} = \frac{C_P + C_N}{2} \tag{14}$$

Later on, the evaluated duty contribution is respectively added and subtracted to the upper and lower sides as an additive contribution to the current control output, as shown in Fig. 3. In order to avoid interference between control bandwidth, a crossover frequency of $f_{c,vb} = 100Hz$ is selected.

D. Differential current balancing

Current unbalance between parallel legs in power converters with interleaving can lead to significant problems [49]: different thermal stress over components, undesired phase voltage difference and increased losses due to an unbalanced load seen by discrete devices, leading to uneven thermal stress among the devices.

Consequently, two equal control loops are implemented to avoid this imbalance between parallel legs on the upper and lower sides of the converter. Fig. 11 presents the block scheme of the control loop.

A PI-regulated control is implemented, and the parameters are tuned according to the small signal model presented in Fig. 4 and the equations (2):

$$\begin{cases} k_{P,ib} \approx w_{c,ib} L_{dm} \\ k_{I,ib} = \dfrac{w_{c,ib}}{10} k_{P,ib} \end{cases} \tag{15}$$

Fig. 12 presents the Bode plots of the presented control loop routine, with a cutoff frequency of $f_{c,ib} = 1.7kHz$.

Table I summarizes the chosen parameters for the implemented control scheme. Regarding Fig. 2, the currents i_{in}, i_h, i_l represent the currents entering the external control loop: the differential one, circulating in the high side and the one in the low side of the converter.

III. Control Implementation

The design of the PI controller has been performed in the continuous-time domain using Bode plots. The actual digital implementation on the microcontroller adopts a discrete-time structure based on the backward Euler method for the integral term. As the system operates at a high sampling frequency, with a sampling rate of 200 kHz, the approximation between the continuous-time design and the discrete-time implementation remains highly accurate.

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TABLE I: Loop control parameters

	External current control	External voltage control	Internal Current control differential mode	internal voltage control balancing control
f_c	$8\ kHz$	$400\ Hz$	$1.7\ kHz$	$100\ Hz$
w_c	$2\pi f_{c,i}$	$2\pi f_{c,v}$	$2\pi f_{c,ib}$	$2\pi f_{c,vb}$
k_P	$2L_{cm}w_{c,i}$	$w_{c,v}\left(\frac{C_P C_N}{(C_P+C_N)}+C_{dc}\right)$	$L_{dm}w_{c,ib}$	$C_{Dc}w_{c,vb}$
k_I	$\frac{w_{c,i}k_{P,i}}{10}$	$\frac{w_{c,i}k_{P,v}}{10}$	$\frac{w_{c,ib}k_{P,ib}}{10}$	$None$

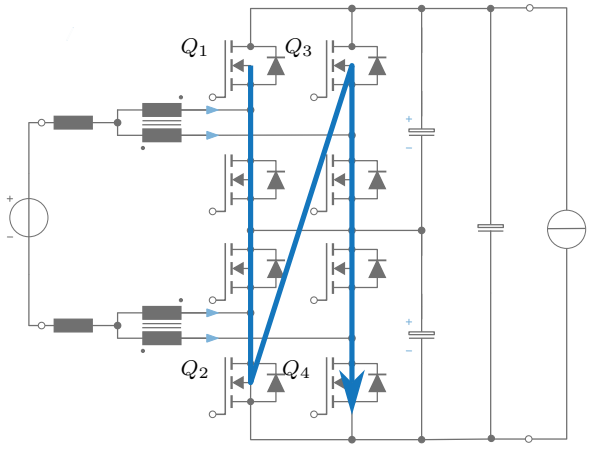


Fig. 13: N-type switch order modulation.

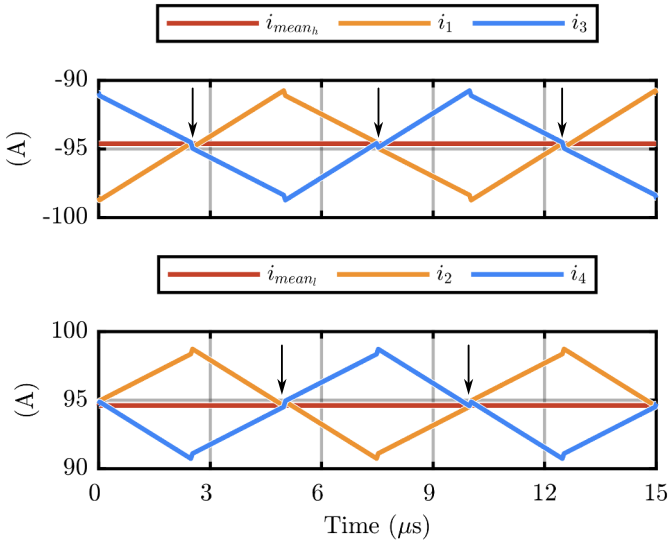


Fig. 14: Current sampling detail for the differential currents of the high side and low side of the converter.

Regarding the modulation strategy, an interleaving with 90° degrees of phase-shift is adopted for the four DC-DC converter legs. Two modulation types can be defined depending on the switching order [21]. For this study, an N-type modulation is implemented as it results in a better efficiency of the converter, an increased capacitor life, and a reduced EMI noise [14].

Fig. 13 a presents the switching order of the transistor legs over a switching period. As a consequence, the current sampling instant should be different for each current.

Fig. 14 highlights the importance of correctly sampling of the currents for each leg. As each leg refers to a different PWM, phase-shifted between each other of 90° The arrows indicate the correct sampling instant to evaluate the currents i_1, i_2, i_3, i_4.

The four duty cycles presented in Fig. 15 are compared with four different carriers (amplitude equal to unity) that are phase-shifted between each other of 90° to generate the switching functions of the power switches, shown in Fig. 17. The trigger of the acquisition is synchronized with the triangular carriers, and each physical quantity is related to a specific carrier. Furthermore, the update of the compare register of the PWM modulator must be done in a specific instant, different for each switching pole. A good solution for synchronizing all needed processes is to define a primary timer n_{main}, whose timer period is set according to the desired switching frequency. In addition, sampling instants must be synchronized with the PWM carrier peaks, as shown in Fig. 17. To compensate

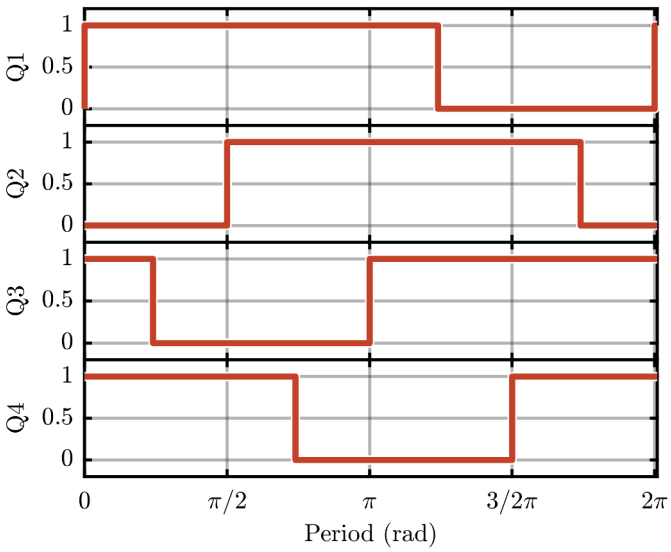


Fig. 15: Switching functions for four phase-shifted legs (90° apart) over one switching period.

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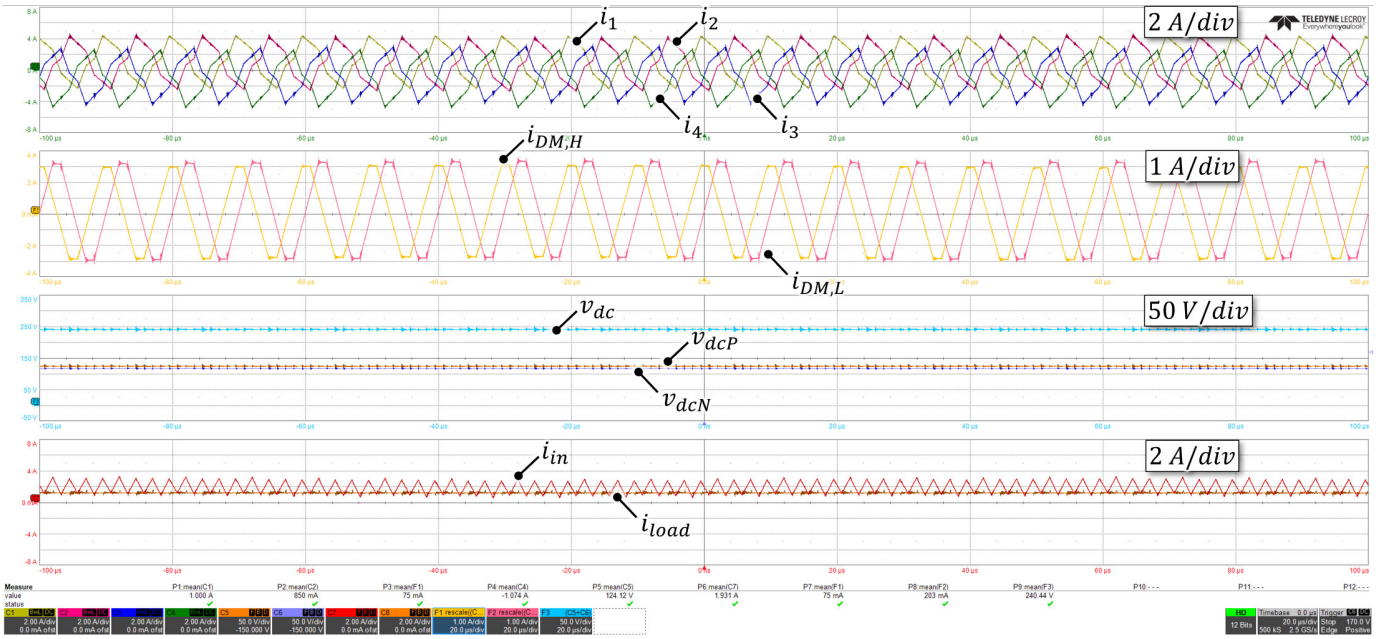


Fig. 16: Converter's waveform under steady-state operation with 150V input, 250V output, d=0.6 and 1.5A load current. (a): input currents of each half bridge leg i_1, i_2, i_3, i_4. (b): differential currents of the upper $i_{DM,H}$ and bottom $i_{DM,L}$ coupled capacitor respectively. (c): voltage across the two mid-point connected capacitors v_{dcP} and v_{dcN} and the rail-to-rail DC-link voltage v_{dc}. (d): converter input current i_{in} and load current i_{load} provided by the electronic load.

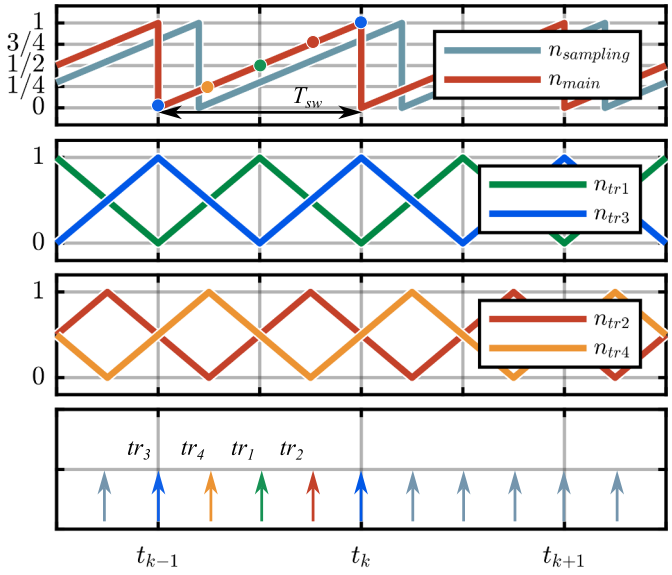


Fig. 17: Top: Main counter and shifted counter. Middle: Carrier phase-shifted of 90°. Bottom: Triggers used for synchronization of the triangular carriers at specific percentage of the main counter content.

the delay introduced by the analog sensors and the analog conditioning circuitry, a new counter $n_{sampling}$ is employed with a specific lag. Triggers for A/D converters are determined by specific $n_{sampling}$ values, allowing for two samples per feedback quantity per PWM period. Moreover, the Interrupt Service Routine (ISR) for DC-DC control must synchronize with the PWM period, requiring termination before a new ISR to ensure the availability of the latest sampled data at T_{sw}.

IV. Experimental Results

The transient and steady-state performance of the proposed control strategy are verified experimentally on a reduced-scale prototype that is shown in Fig.18. The operating conditions and the converter nominal specifications are reported in Table II. The converter's power unit consists of four GaN-based half bridge boards that are properly connected to build the multilevel DC/DC topology, as in Fig. 2. The input voltage is provided by a bidirectional power source and the load current is supplied by an electronic load. The control is implemented in a rapid prototyping platform (RT Box 2 from PLEXIM), using a sampling frequency of 200 kHz and a control frequency of 100 kHz, according to Fig. 14. Complementary switches are driven with a deadtime of 75 ns, which is sufficient to prevent shoot-through without introducing significant distortions and additional losses due to the reverse conduction. Given the DC-DC nature of the converter, any minor distortion caused by deadtime is effectively compensated by the control loop routine, eliminating the need for dedicated deadtime compensation logic.

The main waveforms regarding the converter steady-state operation with 150V input voltage, 250V output voltage and 1.5A of load current are shown in Fig. 16. As the operating duty cycle is different from 0.5 (i.e. 0.6), the current ripples of current i_1,i_2,i_3,i_4 shows a typical segmented piece-wise linear variations that is typical to the multilevel structure. The only exception to this operation is when the duty cycle is equal to 0.5, when the current ripple exhibits a triangular waveform that is shown in Fig.14.

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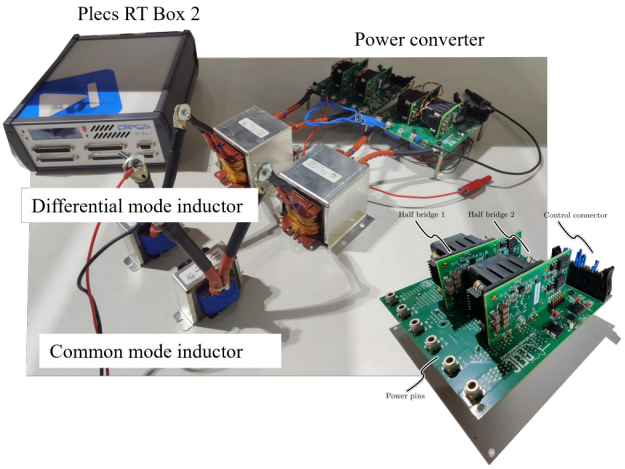


Fig. 18: Experimental setup.

TABLE II: DC/DC CONVERTER SPECIFICATIONS AND NOMINAL OPERATING CONDITIONS.

Parameter	Description	Value
P_o	Output power	2kW
V_{in}	Input Voltage	150V
V_{dc}	DC-link voltage	250V-350V
$I_{load,rated}$	Nominal output current	8A
f_{sw}	Switching frequency	100kHz
C_P, C_N	Mid-point connected capacitance	22.6μF
C_{dc}	External DC-Link Capacitance	340μF
L_{dm}	DM coupled inductance	88μH
L_{cm}	CM inductance	5.6μH
f_{ISR}	Control frequency	100kHz
f_s	Sampling frequency	200kHz

The achieved results demonstrate that the proposed control ensures a stable steady-state operation, guaranteeing a satisfactory voltage balance among the mid-point connected capacitors and a null mean value of the differential mode current, which would saturate the coupled inductors.

To verify the proposed control effectiveness under dynamic conditions, a load current change from 10% to 50% of the nominal output current is imposed in 10 ms. The experimental results for DC-link voltages of 250 V and 350 V are reported in Fig. 20. Also in this case, the control loops are stable proving the required current to the load while controlling the DC-link voltage and ensuring the C_{dcP} and C_{dcN} voltages balancing. Furthermore, the differential currents are highlighted in both cases, showing an accurate balance of the differential currents.

Fig. 19 provides the voltage balancing control loop effect considering the converter operating at 150V input, 350V output and 4A load current. Initially, the voltage balancing loop is disabled and the voltages across C_{dcP} and C_{dcN} are unbalanced even though the output current is only the 50% of the nominal one. Corresponding to time zero, the balancing loop is enabled and consequently the balancing action is performed with a transient response within 1 ms. It is worth to underline that there is a small difference at steady-state after the balance because the voltage balancing control loop consists only of a proportional part.

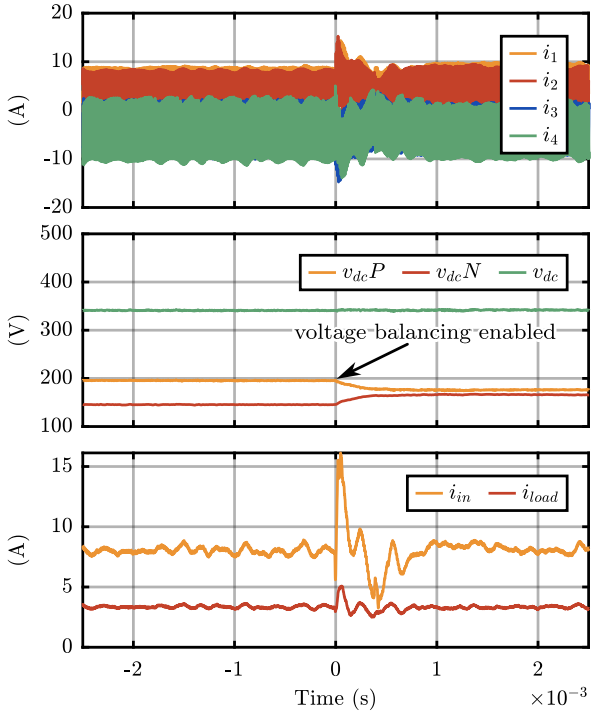


Fig. 19: Experimental results of the capacitor balancing at 150V input, 350V output and 4A load current.

V. CONCLUSIONS

This paper proposes a full digital control of a complex multilevel GaN DC-DC converter, explaining and validating the control scheme under different working conditions.

The experimental results confirm the viability of the proposed control scheme in achieving the desired voltage and current regulation, while also maintaining balanced capacitor voltages and avoiding inductor saturation. Moreover, the digital control approach outlined in this study addresses the challenges associated with high switching frequencies and the synchronization of multiple interleaved switching cells. The proposed methodology offers a robust solution for controlling complex power converter systems.

The contributions of this research highlight the potential of advanced digital control techniques and GaN technology in pushing the boundaries of control dynamics for future fuel cell-powered electric vehicles. Further investigations will explore the scalability of the proposed system and its application to other high-power conversion scenarios.

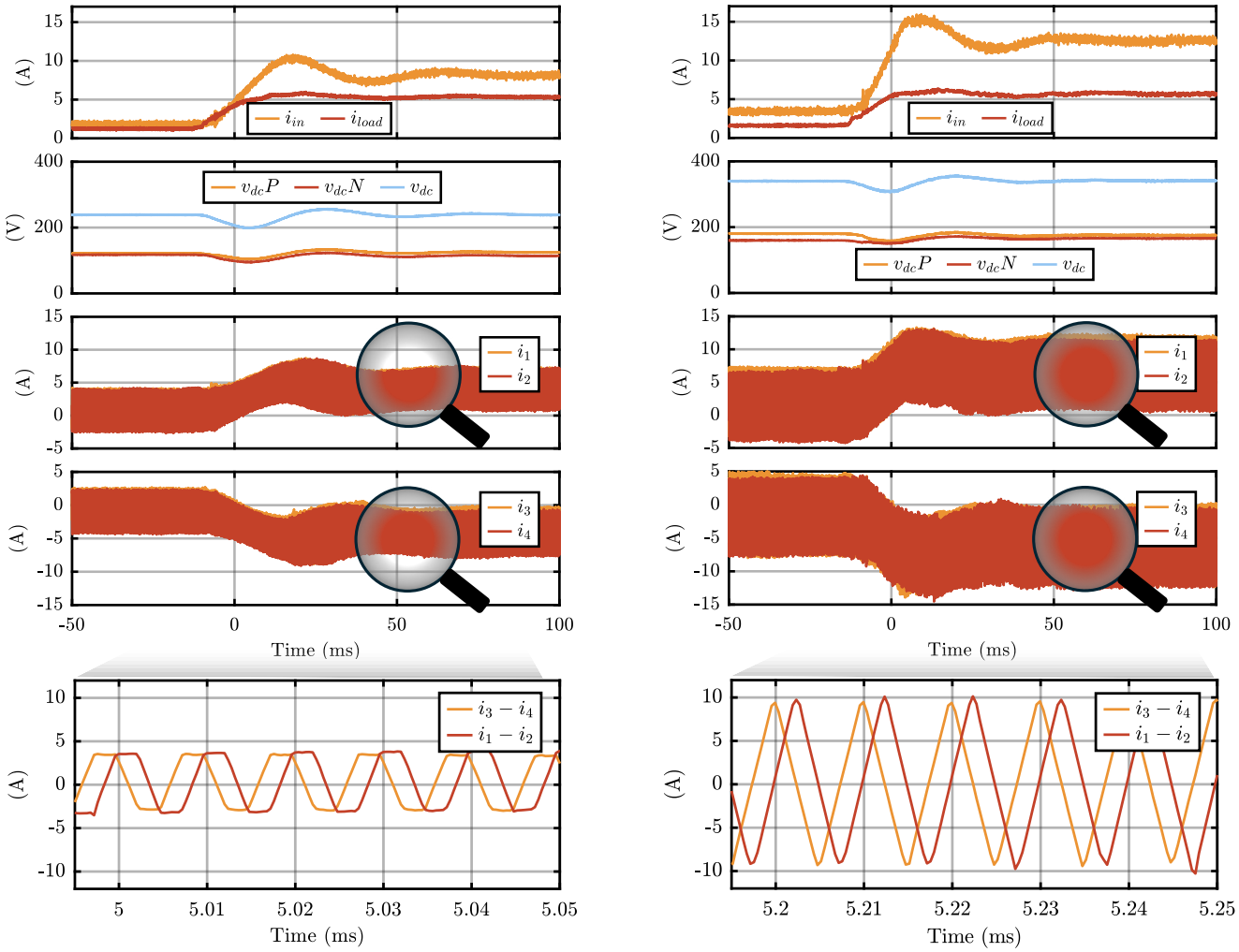
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(a) (b)

Fig. 20: Experimental test of a load current ramp response from 10% to 50% of the nominal output current at 150V input and under different DC-link conditions: (a) 250V, (b) 350V.

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Stefano Savio (Graduate Student Member, IEEE) received the B.Sc. in mechanical engineering and the M.Sc. degree in mechatronics engineering from the Politecnico di Torino, Turin, Italy, in 2020 and 2022 respectively. In 2022, he joined the Power Electronics Innovation Center, Politecnico di Torino, as a PhD student, where he is currently working on power electronics converter control and design. His main research interests include DCDC converters, high-power DC/DC converters, WBG devices, FEA simulations and parasitics analysis.



Simone Giuffrida (Graduate Student Member IEEE) received the B.Sc. and M.Sc. degree in electrical engineering from the Politecnico di Torino, Turin, Italy, in 2020 and 2022 respectively. In 2022, he joined the Power Electronics Innovation Center, Politecnico di Torino, as a Ph.D. student, where he is currently working on power electronics converter design for traction applications using WBG devices. In 2024, he was a Visiting Researcher with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland. His main research interests include traction inverters, high-power AC/DC and DC/DC converters, WBG devices, and high-frequency magnetics.



Fabio Mandrile (Member, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering in 2017 and 2021, respectively, from Politecnico di Torino, Torino, Italy. His research interests include virtual synchronous generators, power electronics for grid-connected applications, and the experimental characterization of converters and motor drives.



Fausto Stella (Member, IEEE) received the bachelor's and master's degrees in electrical engineering and the Ph.D. degree from the Politecnico di Torino, Turin, Italy, in 2012, 2015, and 2019, respectively. In 2017, he was a Visiting Ph.D. student with the University of Nottingham, Nottingham, U.K. He is currently an Assistant Professor with the Politecnico di Torino. His research interests include the design of power electronic converters, focusing on SiC semiconductors and reliability issues, and the control of converters via embedded systems. He is also a Research Fellow with Politecnico di Torino.



Eric Giacomo Armando (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering from Politecnico di Torino, Turin, Italy, in 2002 and 2008, respectively. He is currently a Full Professor of power converters, electrical machines, and drives with Politecnico di Torino . He is the co-author of numerous Journal Papers and three Patents. His research interests include power electronics and high performance AC motor drives. He was the recipient of three awards for innovation, one paper award from the Power Electronics Technical Committee of the IEEE Industrial Electronics Society, and one paper award from the Industrial Drives Committee of the IEEE Industry Applications Society.



Radu Bojoi (Fellow, IEEE) received theM.Sc. degree in electrical engineering from the Technical University of Iasi, Iasi, Romania, in 1993, and the Ph.D. degree in electrical engineering from Politecnico di Torino, Torino, Italy, in 2002. He is a Full Professor of power electronics and electrical drives with the Energy Department G. Ferraris and the Chairman of the Power Electronics Innovation Center with Politecnico di Torino. He has authored and coauthored more than 200 papers covering electrical drives and power electronics for industrial applications, transportation electrification, power quality, and home appliances. He was involved in many research projects with industry for direct technology transfer aiming at obtaining new products. Dr. Bojoi was the co-recipient of 7 IEEE prize paper awards.

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