Design of a Hybrid High Resolution Digital PWM for a Smart Power Point-of-Load Power Converter

Design of a Hybrid High Resolution Digital PWM for a Smart Power Point-of-Load Power Converter

Neha Dalal*, Matteo Landini†, Paolo Vilmercati†, Francesco Musolino* and Paolo Stefano Crovetti*
Email:{neha.dalal,francesco.musolino,paolo.crovetti}@polito.it, {matteo.landini, paolo.vilmercati}@st.com
*Department of Electronics and Telecommunication, Politecnico di Torino, Torino, Italy
†APMS Smart Power R&D, STMicroelectronics, Cornaredo, Italy

***Abstract*—The article presents the design and the architectural optimization of a new Hybrid, High-Resolution Digital Pulse Width Modulator (HHR-DPWM) and its implementation in an integrated, digitally-controlled, voltage-mode, point-of-load (POL) buck converter for automotive applications. The proposed HHR-DPWM architecture, which features a synchronous counter-based DPWM, a delay locked loop (DLL)-based digital-to-time converter (DTC) with sub-clock-cycle resolution, and Dyadic Digital Pulse Modulation (DDPM) dithering, is optimized to meet the requirements of the POL converter at low cost and design effort. The POL converter with the proposed HHR-DPWM is fabricated in the 110 nm BCD9s technology by STMicroelectronics. Based on measurements, the converter regulates the output voltage with 2 mV accuracy, 2 mV peak to peak ripple and a power efficiency up to 95.4% at 3.4 V output voltage.**

***Index Terms*—Delay locked loop (DLL), dyadic digital pulsewidth modulation (DDPWM), limit-cycle-oscillations (LCOs), dithering.**

I. Introduction

Digitally-controlled switching-mode power converters are more and more becoming a compelling choice over the last years as they offer higher flexibility, lower cost and quicker design time compared to converters based on analog control [1]–[4]. Despite such undeniable merits, the operation of digitally-controlled converters can be severely impaired by low frequency limit-cycle-oscillations (LCOs), which arise whenever the digital pulse-width modulator (DPWM) resolution is coarser than the analog-to-digital converter (ADC) resolution, thus limiting in practice the dc accuracy of digitally-controlled converters based on standard counter-based DPWM, especially when operated at high switching frequency [5].

In this context, several techniques have been proposed to enhance the DPWM resolution and attain LCOs-free operation in digitally-controlled power converters [6]–[9]. In [10]–[12], delay-line-based time-to-digital converter is introduced in a counter-based DPWMs to achieve sub-clock cycle resolution, at the cost of increased complexity, area and sensitivity to process, voltage and temperature (PVT) variations [13]. Digital dithering techniques are adopted to increase resolution by varying the duty cycle within specific dithering patterns obtained by thermometric, sigma-delta [14]–[16], dyadic [17] [18]. Though dithering is inexpensive, it can possibly generate sub-harmonic ripple components in the output voltage.

Aiming to address the limitation of previously proposed solutions, this work presents a novel Hybrid High Resolution DPWM (HHR-DPWM) which entails a standard counter-based DPWM, a delay locked loop (DLL)-based TDC and a dyadic digital pulse modulation (DDPM)-based dithering to optimally increase the DPWM effective resolution at the minimal design complexity.

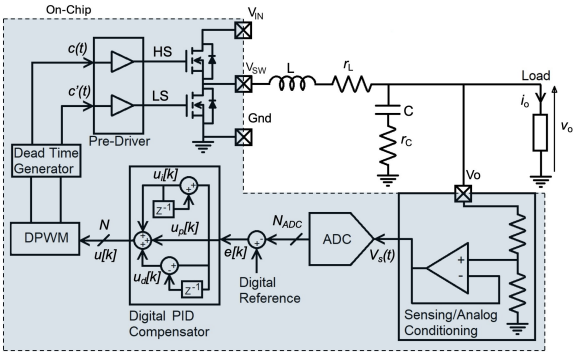

Fig. 1: Digitally controlled POL DC-DC Buck Converter

The proposed design is adopted in point-of-load (POL) power converter targeting automotive applications, designed and fabricated in 110nm BCD9s technology. Experimental validation supports the claim of enhanced resolution of DPWM at low cost and without impairing output ripple and dynamic performance.

The rest of the article is organized as follows: Sect. II revises the architecture of digitally controlled power converter emphasing the requirement of high resolution DPWM. In Sect. III, the HHR-DPWM architecture is thoroughly presented and its optimal design is discussed. Further, Sect. IV includes the experimental setup and results along with performance comparison with other state-of-the-art digital buck converters. Some concluding remarks are finally drawn in Sect. V.

II. Digitally Controlled Buck Converter Architecture

In this work, a HHR-DPWM targeting the requirements of a digitally-controlled POL synchronous DC-DC Buck converter for automotive applications, intended to convert the 5 V $\pm 10\%$ voltage provided by a first-stage regulator from the battery voltage, and converting it into a wide range of configurable regulated voltages from 0.8 V to 3.4 V with mV-range accuracy, as needed to supply on-vehicle electronic control units (ECUs) with currents in the 0.5 A - 2.5 A range.

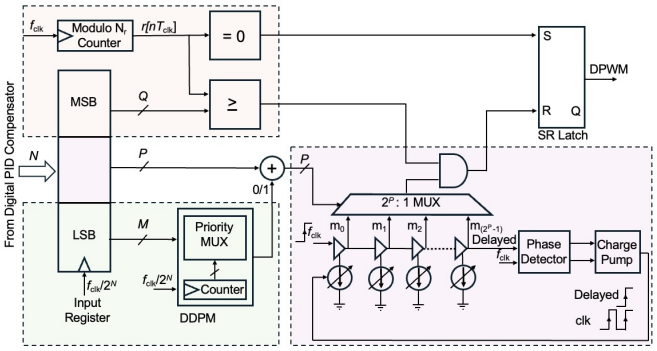

Fig. 2: HHR-DPWM Architecture

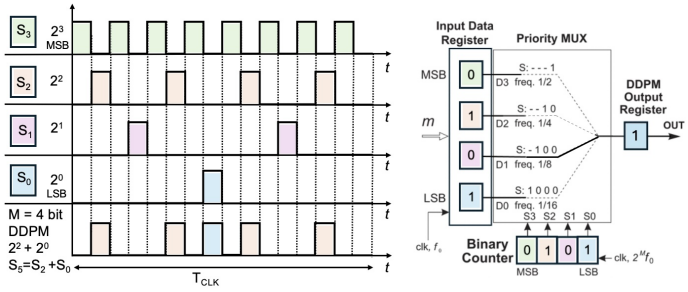

Fig. 3: DDPM pattern and hardware implementation [17]

The converter, whose block diagram is shown in Fig. 1, operates at a switching frequency $f_\mathrm{s} = 1/T_\mathrm{s} = 2\,\mathrm{MHz}$. Its output voltage, v_o is scaled by a factor $H = 9/10$ by a voltage divider, resulting in the conditioned voltage $v_\mathrm{s} = H \cdot v_\mathrm{o}(t)$, and then sampled at f_s ($v_\mathrm{s}[k] = v_\mathrm{o}(kT_\mathrm{s})$) and quantized by the ADC with a resolution $q_v^{(\mathrm{ADC})} = V_\mathrm{FS}/(H \cdot 2^{N_\mathrm{ADC}})$, where V_FS =1.8V and $N_\mathrm{ADC} = 10$ is number of bits of ADC.

The digital error signal, $e[k] = V_\mathrm{ref} - v_\mathrm{s}[k]$ is generated as the difference of the digital reference V_ref and the ADC output code, and is fed into a digital proportional-integral-derivative (PID) compensator. The command signal, $u[k]$ generated by PID is subsequently processed by HHR-DPWM, operating at a clock frequency $f_\mathrm{CLK} = 1/T_\mathrm{CLK} = 40\,\mathrm{MHz}$ which generates the DPWM signals to operate the power devices.

Based on [5], for LCO-free operation, the ADC bin size should be larger than the DPWM output voltage resolution, $q_\mathrm{v}^{(\mathrm{DPWM})} = V_\mathrm{IN}/2^N$ to have at least one of the quantized DC output voltages fall into zero-error bin, mathematically

$$q_\mathrm{v}^{(\mathrm{ADC})} > q_\mathrm{v}^{(\mathrm{DPWM})} \tag{1}$$

resulting in the requirement for the DPWM resolution N

$$N > \log_2\left[H\frac{V_\mathrm{IN}}{V_\mathrm{FS}}2^{N_\mathrm{ADC}}\right]. \tag{2}$$

In the proposed POL converter, based on Eqn.(2), a DPWM resolution N exceeding 11.58 bits is required for LCO-free operation. For a switching frequency of f_s= 2 MHz such a resolution would require an impractically high clock frequency of over 6 GHz in a plain counter-based DPWM, thus motivating the necessity of an alternative implementation.

III. Proposed HHR-DPWM

The proposed HHR-DPWM is shown in Fig. 2. Here, the N-bit high-resolution command word $u[k]$ from the PID compensator is split into three sub-words of Q, P and M bits, respectively, which are forwarded to a standard counter-based DPWM, to a Delay-Locked-Loop (DLL)-based digital-to-time converter (DTC) and to a DDPM modulator, respectively, which synergistically contribute to the overal DPWM resolution as discussed in what follows.

A. Architecture of HHR-DPWM

In the counter-based DPWM in Fig. 2, a DPWM signal with a frequency f_s and a duty cycle coarsely quantized over $N_\mathrm{r} = f_\mathrm{clk}/f_\mathrm{s}$ levels is generated by a SR-latch, which is set when the content of a free-running modulo-N_r counter operated at the system clock frequency f_clk is equal to zero, and is reset when the counter content matches the first Q most significant bits (MSBs) of the command word, as illustrated in Fig.5.

To increase the DPWM resolution, the delay of the SR-latch reset rising edge from the beginning of the system clock period, which defines the timing of the DPWM falling edge, is fine-tuned with a sub-clock cycle resolution by a DLL-based DTC depending on the intermediate P bits of the command word. The DLL, which is shown in Fig.2, is made up of 2^P identical, current-controlled delay elements, whose total delay is enforced to match the system clock period T_clk by a negative feedback loop, thus resulting in a single cell delay $\Delta t_{DLL} = T_\mathrm{clk}/2^P$. Once the system clock signal is applied at the input of the DLL, a $2^P : 1$ multiplexer (MUX) is used to select one of the 2^P uniformly spaced, delayed versions $m_0 \ldots m_{2^P-1}$ of the clock signal available at each tap of the delay line based on the P intermediate bits of the command word, so that to effectively tune the falling edge of the DPWM signal with a Δt_{DLL} resolution.

Even if a time resolutions as small as the minimum propagation delay of a digital gate can be achieved with a DLL-based DTC, the complexity of the DLL increases exponentially with the number of bits P, resulting in a significant area and power penalty. To enhance the DPWM resolution at lower cost, DDPM-based dithering [17], [18] is integrated on top of the proposed HRR-DPWM architecture. In detail, the last M LSBs of the command word are processed by a DDPM modulator, whose hardware implementation is straightforward (see detail in Fig.3) to increase the DPWM pulse width by Δt_{DLL} in m periods over 2^M periods of a DDPM pattern, as illustrated in Fig.5 [19], and hence to get an averaged duty cycle over the 2^M periods of a DDPM pattern with sub-LSB resolution and with the lowest possible ripple, thanks to the favorable spectral characteristics of the DDPM modulation [17].

Nevertheless the spectral components resulting in switching frequencies sub-harmonic tones inside the pass-band of output filter, which cannot be filtered, imparts critical contribution in output voltage ripple. Thus dithering is easy to implement

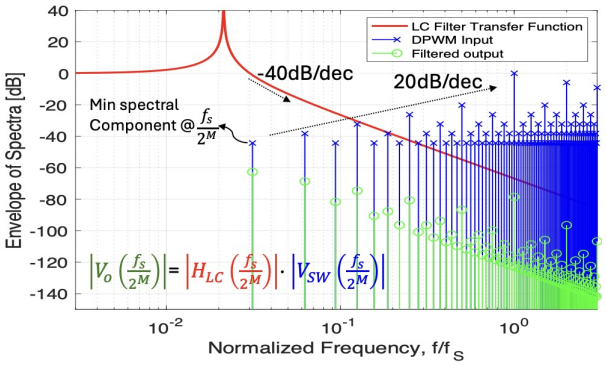

Fig. 4: Envelope Dyadic PWM Spectra.

but there is trade-off between regulation performances and frequency behavior.

B. HHR-DPWM Architecture Optimization

The proposed HHR-DPWM is designed to attain the target $N > 11.58$ bit resolution required for the POL buck converter described in Sect.II at minimum hardware complexity and without output ripple degradation.

For this purpose, the maximum possible number of DPWM quantization levels compatible with the system clock frequency $f_{\rm clk} = 40\,\text{MHz}$ and the switching frequency $f_{\rm s} = 2\,\text{MHz}$, i.e. $N_{\rm r} = f_{\rm clk}/f_{\rm s} = 20$ are obtained from the counter-based DPWM, which is directly driven with the $Q = \lceil \log_2 N_{\rm r} \rceil = 5$ most significant bits of the command word.

Then, to reduce the DLL hardware complexity, the DDPM dithering block is designed to provide the maximum resolution enhancement (i.e., with the largest possible M) without resulting in output ripple degradation. From the envelope of the spectra of Dyadic DPWM signals reported in [19] and shown in Fig.4, the DDPM dithering-induced output ripple is dominated by the dithering spectral component at the lowest sub-harmonic frequency $f_{\rm s}/2^M$, which is scarcely attenuated by the LC filter of the power converter. In view of that, the maximum number of DDPM dithering bits M is derived imposing that the amplitude of the lowest sub-harmonic component after LC-filtering is less than the target output voltage accuracy of the converter, i.e. $0.5\,q_{\rm v}^{(\rm ADC)}$. Since, based on [19], the amplitude of the sub-harmonic at $f_{\rm s}/2^M$ before filtering is $V_{\rm in}/2^{N-M}$, the above condition to avoid output ripple degradation reads:

$$H\frac{V_{\rm in}}{2^{N-M}} \cdot \left| H_{\rm LC}\left(\frac{f_{\rm s}}{2^M}\right)\right| \leq \frac{V_{\rm FS}}{2^{N_{\rm ADC}+1}} \tag{3}$$

where $|H_{\rm LC}(f_{\rm s}/2^M)|$ is the magnitude of the LC filter response at $f_s/2^M$, that gives:

$$M \leq \frac{1}{3}\left[\log_2\left(\frac{f_{\rm s}^2 \cdot V_{\rm FS}}{f_{\rm c}^2 \cdot H \cdot V_{\rm in}}\right) + N - N_{\rm ADC} - 1\right] \tag{4}$$

where $f_{\rm c} = 1/(2\pi\sqrt{LC}) = 12\,\text{kHz}$ for the POL converter considered in Sect. II. From Eqn.(4) the maximum number of DDPM dithering bits is 4.58 bits, so a DDPM dithering resolution $M = 4$ is fixed to avoid output ripple degradation.

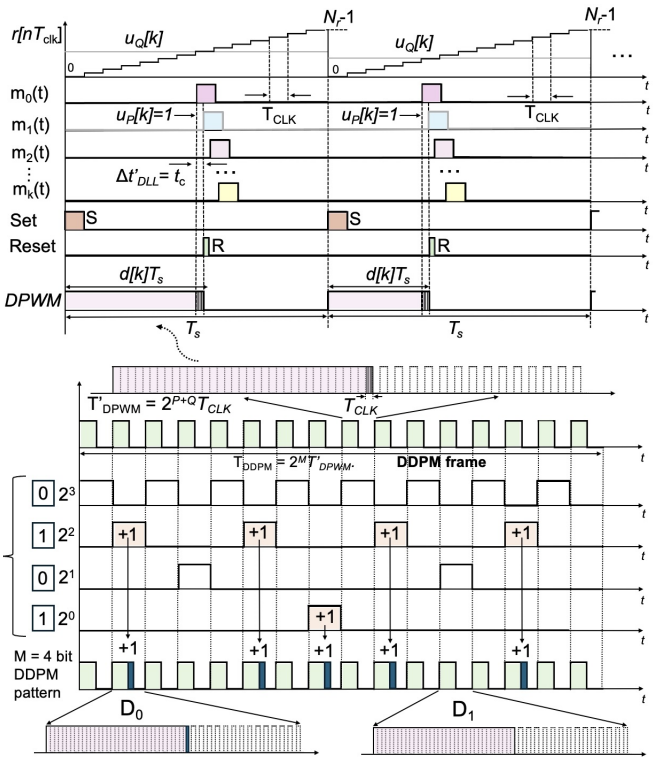

Fig. 5: Waveform of Counter-based + DLL + Dyadic Dithering

Once the number of levels of the counter-based DPWM ($N_{\rm r} = 20$) and the number of DDPM dithering bits ($M = 4$) have been fixed, the DLL-based TDC resolution P is designed to meet the overall $N \geq 11.58$-bit DPWM resolution for LCO-free operation. In detail:

$$P = \lceil N - \log_2 N_{\rm r} - M \rceil \tag{5}$$

where $\lceil \cdot \rceil$ is the ceiling operator. From Eqn.(5), a $P = 4$ bit DLL DTC is adopted in the proposed converter. It is worth noting that, in order to meet the target resolution with the DLL alone, an 8-bit DLL would be needed, thus resulting in 16X more area and power consumption compared to the proposed HHR-DPWM design.

IV. Experimental Results

The digitally-controlled buck converter described in Sect.II with the proposed HHR-DPWM has been fabricated in the BCD9s 110 nm technology by STMicroelectronics and occupies a total die area of 1.365 mm^2. The micrograph of the cell is shown in Fig. 6a.

To validate the HHR-DPWM design described in Sect. IIIB, the number of bits M utilized for dyadic dithering in the test chip has been made configurable via a serial interface. The measured output voltage in open loop with $V_{\rm in} = 5\,\text{V}$, $V_{\rm out} = 1.2\,\text{V}$ and $I_{\rm L} = 1\,\text{A}$ and a varying number of DDPM dithering bits M ranging from 0 to 7 is shown in Fig. 6c-6f, and the measured ripple at each M is reported in Fig.6b, revealing a negligible dithering-related ripple for $M \leq 4$, as predicted by

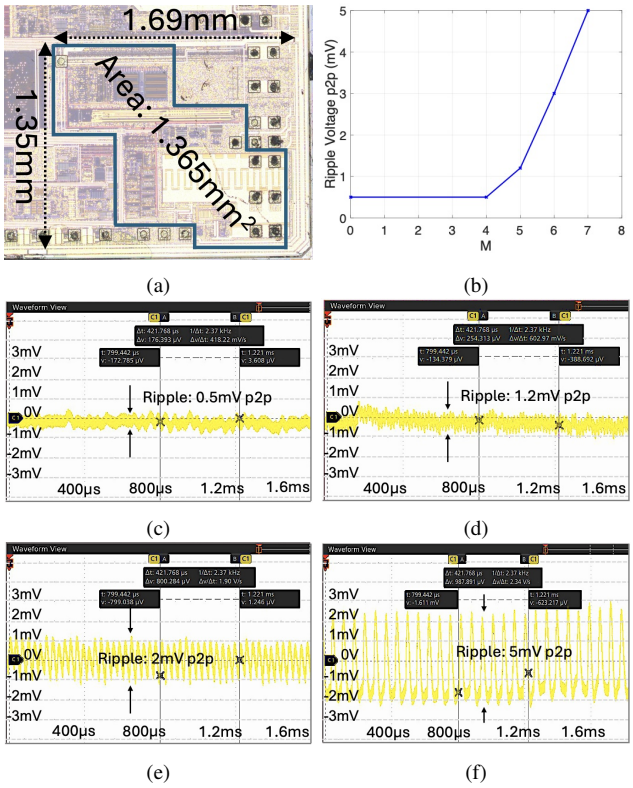

Fig. 6: a) Test-chip Micrograph b) Measured trend of output ripple voltage vs DDPM bits c) $M = 4$ d) $M = 5$ e) $M = 6$ f) $M = 7$

Eqn.(4) and confirms the validity of the HHR-DPWM design procedure described in Sect.IIIB.

In Fig. 7a the measured steady-state output voltage of the buck converter in closed loop with the optimal HHR-DPWM design parameters derived in Sect. IIIB ($Q = 5$, $P = 4$ and $M = 4$), and for $V_{\text{in}} = 5\,\text{V}$, $V_{\text{out}} = 1.2\,\text{V}$ and $I_{\text{L}} = 1\,\text{A}$ is reported revealing a DC accuracy better than 2 mV and a peak-to-peak ripple voltage of 2 mV. Under the same conditions, the load transient for a step current from 0.5 A to 2.5 A, and the line transient for a step input voltage from 4 V to 6 V are reported in Fig. 7b and Fig. 7c, respectively, revealing

TABLE I: Performance Comparison of Different Digital Buck Converter Typologies

Parameter	This Work	[20]	[7]	[21]	[22]
Technology	110nm BCD9s	180nm	180nm	180nm	180nm
V_{IN} (V)	4.0 - 6.0	3.3 - 5	2.4 - 3.6	2 - 3.3	2.7 - 4.2
V_{o} (V)	0.8 - 3.4	0.9 - 3.3	0.1 ∼ 3.5	0.8 - 1.6	0.9 - 1.2
f_{s} (MHz)	2	1	4	3 - 9.5	0.781
C (μF)	100	15	4.7	10	22
L (μH)	1.1	0.8	1.5	0.33	4.7
I_{o} (A)	2.5	7.5	1	6	0.6
Settling Time (μs)	40	–	16	6	84.5
Overshoot (mV) @ Load step	< 50 @ 2A/2μs	80.3 @ 0.5A/0.6μs	87 @ 0.4A	125 @ 1.8A/0.2μs	84 @ 0.59A
Output Ripple P2P (mV)	≈2	–	–	± 1%	< 30
Max. Efficiency (%) @ Vo	95.4, Vo = 3.4V	95.6, Vo = 3.3V	95.2	93, Vo = 1.6V	91
Output Power (W)	9	24.75	3.5	9.6	0.72
Chip Area (mm²)	1.365	1.61	–	–	–

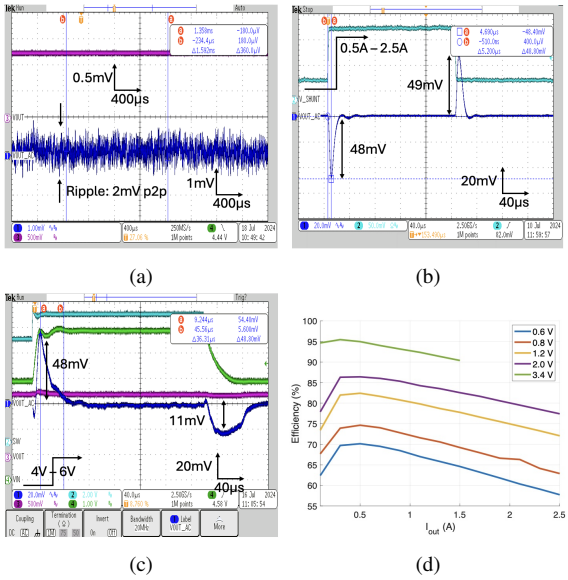

Fig. 7: a) Steady state ripple b) Load transient response c) Line transient response regulated at 1.2V d) Measured power efficiency at $V_{in} = 4\text{V}$.

an overshoot and undershoot voltage of less than 50 mV which is well recovered within 40 μs. Such results reveal excellent dynamic performance and are almost identical to those obtained without DDPM dithering and with a $P = 7$ bit DLL (not shown for space reasons), thus confirming the negligible impact of dyadic dithering on dynamic performance [19]. The measured efficiency of the power converter is finally reported in Fig. 7d, that reveals a peak efficiency of 95.4% at 4 V input voltage and 3.4 V output voltage.

The performance of the proposed digitally controlled buck converter is compared in Table. I with other digitally-controlled buck converters in the state of the art with comparable specifications, revealing a lower overshoot (50 mV) for the largest current step (2 A), and the lowest reported ripple (2 mV) and DC accuracy at low area.

V. Conclusion

A novel HHR-DPWM integrating a synchronous counter-based DPWM, a DLL-based DTC with sub-clock-cycle resolution, and DDPM dithering has been presented and designed to achieve LCO-free operation in a digitally-controlled POL buck converter targeting automotive applications. In particular the HHR-DPWM has been optimized for the minimum hardware complexity without impairing the output ripple of the power converter. The buck converter featuring the proposed HHR-DPWM has been fabricated in 110 nm BCD9s technology, achieving a 2 mV DC accuracy and 2 mV output ripple at 16X lower hardware complexity compared to a DLL-based DPWM with the same resolution, thus revealing the effectiveness of the proposed approach.

ACKNOWLEDGEMENT

This publication is part of the project PNRR-NGEU which has received funding from MUR - DM 117/2023.

REFERENCES

[1] H.-S. Youn, J.-S. Park, K.-B. Park, J.-I. Baek, and G.-W. Moon, "A digital predictive peak current control for power factor correction with low-input current distortion," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 900–912, 2016. doi:10.1109/TPEL.2015.2417194.

[2] P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodriguez, "Predictive control in power electronics and drives," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, pp. 4312–4324, 2008. doi:10.1109/TIE.2008.2007480.

[3] Maksimovic, Zane, and Erickson, "Impact of digital control in power electronics," in *2004 Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, pp. 13–22, 2004. doi:10.1109/WCT.2004.240284.

[4] I. Vaisband, M. Azhar, E. G. Friedman, and S. Köse, "Digitally controlled pulse width modulator for On-Chip power management," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 12, pp. 2527–2534, 2014. doi:10.1109/TVLSI.2013.2294402.

[5] A. Peterchev and S. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 301–308, 2003. doi:10.1109/TPEL.2002.807092.

[6] M. Bradley, E. Alarcón, and O. Feely, "Design-oriented analysis of quantization-induced limit cycles in a multiple-sampled digitally controlled buck converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 4, pp. 1192–1205, 2014. doi:10.1109/TCSI.2013.2283671.

[7] Q. Huang, C. Zhan, and J. Burm, "A 4-MHz digitally controlled voltage-mode buck converter with embedded transient improvement using delay line control techniques," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 4029–4040, 2020. doi:10.1109/TCSI.2020.3012014.

[8] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of quantization effects in digitally controlled DC–DC converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 208–215, 2007. doi:10.1109/TPEL.2006.886602.

[9] A. Peterchev and S. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, vol. 2, pp. 465–471 vol.2, 2001. doi:10.1109/PESC.2001.954158.

[10] A. Syed, E. Ahmed, D. Maksimovic, and E. Alarcon, "Digital pulse width modulator architectures," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, vol. 6, pp. 4689–4695 Vol.6, 2004. doi:10.1109/PESC.2004.1354828.

[11] A. Prodic, D. Maksimovic, and R. Erickson, "Digital controller chip set for isolated DC power supplies," in *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC '03.*, vol. 2, pp. 866–872 vol.2, 2003. doi:10.1109/APEC.2003.1179318.

[12] A. Syed, E. Ahmed, and D. Maksimovic, "Digital PWM controller with feed-forward compensation," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, vol. 1, pp. 60–66 Vol.1, 2004. doi:10.1109/APEC.2004.1295788.

[13] T. T. K. Nga, H. Abbasizadeh, T. Van Cong Thuong, and K.-Y. Lee, "A high efficiency digital PWMDC-DC converter using hybrid control technique for EH applications," in *2017 International SoC Design Conference (ISOCC)*, pp. 204–205, 2017. doi:10.1109/ISOCC.2017.8368853.

[14] J. Fang, X. Yang, L. Zhang, and Y. Tang, "An optimal digital pulse-width-modulated dither technique to enhance the resolution of wide bandgap device-based high frequency power converters," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1–1, 10 2016. doi:10.1109/TPEL.2016.2622249.

[15] J. Mooney, M. Halton, P. Iordanov, and V. O'Brien, "Dithered multi-bit sigma-delta modulator based DPWM for DC-DC converters," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2835–2839, 2015. doi:10.1109/APEC.2015.7104752.

[16] A. Kelly and K. Rinne, "High resolution DPWMin a DC-DC converter application using digital Sigma-Delta techniques," in *2005 IEEE 36th Power Electronics Specialists Conference*, pp. 1458–1463, 2005. doi:10.1109/PESC.2005.1581822.

[17] P. S. Crovetti, "All-Digital high resolution D/A conversion by dyadic digital pulse modulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 573–584, 2017. doi:10.1109/TCSI.2016.2614231.

[18] M. Usmonov, P. S. Crovetti, F. Gregoretti, and F. Musolino, "Suppression of quantization-induced limit cycles in digitally controlled DC-DC converters by dyadic digital pulse width modulation," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2224–2231, 2019. doi:10.1109/ECCE.2019.8913214.

[19] P. S. Crovetti, M. Usmonov, F. Musolino, and F. Gregoretti, "Limit-cycle-free digitally controlled DC–DC converters based on dyadic digital PWM," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 11155–11166, 2020. doi:10.1109/TPEL.2020.2978696.

[20] N. Beohar, D. Mandal, V. Parasuram, A. M. Reddy, A. Kumar, V. N. K. Malladi, K. Pappu, C. Fu, P. C. Adell, and B. Bakkaloglu, "A digitally controlled DC-DC buck converter with automatic digital PFM to PWM transition scheme," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 517–522, 2021. doi:10.1109/APEC42165.2021.9487365.

[21] M. Sun, Z. Yang, K. Joshi, D. Mandal, P. Adell, and B. Bakkaloglu, "A 6A, 93% peak efficiency, 4-phase digitally synchronized hysteretic buck converter with $\pm 1.5\%$ frequency and $\pm 3.6\%$ current-sharing error," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 3081–3094, 2017. doi:10.1109/JSSC.2017.2744618.

[22] C.-H. Tsai, C.-H. Yang, J.-H. Shiau, and B.-T. Yeh, "Digitally controlled switching converter with automatic multimode switching," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1830–1839, 2014. doi:10.1109/TPEL.2013.2265297.