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# Design of a Hybrid High Resolution Digital PWM for a Smart Power Point-of-Load Power Converter

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**Abstract**—The article presents the design and the architectural optimization of a new Hybrid, High-Resolution Digital Pulse Width Modulator (HHR-DPWM) and its implementation in an integrated, digitally-controlled, voltage-mode, point-of-load (POL) buck converter for automotive applications. The proposed HHR-DPWM architecture, which features a synchronous counter-based DPWM, a delay locked loop (DLL)-based digital-to-time converter (DTC) with sub-clock-cycle resolution, and Dyadic Digital Pulse Modulation (DDPM) dithering, is optimized to meet the requirements of the POL converter at low cost and design effort. The POL converter with the proposed HHR-DPWM is fabricated in the 110 nm BCD9s technology by STMicroelectronics. Based on measurements, the converter regulates the output voltage with 2 mV accuracy, 2 mV peak to peak ripple and a power efficiency up to 95.4% at 3.4 V output voltage.

**Index Terms**—Delay locked loop (DLL), dyadic digital pulsewidth modulation (DDPWM), limit-cycle-oscillations (LCOs), dithering.

## I. INTRODUCTION

Digitally-controlled switching-mode power converters are more and more becoming a compelling choice over the last years as they offer higher flexibility, lower cost and quicker design time compared to converters based on analog control [1]–[4]. Despite such undeniable merits, the operation of digitally-controlled converters can be severely impaired by low frequency limit-cycle-oscillations (LCOs), which arise whenever the digital pulse-width modulator (DPWM) resolution is coarser than the analog-to-digital converter (ADC) resolution, thus limiting in practice the dc accuracy of digitally-controlled converters based on standard counter-based DPWM, especially when operated at high switching frequency [5].

In this context, several techniques have been proposed to enhance the DPWM resolution and attain LCOs-free operation in digitally-controlled power converters [6]–[9]. In [10]–[12], delay-line-based time-to-digital converter is introduced in a counter-based DPWMs to achieve sub-clock cycle resolution, at the cost of increased complexity, area and sensitivity to process, voltage and temperature (PVT) variations [13]. Digital dithering techniques are adopted to increase resolution by varying the duty cycle within specific dithering patterns obtained by thermometric, sigma-delta [14]–[16], dyadic [17] [18]. Though dithering is inexpensive, it can possibly generate sub-harmonic ripple components in the output voltage.

Aiming to address the limitation of previously proposed solutions, this work presents a novel Hybrid High Resolution

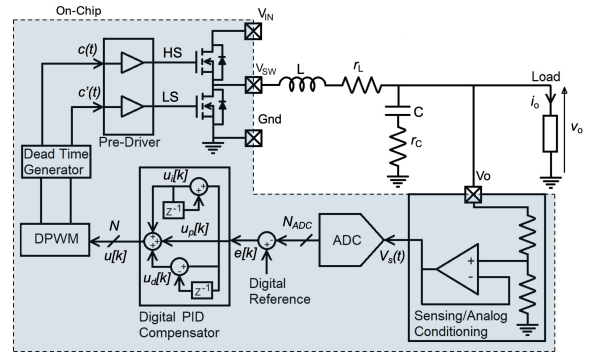


Fig. 1: Digitally controlled POL DC-DC Buck Converter

DPWM (HHR-DPWM) which entails a standard counter-based DPWM, a delay locked loop (DLL)-based TDC and a dyadic digital pulse modulation (DDPWM)-based dithering to optimally increase the DPWM effective resolution at the minimal design complexity.

The proposed design is adopted in point-of-load (POL) power converter targeting automotive applications, designed and fabricated in 110nm BCD9s technology. Experimental validation supports the claim of enhanced resolution of DPWM at low cost and without impairing output ripple and dynamic performance.

The rest of the article is organized as follows: Sect. II revises the architecture of digitally controlled power converter emphasizing the requirement of high resolution DPWM. In Sect. III, the HHR-DPWM architecture is thoroughly presented and its optimal design is discussed. Further, Sect. IV includes the experimental setup and results along with performance comparison with other state-of-the-art digital buck converters. Some concluding remarks are finally drawn in Sect. V.

## II. DIGITALLY CONTROLLED BUCK CONVERTER ARCHITECTURE

In this work, a HHR-DPWM targeting the requirements of a digitally-controlled POL synchronous DC-DC Buck converter for automotive applications, intended to convert the  $5\text{ V} \pm 10\%$  voltage provided by a first-stage regulator from the battery voltage, and converting it into a wide range of configurable regulated voltages from 0.8 V to 3.4 V with mV-range accuracy, as needed to supply on-vehicle electronic control units (ECUs) with currents in the 0.5 A - 2.5 A range.



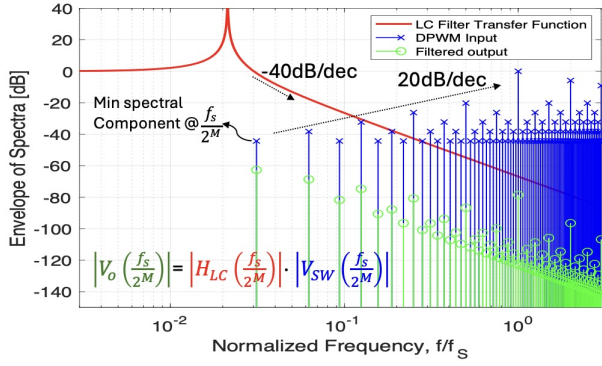


Fig. 4: Envelope Dyadic PWM Spectra.

but there is trade-off between regulation performances and frequency behavior.

### B. HHR-DPWM Architecture Optimization

The proposed HHR-DPWM is designed to attain the target  $N > 11.58$  bit resolution required for the POL buck converter described in Sect.II at minimum hardware complexity and without output ripple degradation.

For this purpose, the maximum possible number of DPWM quantization levels compatible with the system clock frequency  $f_{\text{clk}} = 40$  MHz and the switching frequency  $f_s = 2$  MHz, i.e.  $N_r = f_{\text{clk}}/f_s = 20$  are obtained from the counter-based DPWM, which is directly driven with the  $Q = \lceil \log_2 N_r \rceil = 5$  most significant bits of the command word.

Then, to reduce the DLL hardware complexity, the DDPM dithering block is designed to provide the maximum resolution enhancement (i.e., with the largest possible  $M$ ) without resulting in output ripple degradation. From the envelope of the spectra of Dyadic DPWM signals reported in [19] and shown in Fig.4, the DDPM dithering-induced output ripple is dominated by the dithering spectral component at the lowest sub-harmonic frequency  $f_s/2^M$ , which is scarcely attenuated by the  $LC$  filter of the power converter. In view of that, the maximum number of DDPM dithering bits  $M$  is derived imposing that the amplitude of the lowest sub-harmonic component after  $LC$ -filtering is less than the target output voltage accuracy of the converter, i.e.  $0.5 q_V^{\text{(ADC)}}$ . Since, based on [19], the amplitude of the sub-harmonic at  $f_s/2^M$  before filtering is  $V_{\text{in}}/2^{N-M}$ , the above condition to avoid output ripple degradation reads:

$$H \frac{V_{\text{in}}}{2^{N-M}} \cdot \left| H_{\text{LC}} \left( \frac{f_s}{2^M} \right) \right| \leq \frac{V_{\text{FS}}}{2^{N_{\text{ADC}}+1}} \quad (3)$$

where  $|H_{\text{LC}}(f_s/2^M)|$  is the magnitude of the  $LC$  filter response at  $f_s/2^M$ , that gives:

$$M \leq \frac{1}{3} \left[ \log_2 \left( \frac{f_s^2 \cdot V_{\text{FS}}}{f_c^2 \cdot H \cdot V_{\text{in}}} \right) + N - N_{\text{ADC}} - 1 \right] \quad (4)$$

where  $f_c = 1/(2\pi\sqrt{LC}) = 12$  kHz for the POL converter considered in Sect.II. From Eqn.(4) the maximum number of DDPM dithering bits is 4.58 bits, so a DDPM dithering resolution  $M = 4$  is fixed to avoid output ripple degradation.

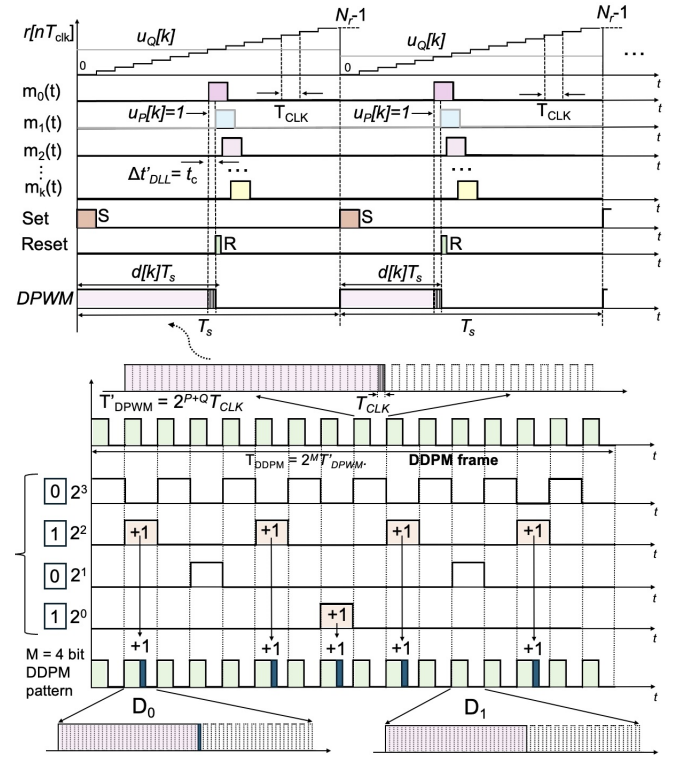


Fig. 5: Waveform of Counter-based + DLL + Dyadic Dithering

Once the number of levels of the counter-based DPWM ( $N_r = 20$ ) and the number of DDPM dithering bits ( $M = 4$ ) have been fixed, the DLL-based TDC resolution  $P$  is designed to meet the overall  $N \geq 11.58$ -bit DPWM resolution for LCO-free operation. In detail:

$$P = \lceil N - \log_2 N_r - M \rceil \quad (5)$$

where  $\lceil \cdot \rceil$  is the ceiling operator. From Eqn.(5), a  $P = 4$  bit DLL DTC is adopted in the proposed converter. It is worth noting that, in order to meet the target resolution with the DLL alone, an 8-bit DLL would be needed, thus resulting in 16X more area and power consumption compared to the proposed HHR-DPWM design.

## IV. EXPERIMENTAL RESULTS

The digitally-controlled buck converter described in Sect.II with the proposed HHR-DPWM has been fabricated in the BCD9s 110 nm technology by STMicroelectronics and occupies a total die area of 1.365 mm<sup>2</sup>. The micrograph of the cell is shown in Fig. 6a.

To validate the HHR-DPWM design described in Sect. IIIB, the number of bits  $M$  utilized for dyadic dithering in the test chip has been made configurable via a serial interface. The measured output voltage in open loop with  $V_{\text{in}} = 5$  V,  $V_{\text{out}} = 1.2$  V and  $I_L = 1$  A and a varying number of DDPM dithering bits  $M$  ranging from 0 to 7 is shown in Fig. 6c-6f, and the measured ripple at each  $M$  is reported in Fig.6b, revealing a negligible dithering-related ripple for  $M \leq 4$ , as predicted by

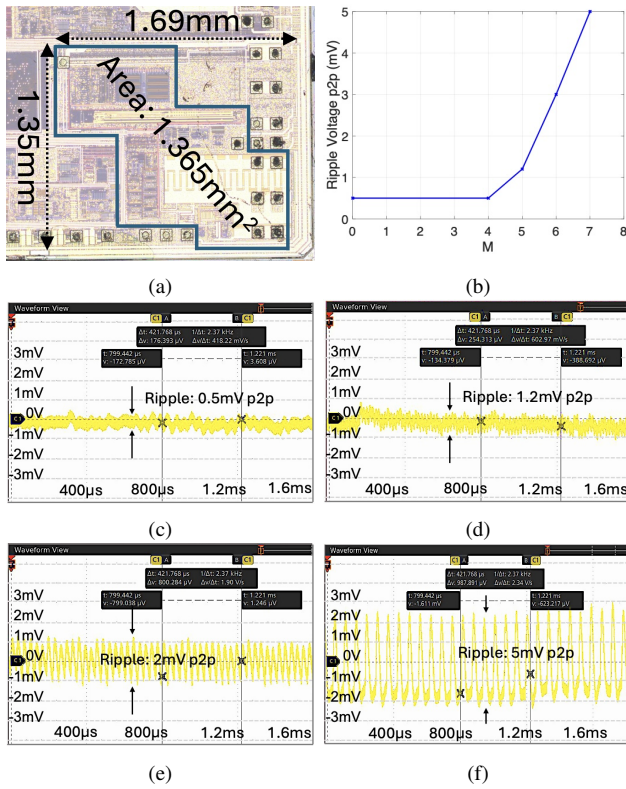


Fig. 6: a) Test-chip Micrograph b) Measured trend of output ripple voltage vs DDPM bits c)  $M = 4$  d)  $M = 5$  e)  $M = 6$  f)  $M = 7$

Eqn.(4) and confirms the validity of the HHR-DPWM design procedure described in Sect.IIIB.

In Fig. 7a the measured steady-state output voltage of the buck converter in closed loop with the optimal HHR-DPWM design parameters derived in Sect. IIIB ( $Q = 5$ ,  $P = 4$  and  $M = 4$ ), and for  $V_{in} = 5V$ ,  $V_{out} = 1.2V$  and  $I_L = 1A$  is reported revealing a DC accuracy better than 2 mV and a peak-to-peak ripple voltage of 2 mV. Under the same conditions, the load transient for a step current from 0.5 A to 2.5 A, and the line transient for a step input voltage from 4 V to 6 V are reported in Fig. 7b and Fig. 7c, respectively, revealing

TABLE I: Performance Comparison of Different Digital Buck Converter Typologies

Parameter	This Work	[20]	[7]	[21]	[22]
Technology	110nm BCD9s	180nm	180nm	180nm	180nm
$V_{in}$ (V)	4.0 - 6.0	3.3 - 5	2.4 - 3.6	2 - 3.3	2.7 - 4.2
$V_o$ (V)	0.8 - 3.4	0.9 - 3.3	0.1 ~ 3.5	0.8 - 1.6	0.9 - 1.2
$f_s$ (MHz)	2	1	4	3 - 9.5	0.781
$C$ ( $\mu$ F)	100	15	4.7	10	22
$L$ ( $\mu$ H)	1.1	0.8	1.5	0.33	4.7
$I_o$ (A)	2.5	7.5	1	6	0.6
Settling Time ( $\mu$ s)	40	-	16	6	84.5
Overshoot (mV) @ Load step	< 50 @ 2A/2 $\mu$ s	80.3 @ 0.5A/0.6 $\mu$ s	87 @ 0.4A	125 @ 1.8A/0.2 $\mu$ s	84 @ 0.59A
Output Ripple P2P (mV)	$\approx 2$	-	-	$\pm 1\%$	< 30
Max. Efficiency (%) @ $V_o$	95.4, $V_o = 3.4V$	95.6, $V_o = 3.3V$	95.2	93, $V_o = 1.6V$	91
Output Power (W)	9	24.75	3.5	9.6	0.72
Chip Area (mm <sup>2</sup> )	1.365	1.61	-	-	-

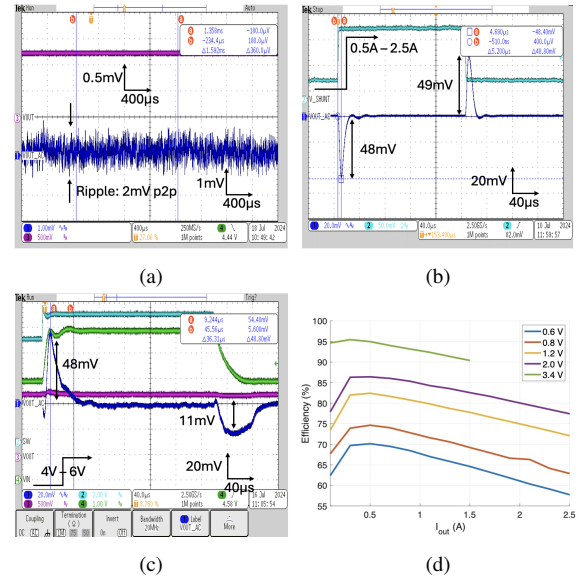


Fig. 7: a) Steady state ripple b) Load transient response c) Line transient response regulated at 1.2V d) Measured power efficiency at  $V_{in} = 4V$ .

an overshoot and undershoot voltage of less than 50 mV which is well recovered within 40  $\mu$ s. Such results reveal excellent dynamic performance and are almost identical to those obtained without DDPM dithering and with a  $P = 7$  bit DLL (not shown for space reasons), thus confirming the negligible impact of dyadic dithering on dynamic performance [19]. The measured efficiency of the power converter is finally reported in Fig. 7d, that reveals a peak efficiency of 95.4% at 4V input voltage and 3.4 V output voltage.

The performance of the proposed digitally controlled buck converter is compared in Table. I with other digitally-controlled buck converters in the state of the art with comparable specifications, revealing a lower overshoot (50 mV) for the largest current step (2 A), and the lowest reported ripple (2 mV) and DC accuracy at low area.

## V. CONCLUSION

A novel HHR-DPWM integrating a synchronous counter-based DPWM, a DLL-based DTC with sub-clock-cycle resolution, and DDPM dithering has been presented and designed to achieve LCO-free operation in a digitally-controlled POL buck converter targeting automotive applications. In particular the HHR-DPWM has been optimized for the minimum hardware complexity without impairing the output ripple of the power converter. The buck converter featuring the proposed HHR-DPWM has been fabricated in 110 nm BCD9s technology, achieving a 2 mV DC accuracy and 2 mV output ripple at 16X lower hardware complexity compared to a DLL-based DPWM with the same resolution, thus revealing the effectiveness of the proposed approach.

## ACKNOWLEDGEMENT

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