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A Pseudo-CMOS bootstrap DIGOTA in a 600nm Flexible IGZO Technology / Sousa, D., Marcelino, J., Santos, A., Viana, H., Xavier, J., Barquinha, P., Toledo, P., Crovetti, P.. - ELETTRONICO. - (2024). (2024 IEEE International Flexible Electronics Technology Conference (IFETC) Bologna (Ita) September 15-18, 2024) [10.1109/IFETC61155.2024.10771852].

Availability:
This version is available at: 11583/3001347 since: 2025-06-28T10:03:16Z

Publisher:
IEEE

Published
DOI:10.1109/IFETC61155.2024.10771852

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(Article begins on next page)

20 November 2026

A Pseudo-CMOS bootstrap DIGOTA in a 600nm Flexible IGZO Technology

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***Abstract*—The design of a Digital-Based Operational Transconductance Amplifier (DIGOTA) featuring pseudo-CMOS inverters based on bootstrap pseudo-pMOS devices integrated in a 600 nm Indium-Gallium-Zinc-Oxide (IGZO) Thin-Film Transistors (TFT) Flexible Integrated Circuits (FlexICs) technology is presented in this paper. Based on post-layout simulations, the proposed DIGOTA operates at 3 V power supply and achieves a DC gain of 33.8 dB and a GBW of 64.9 kHz at 221 μW power. Despite maintaining performance comparable to the previous Flexible DIGOTA, this new design occupies 26% less area, requires less logical gates, and enhances the slew rate whilst maintaining reasonable energy efficiency and large signal figures of merit of 14.5 MHz·pF/mW and 50.2 V.pF/s.mW, respectively.**

***Index Terms*—Flexible Integrated Circuits (FlexICs), Operational Transconductance Amplifier (OTA), Digital-Based Circuit, Indium-Gallium-Zinc-Oxide (IGZO), Thin-Film Transistors (TFT), Pseudo-CMOS Bootstrapped Inverter**

I. Introduction

Recently, relevant progress in circuit design is being made with the development of flexible integrated circuits using TFTs [1]. These environmental-friendly circuits are essential for the creation of innovative products that can capitalize on their low fabrication costs [2], high efficiency, and unique physical properties such as flexibility [3], [4] and light transparency. Such unique features, indeed, are paving the way to many applications in the Internet of Things (IoT), in display technology and wearable electronics [5]. In details, flexible electronics has been rapidly emerging as an alternative to conventional silicon chips in areas where the use of inexpensive devices is of paramount importance, giving rise to more complex and useful circuits such as dynamic frequency dividers [6], a flexible 32-bit ARM processor [7], a flexible MOS 6502 microprocessor [8], a hardwired machine learning processing engine [9] and AM receivers [10] that can be integrated into a variety of consumer products and industrial applications.

Contributions to flexible analog building blocks such as Operational Transconductance Amplifiers (OTAs) are still limited in number [11–15] and generally exhibit relatively poor performance due to the intrinsic limitations of IGZO technology and to the lack of complementary devices.

In this context, digital-based analog design techniques [16–20] have gained momentum, leading to the design of a flexible DIGOTA in 800 nm TFT FlexIC technology [21]. While the DIGOTA design presented in [21] is based on nMOS-only logic gates with resistive loads [], this work explores explores an alternative DIGOTA implementation which takes advantage of a pseudo-CMOS logic gates in which a transistor with complementary polarity (pseudo-pMOS) is obtained by bootstrap techniques [22], [23]. The new topology is designed and tested in the 600 nm a-IGZO FlexIC technology provided by Pragmatic.

The rest of this work is structured as follows: Section II describes the proposed circuit and how it works, highlighting the differences from the original design first published in [21]. The results of the post-layout are discussed in section III and subsequently compared with the state-of- the-art, and finally, section IV summarizes the results of the present work.

II. Proposed Design and Circuit Description

The proposed DIGOTA is a single-ended OTA based on the architecture originally introduced in [24] Fig. 1a. In details, it entails a resistive summing network, a cascade of inverters, an output stage and a common-mode extractor, each comprising a NOR logic gate and a three-state digital buffer.

The operation of the circuit is related to the digital outputs OUT+ and OUT- of the cascade of inverters: if OUT+ and OUT- have different binary values (OUT+="1"("0") and OUT-="0"("1")) the output stage is activated and drives the output load. Otherwise, considering OUT+=OUT-, the common-mode extractor feedback circuit its activated: if the logic value is high ($V_{CM} > V_{TP}$), it lowers the V_{CM} node; if the logic value is low ($V_{CM} < V_{TP}$), it increases the V_{CM} node in order to return to one of the first two conditions. A detailed description of the DIGOTA operation is presented in [24],[25].

The first inverters of the cascade are responsible for the conversion from an analog voltage to a digital signal and are particular important for the DIGOTA performance. In the former DIGOTA implementation in IGZO technology [21], nMOS-only resistive inverters have been introduced, which present a low trip point voltage (V_{TP}) and asymmetric rise time [26].

Aiming to address the limitations of nMOS-only resistive gates in IGZO technology, the pseudo-CMOS bootstrap architecture shown in Fig.1a was introduced in [23] to enable a higher trip point, a faster rise time, and rail-to-rail output swing, at the cost of higher power dissipation and area. The faster rise time results in increase and symmetric slew rate and higher DC gain compared with a resistive-load inverter. In consideration of these advantages, pseudo-CMOS inverters are

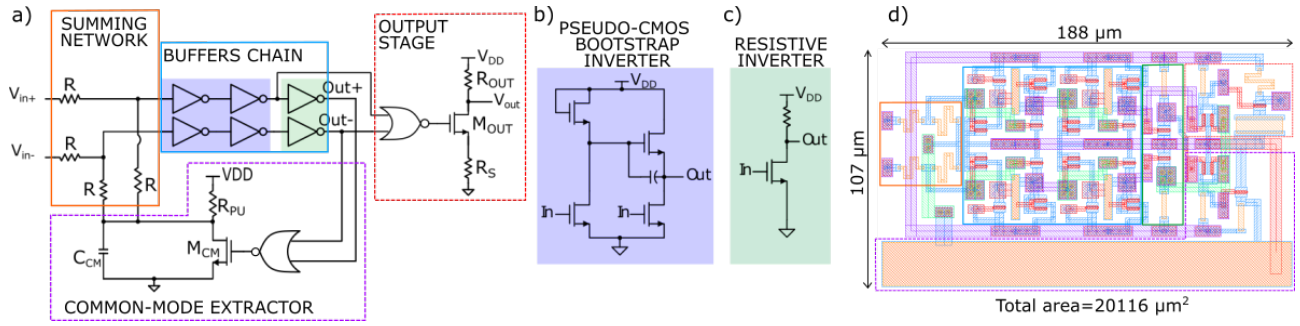


Fig. 1: DIGOTA schematic(a), pseudo-CMOS bootstrap inverter's schematic (b), resistive inverter's schematic (c), DIGOTA layout (d).

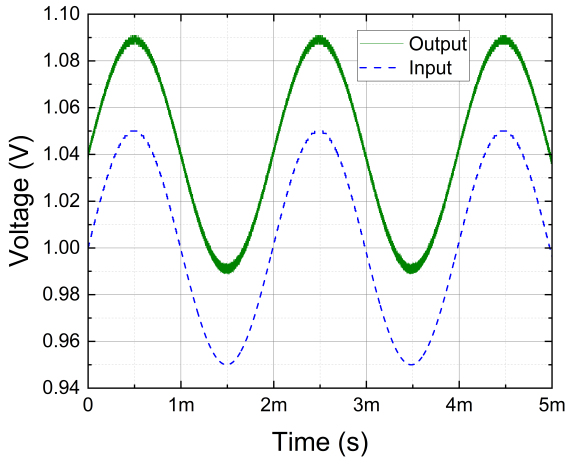


Fig. 2: Post-layout transient simulated input and output wave in voltage-follower configuration.

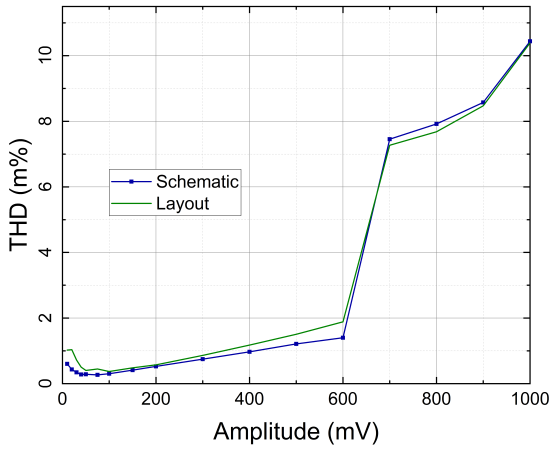


Fig. 4: THD (m%) versus input amplitude.

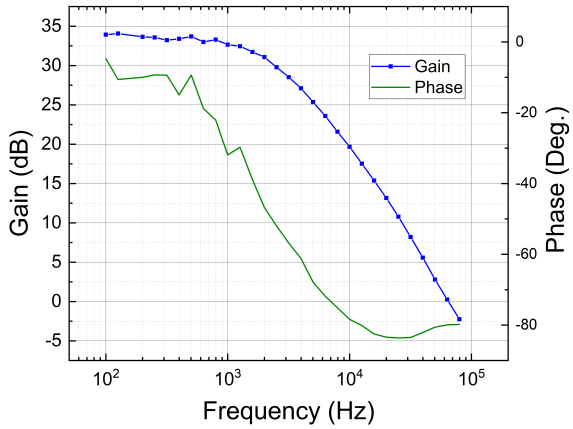


Fig. 3: Simulated frequency response.

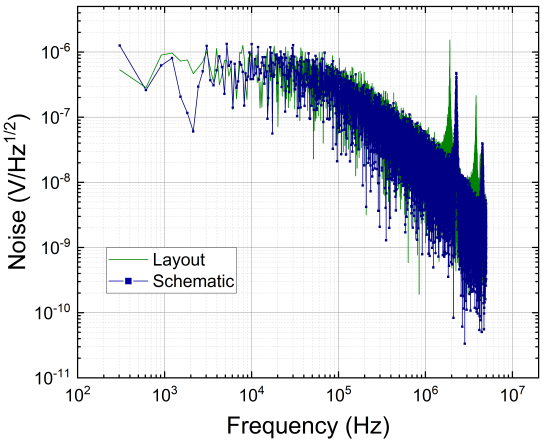


Fig. 5: Noise power spectral density.

introduced in the first stages of the buffer chain of the DIGOTA design proposed in this work, taking into advantage the higher common mode input rage offered by this architecture.

III. Simulation Results

The Pseudo-CMOS DIGOTA describeb in II has been designed for fabrication in the PragmatIC 600 nm IGZO TFT technology and its layout is shown in Fig. 1 (b). The DIGOTA performance have been assessed based on post-layout simulations in the voltage follower configuration, with a supply voltage (V_{DD}) of 3 V, and a load of 50 pF in parallel with 4 M. Corner analysis has been performed to assess the impact of a 10% variation in V_{DD}, encompassing a range of transistor variations (fast, typical, and slow) and resistance values (maximum, nominal, and minimum).

The response to a sinewave input at 50 mV peak amplitude and 500 Hz frequency is presented in Fig. 2. The output presents the characteristic ripple observed in all DIGOTAs. The frequency response of the amplifier is presented in Fig. 3. Due to its dynamic operation, this analysis was conducted by

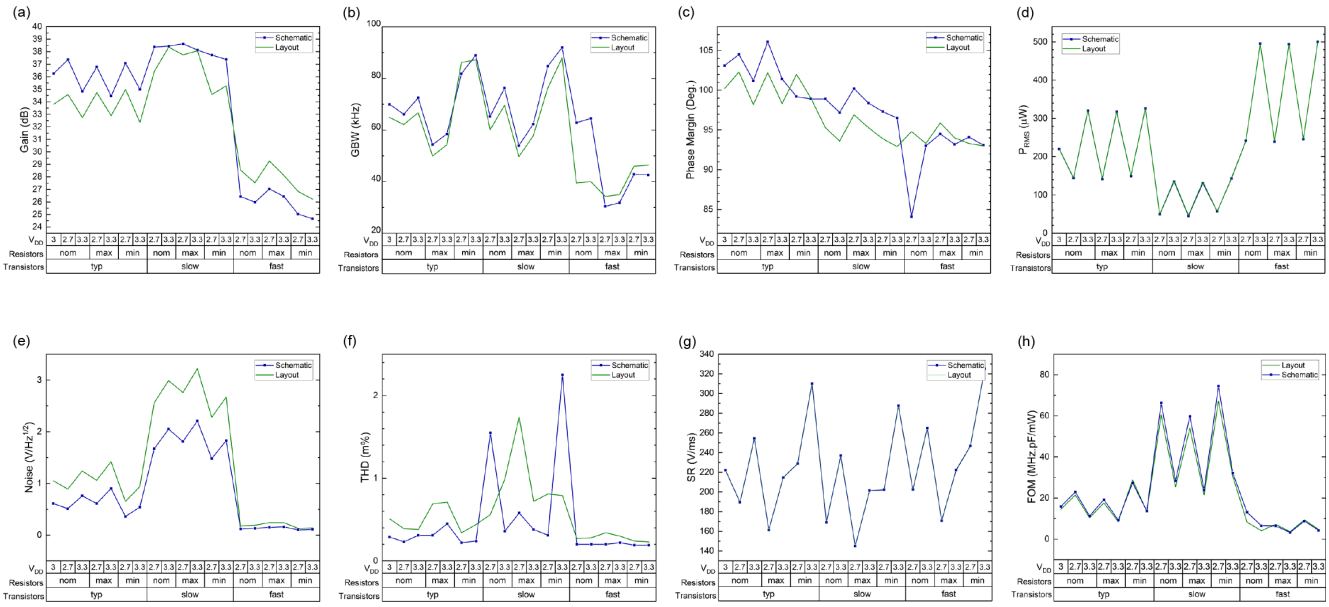


Fig. 6: PivotCharts of schematic and post-layout simulation results for (a) DC gain, (b) gain band width (GBW), (c) phase margin (PM), , (d) power dissipation, (e) in-band noise, (f) THD, (g) slew rate (SR) and (h) figure of merit (FoM).

sweeping the input wave frequency in a transient simulation. It is possible to observe that the circuit behaves as a single pole system, with the pole located at around 2 kHz. has a DC gain of 33.8 dB, a gain-bandwidth product (GBW) of 65 kHz, and a phase margin of 100°.

Considering a noise bandwidth close to 100×GBW, i.e. 10 GHz, Fig. 5 reveals an in-band noise of 1.05 mV_{rms}. The Total Harmonic Distortion (THD) analysis presented in Fig. 4 aims to evaluate the impact of input amplitude on the output distortion. The THD value is as low as 0.40 % at 50 mV amplitude and less than 10.4% up to 1 V peak amplitude.

The circuit's performance between schematic-only and post-layout simulation results across process-voltage (PV) corners, pivot charts are presented in Fig. 6.

Post-layout simulations reveal a nominal value of DC gain of 33.8 dB and a worst case of 26.2 dB while demonstrating the tendency of lowering the DC gain for fast transistors corners, as can be seen in Fig. 6 (a).

Regarding GBW results, presented in Fig. 6 (b), it is possible to conclude that this parameter is one of the most sensitive to PV since it varies from 65 kHz in the nominal corner, with the worst corner lowering it to 35 kHz. Once more, it is possible to notice that the maximum resistance corners present a generally lower GBW due to the increasing output impedance that leads to a lower frequency of the dominant pole.

On the other hand the PM is very insensitive to corners variation and is always above 84°, as shown in Fig 6 (c), which corresponds to a robustly stable closed-loop operation across corners, as expected for a single-pole circuit.

From Fig. 6 (d), power consumption is strongly correlated with the transistor's process corner. The pre-layout analysis yielded a value of 220 μW for the nominal case, and 500 μW for the worst case. Notably, the inclusion of parasitic elements did not significantly alter these values, with post-layout results indicating an almost identical consumption of 221 μW for the nominal condition and 500 μW for the worst-case corner.

Fig. 6 (e) presents the pivot-chart for in-band noise. It is possible to see that the value for the nominal corner is 1.05 mV_{rms} and for the worst corner is 2.99 mV_{rms}.

The THD parameter was also tested across corners for an input amplitude value of 50 mV and 500 Hz of input frequency and the results are presented in Fig. 6 (f). Regarding post-layout values, despite the worst corner presenting a value of 1.74%, the remaining corners present a lower THD, including the nominal value, with a value of 0.51 %.

From Fig. 6 (g) it is observed that parasitics have almost no influence on the slew rate. The nominal value changed from 221.9 kV/s to 221.6 kV/s and the worst case value from 145.1 kV/s to 144.8 kV/s.

The energy efficiency figure of merit (FoM), defined as $(\text{GBW}\cdot C_{\text{out}})/\text{Power}$, across PV variation is shown in Fig.6 (h). For post-layout, the obtained values were 14.5 MHz.pF/mW and 3.55 MHz.pF/mW for nominal and worst corner, respectively.

Table I presents the comparison between existing literature and the proposed topology for typical and worst PV corner. The proposed DIGOTA operates at the lowest supply voltage and achieves the highest slew rate, while occupying the smallest area among the other layouts under consideration. Despite the power consumption is about 2× compared to [21] at comparable GBW, but it is competitive with all the other works. A significant benefit of the selected inverter topology is its superior slew rate.

As mentioned in section 2, the gain is highly connected with the reduced number of inverters in the inverter chain. Although the DC gain is not the highest among all the presented in Table I it could be increased just by increasing the number

TABLE I: Comparison of DIGOTA results with the State-of-the-Art among Flexible Operational Transconductance Amplifiers.

	[27]$^{+}$	[28]$^{+}$	[29]$^{+}$	[30]$^{+}$	[21]*	This work*	
						Typical	Worst corner
Technology (Lmin [μm])	a-IGZO (3)	a-IGZO	Flexible IGZO (0.8)	a-IGZO	Flexible IGZO (0.8)	Flexible IGZO (0.6)	
Topology	Analog // Pseudo-CMOS	Analog // Positive feedback	Analog // Common source	Analog // Pseudo-CMOS	Digital based // Resistive	Digital based // Pseudo-CMOS	
DC gain [V]	**57**	32.67	28.9	22.5	36.3	33.8	26.2
GBW [Hz]	311 k	200 k	**3.34 M**	31 k	86 k	64.9 k	34.29 k
Output Load	-	-	50 fF // 1.25 M	15 pF // 1 M	50 pF // 8 M	50 pF // 4 M	
PM [degrees]	75	35.8	-	-	87	**100.2**	92.9
V_{DD} [V]	10	15	8	5	3.3	3	
Consumption [mW]	2.43	0.68	14.2	0.160	**0.113**	0.221	0.500
Area [mm^2]	3.69	4.42	0.33	9.83	0.0252	**0.020**	
Noise [mV_{rms}]	-	-	-	-	**0.087**	1.05	2.99
Slew Rate [V/ms]	-	-	-	-	187	**222**	145
**FoM [MHz.pF/mW]	-	-	11.73	2.91	**38.05**	14.49	3.55

$^{+}$experimental; *simulation, MC mean value; **FOM = $\frac{\text{GBW}\cdot C_{\text{out}}}{\text{Power}}$; **best performance in bold**;

of inverters at the cost of higher power dissipation and larger area.

In spite of such improvements, it can be concluded that, while the introduction of pseudo-CMOS solutions and bootstrapped stages result in a significant gain and performance improvement in traditional analog OTAs in IGZO technologies, the performance of DIGOTAs in Flexible IGZO are only slightly affected in consideration of the digital operation its inherent insensitivity to the analog characteristics of the devices.

IV. Conclusion

This paper presented a Digital-Based (OTA) in a 600 nm IGZO TFT FlexICs technology and exhibited post-layout simulation results comparing them with state-of-the-art literature. The proposed DIGOTA explored a new topology by implementing pseudo-CMOS bootstrap inverters. This modification allowed to achieve a DC gain of 33.8 dB and a GBW of 64.9 kHz, which is in line with the previous DIGOTA, but with less area and fewer gates. The proposed topology also improved the slew rate and the phase margin.

Acknowledgment

The authors acknowledge the support of PragmatIC for providing the technology PDK. This work was financed by (...).

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