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Digital Control of a Multilevel Interleaved DC-DC GaN Converter for Fuel Cell Traction Applications

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***Abstract*—Nowadays, fuel cells represent a promising alternative to replace battery packs for electric vehicles where weight or the limited range is a concern. With respect to a battery pack, built up to 800 V, the output voltage of fuel cell stacks is rather low (typically below 200 V) and it is strongly dependent on the load current. Therefore, the integration of a fuel cell in an electrical powertrain needs a DC-DC converter. To maximize the power density, the gallium-nitride (GaN) technology represents an interesting solution as it allows unprecedented performance in terms of switching frequency. As the rated voltage of available GaN devices is limited to 650 V, multilevel solutions must be employed for DC-DC converters whose output is 800 V. As the switching frequencies are usually above 100 kHz, the control of such converters is challenging, especially when multiple interleaved switching cells must be controlled. The literature reports several publications focusing on the adopted topologies for DC-DC conversion, while few papers deal with the digital control of such multilevel DC-DC converters. Therefore, the goal of this paper is the digital control applied to a high-power multilevel interleaved GaN DC-DC converter for an electrical powertrain fed by fuel cell.**

***Index Terms*—Fuel cells, Digital control, DCDC converter, GaN**

I. Introduction

Fuel cells (FCs) are considered today as a valid replacement of heavy and bulky battery packs in electrical powertrains for trucks, buses, or commercial vehicles [1]. FCs offer a high energy density and can effectively solve problems related to the energy waste in long-distance transportation, providing a more sustainable and efficient solution compared to traditional battery systems [2]. However, a one-to-one replacement of the battery pack with the fuel cell stack is not possible due to the non-linear and low voltage output characteristics of the fuel cell. Consequently, a boost DC-DC converter is usually employed in FC electrical vehicles (FCEV) as an electronic interface between the FC and the traction inverter [3], as shown in the diagram of Fig. 1. This configuration also includes a smaller battery storage for peak power shaving and regenerative braking.

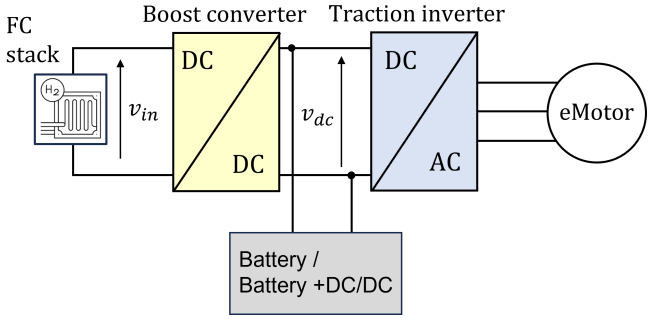


Fig. 1. FC powered electrical powertrain with 3d renders of the converters.

Traditional DC-DC boost converters have advantages in terms of cost and low complexity, but they encounter significant limitations as the required voltage increases [4]. As power demands grow, the efficiency and reliability of conventional boost converters diminish, necessitating advanced designs to meet these stringent requirements.

As a consequence, the choice of an interleaved structure can significantly increase the requested target power. The interleaved parallel configuration is achieved through the parallelization of multiple power converter modules, bringing significant benefits: it reduces the current and voltage ripple and increases the effective switching frequency at the input and output of the converter, thereby improving the dynamic response of the circuit [5]. This configuration also distributes the thermal load among the modules, enhancing the overall

thermal management and reliability of the system.

Furthermore, conventional silicon power semiconductors introduce problems when involved in high-power applications [6]. Silicon semiconductors have lower breakdown voltage capabilities, which restricts their ability to handle high voltages without undergoing avalanche breakdown. This limitation leads to increased stress on the components, potentially causing failure during high-voltage operations. Additionally, silicon devices suffer from high conduction and switching losses. To avoid excessive commutation losses due to the higher frequency, the introduction of wide bandgap (WBG) devices is beneficial.

The gallium-nitride (GaN) technology represents an interesting solution to increase the power density of DC-DC converters, as it allows unprecedented performance in terms of switching frequency [7]. GaN devices offer lower conduction losses and higher efficiency compared to silicon-based devices, making them ideal for high-frequency operations. However, the rated voltage of available high-current GaN devices is limited to 650 V, necessitating multilevel solutions for DC-DC converters whose output exceeds this voltage threshold [7]. On the other hand, higher switching frequencies require further studies related to the inductor's design to avoid excessive losses. Different inductor topologies, such as interleaved inductors, represent a valuable solution to mitigate these constraints.

Indeed, to reduce costs and increase power density, coupled inductors are introduced, adding to the system an increased level of complexity [8]. Moreover, as the switching frequencies are usually above 100 kHz, the control of such converters is challenging, especially when multiple interleaved switching cells must be controlled. The literature reports publications focusing more on the design of multilevel topologies for DC-DC conversion [9], while few papers deal with the digital control of such solutions [10].

Therefore, the goal of this paper is the digital control applied to a high-power, multilevel interleaved GaN DC-DC converter using a switching frequency of 100 kHz. An accurate analysis of the sampling time, synchronization, and implementation of the control strategy routine are described. The results and experimental validation are provided on a 5 kW prototype.

II. DC-DC Converter Control

As shown in Fig. 2, the considered DC-DC converter consists of two cascaded units (P and N). The cascaded structure is superior to the conventional H-bridge structure as it achieves an higher efficiency due to a lower stress on passive elements and a lower total harmonic distortion [11]. Each cell is then composed of two interleaved switching cells using coupled inductors L_{dm} and input single inductors L_{cm}. The use of coupled inductors significantly influences inductor and converter sizing [12], while reducing the current ripple and switching losses [13].

The proposed digital DC-DC control scheme is presented in Fig. 3. Common-mode and differential mode controllers are implemented in a cascaded configuration with an outer

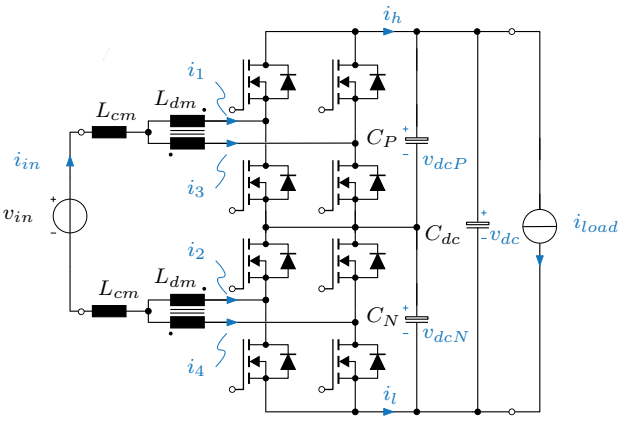


Fig. 2. Considered DC-DC converter structure.

voltage control loop. The presence of a voltage control loop balancing is mandatory due to the split DC-Link of the cascaded structure. Furthermore, an inner common mode and a differential mode current control loops are implemented.

Five control loops have been implemented: two main (common mode) voltage and current loops (Fig. 3) and three additional (differential mode) loops related to the voltage capacitor balancing and current balancing to avoid inductor saturation. The currents flowing in the differential inductors, i_1, i_3, i_2, i_4, the input voltage and capacitor output voltages, v_{in}, v_{dcP} and v_{dcN} are measured. The i_{in} current can be evaluated by (1):

$$i_{in} = i_1 + i_3 = i_2 + i_4 \tag{1}$$

and v_{dc} is estimated as the sum of the voltages v_{dcP} and v_{dcN}.

In order to evaluate the control parameters, the small signal model of the converter is defined [14]. Based on the simplified models shown in Fig. 4, the following state space equations are derived:

$$\begin{cases} 2L_{cm}\dfrac{di_{in}}{dt} = v_{in} - v_d \\ C_{eq}\dfrac{dv_{dc}}{dt} = i_h - i_{load} \\ C_P\dfrac{dv_{dc,P}}{dt} - C_N\dfrac{dv_{dc,N}}{dt} = i_{vb} \\ L_{dm}\dfrac{di_{ib}}{dt} = v_{dc,P1} - v_{dc,P2} \end{cases} \tag{2}$$

where C_{eq} is the equivalent capacitor at the converter output, v_d is the voltage across the switch, i_h is the sampled high side current: the i_{vb} is the DC-Link midpoint current and i_{ib} is the differential current recirculating in high side and low side of the converter, as reported in (3).

$$\begin{cases} C_{eq} = \left(\dfrac{C_P C_N}{(C_P + C_N)} + C_{dc}\right) \\ v_d = dv_{dc} \\ i_{vb} = i_{in}(d_h - d_l) \\ i_{ib} = \dfrac{i_1 - i_3}{2} \end{cases} \tag{3}$$

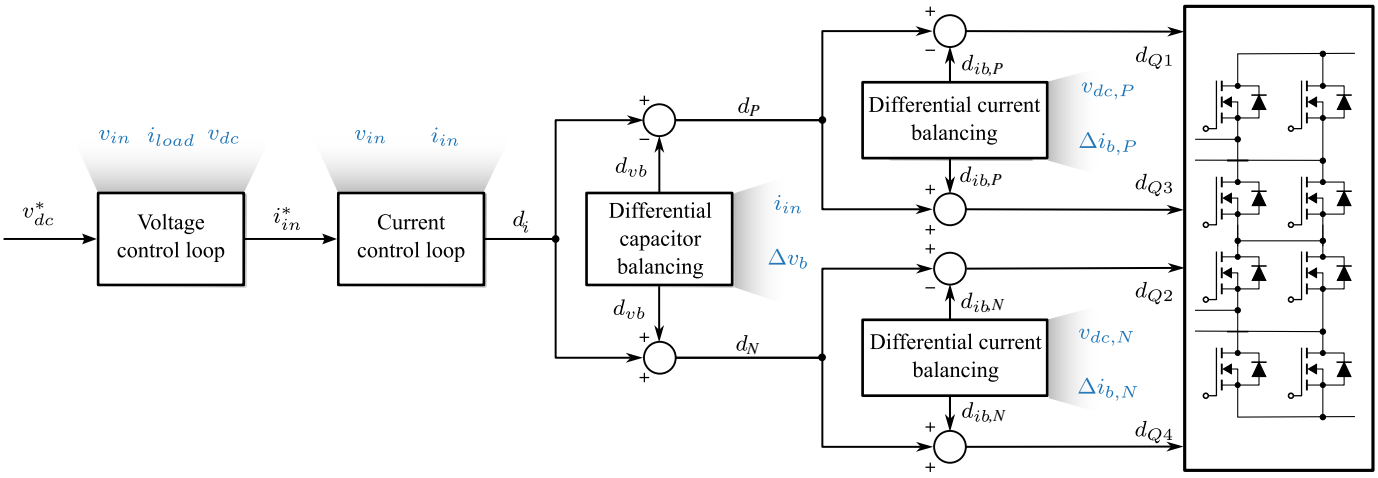


Fig. 3. Proposed DC-DC converter control loop.

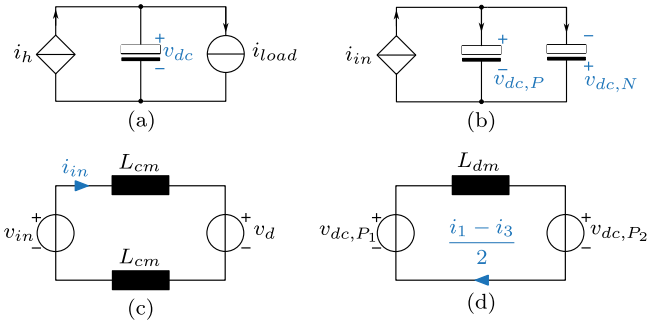


Fig. 4. Equivalent circuit representation of the system state-space equations: **(a)** Voltage loop, **(b)** Voltage capacitor balancing, **(c)** Current loop, **(d)** Differential inductor current balancing.

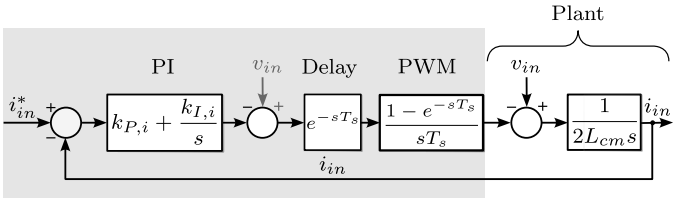


Fig. 5. Detailed block diagram of the main current control loop

A. Current control loop

The external current control is implemented to achieve zero steady-state tracking error between the desired input current and the feedback one evaluated through (1). Fig. 5 presents the block scheme. The voltage to current plant transfer function is evaluated through the state space equations presented in (2) as

$$G_{p,i} = \frac{i_{in}(s)}{v_d(s)} = \frac{1}{s2L_{cm}} \tag{4}$$

Disturbance components are disregarded in the plant evaluation and compensated by a suitable feed-forward term in the control loop routine. Furthermore, the digital implementation of the control loop introduces delays that affects negatively the control routine [15], in particular a first contribution is related to the digital processing and one due to the PWM modulator that introduced a zero-order hold (ZOH) effect over the sampling period. As a result, the delay transfer function is evaluated as:

$$G_{d,i} = e^{-sT_s} \frac{1 - e^{-sT_s}}{sT_s} \tag{5}$$

The current control is implemented with a simple Proportional-Integral (PI) current regulator whose transfer function is

$$G_{c,i}(s) = k_{P,i} + \frac{k_{I,i}}{s} \tag{6}$$

$k_{P,i}$ and $k_{I,i}$ are the proportional and integrative coefficients. Consequently the open loop transfer function can be written as:

$$G_{ol,i}(s) = G_{p,i}(s)G_{d,i}(s)G_{c,i}(s) \tag{7}$$

The PI regulator tuning is performed using the open-loop transfer function of the current loop. A cross-over frequency $\omega_{c,i}$ is chosen and solving the magnitude equation $|G_{ol,i}(jw_{c,i})| = 1$ a 0 dB magnitude crossing is achieved. The integral coefficient k_i is chosen ten times smaller than k_p for stability reasons [16]. The parameters are consequently evaluated through (8):

$$\begin{cases} k_{P,i} \approx w_{c,i} 2L_{cm} \\ k_{I,i} = \dfrac{w_{c,i}}{10} k_{P,i} \end{cases} \tag{8}$$

For the considered system, a crossover frequency of $f_{c,i} = 10kHz$ is chosen.

B. Voltage control loop

The voltage control loop consist of a PI regulator, a feed-forward contribution, a gain-adjustment block and the plant transfer function. The block scheme is presented in Fig. 6. As the DC-DC stage input power is known accurately, i_{load} is estimated and fed forward in the control routine. Indeed, the plant transfer function of the studied control loop routine can

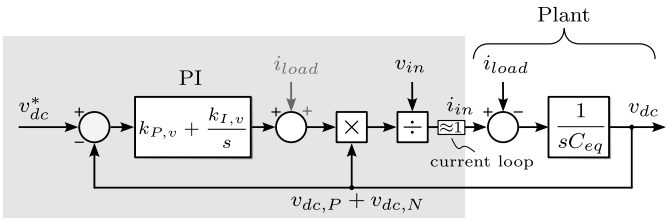


Fig. 6. Voltage loop control block scheme

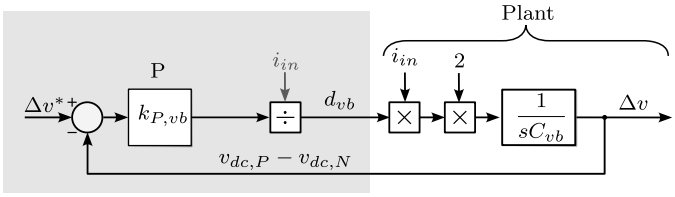


Fig. 7. Detailed block diagram of the voltage balancing control loop.

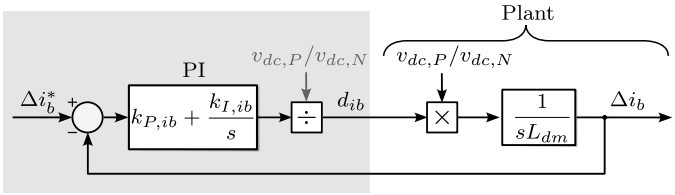


Fig. 8. Detailed block diagram of the current balancing control loop.

be evaluated through equation presented in (2) from the small signal model shown in Fig. 4(a) as:

$$G_{p,v} = \frac{v_{dc}(s)}{i_h(s)} = \frac{1}{sC_{eq}} \tag{9}$$

The controller transfer function is

$$G_{c,v}(s) = k_{P,v} + \frac{k_{I,v}}{s} \tag{10}$$

where $k_{P,v}$ and $k_{I,v}$ are the proportional and integral coefficients of the regulator.

Since the current inner loop has a much faster dynamics, in this analysis it can be considered as ideal (i.e. unitary gain block). As a result, the transfer function of the system become:

$$G_{ol,v}(s) = G_{p,v}(s)G_{c,v}(s) \tag{11}$$

A PI controller is adopted and tuned as has been described in the previous section:

$$\begin{cases} k_{P,v} \approx w_{c,v}C_{eq} \\ k_{I,v} = \dfrac{w_{c,v}}{10}K_{P,v} \end{cases} \tag{12}$$

C. Voltage capacitor balancing

Multilevel converter are characterized by a split DC-Link. Due to the known variability of capacitance values related to specific working conditions [17], an additional voltage control loop is implemented in order to balance capacitors in the upper and lower side. This control routine is achieved by performing a zero steady state differential voltage balance, presented in Fig. 7. A proportional stage regulator is evaluated from (2) as:

$$k_{P,vb} = w_{c,vb}C_{vb} \tag{13}$$

where

$$C_{vb} = \frac{C_P + C_N}{2} \tag{14}$$

Later on the evaluated duty contribution is respectively added and subtracted to the upper and lower sides as an additive contribution to the current control output, as shown in Fig. 3. In order to avoid interference between control bandwidth, a crossover frequency of $f_{c,vb} = 50Hz$ is chosen.

D. Differential current balancing

Current unbalance between parallel legs in power converters with interleaving can lead to significant problems [18], such as different thermal stress over components, undesired phase voltage difference and increased losses due to an unbalanced load seen by discrete devices can lead to undesired results in the overall power management. Consequently, two equal control loops are implemented to avoid this imbalance between parallel legs on the upper and lower sides of the converter. Fig. 8 presents the block scheme of the control loop. A PI-regulated control is implemented, and the parameters are tuned according to the small signal model presented in Fig. 4 and the equations (2):

$$\begin{cases} k_{P,ib} \approx w_{c,ib}L_{dm} \\ k_{I,ib} = \dfrac{w_{c,ib}}{10}k_{P,ib} \end{cases} \tag{15}$$

III. Control Implementation

An interleaving with 90° degrees of phase-shift is adopted for the four DC-DC converter legs. Two modulation types can be defined depending on the switching order [9]. For this study, an N-type modulation is implemented as it results in a better efficiency of the converter, an increased capacitor life, and a reduced EMI noise [5].

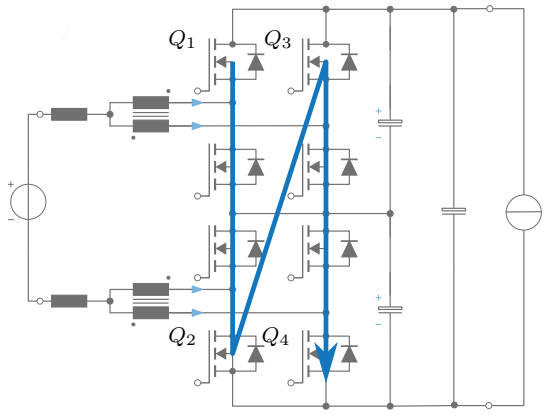


Fig. 9. N-type switch order modulation

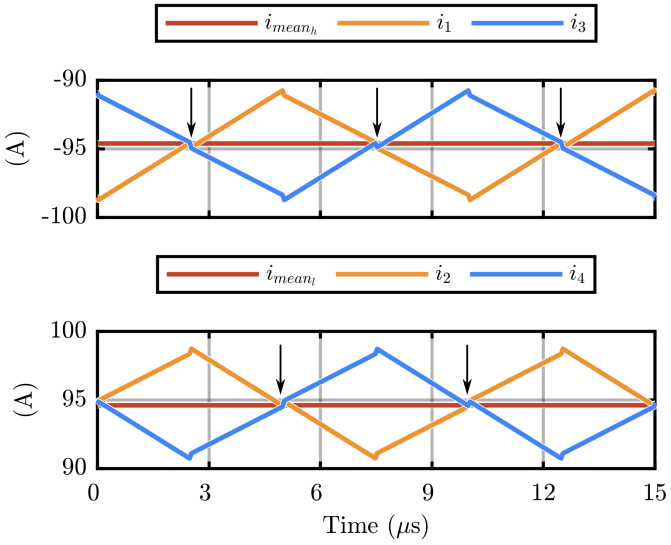


Fig. 10. Current sampling detail for the differential currents of the high side and low side of the converter.

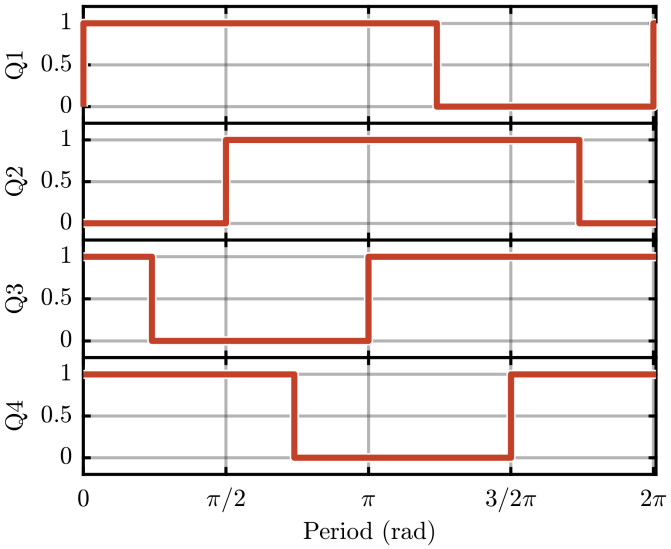


Fig. 11. Order command series over one switching period

Fig. 9 a presents the switching order of the transistor legs over a switching period. As a consequence, the current sampling instant should be different for each current.

Fig. 10 presents this aspect. The arrows indicates the correct sampling instant to evaluate the currents i_1, i_2, i_3, i_4.

The four duty cycles are compared with four different carrier phase-shifted between each other of 90° to generate the desired modulation, shown in Fig. 12. The trigger of the acquisition is synchronized with the triangular carriers, and each physical quantity is related to a specific carrier. Furthermore, the update of the compare register of the PWM modulator must be done in a specific instant, different for each switching pole. A good solution for synchronizing all needed processes is to define a primary timer n_{main}, whose timer period is set according

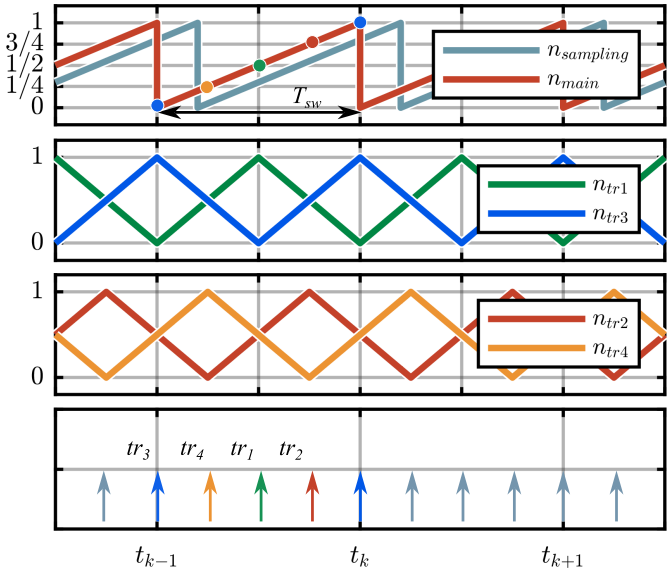


Fig. 12. Top: Main counter and shifted counter. Middle: Carrier phase-shifted of 90°. Bottom: Triggers used for synchronization of the triangular carriers at specific percentage of the main counter saw-tooth.

TABLE I
GAN CONVERTER PARAMETERS.

DC-Link	V_{in}	200	V
Max Output Voltage	$\hat{V}_{dc}$	300	V
Max Input Current	$\hat{I}$	25	A
Switching frequency	f_{sw}	100	kHz
DC-Link	C_{eq}	4.30	μF

to the desired switching frequency. Furthermore, sampling instants must be synchronized with the PWM carrier peaks, as shown in Fig. 12. To compensate the delay introduced by the analog sensors and the analog conditioning circuitry, a new counter $n_{sampling}$ is employed with a specific lag. Triggers for A/D converters are determined by specific $n_{sampling}$ values, allowing for two samples per feedback quantity per PWM period. Furthermore, the ISR for DC-DC control must synchronize with the PWM period, requiring termination before a new ISR to ensure the availability of the latest sampled data at T_{sw}.

IV. EXPERIMENTAL RESULTS

The dynamical and steady-state performances of the proposed control strategy are verified experimentally on a rescaled setup proposed in Fig.13, according to the parameters presented in Table I. Two half-bridge modules from Texas instruments LMG3526R030 GaN are assembled to achieve a multilevel DC-DC converter. The nominal on-state resistance is 30mΩ at 25°C, with an operating maximum voltage of 520 V V_{dc}. Due to the absence of parallel legs and interleaving inductors, the current balancing loop could not be tested.

Indeed, the proposed setup aims to verify the effectiveness of the control loop routine of the main external voltage loop, current loop and the voltage capacitor balancing loop. The following tests have been performed:

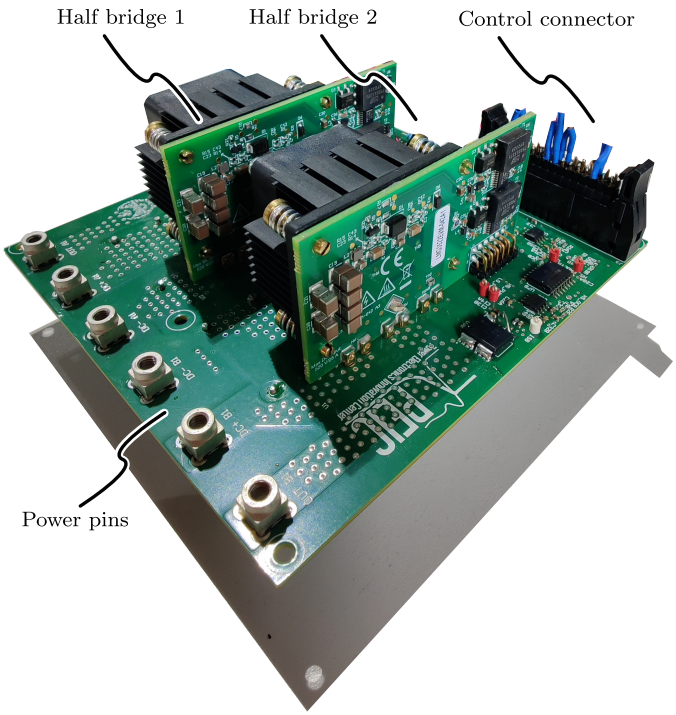


Fig. 13. DC-DC converter setup.

1) Test 1: step voltage variation.
   Closed-loop control systems with both voltage and current regulation are typically tested with a voltage step to evaluate the system's dynamic response. This approach allows for the assessment of how the system reacts to a sudden and significant change in the reference voltage, providing critical insights into the stability and effectiveness of the control. Fig. 14 presents a voltage step response test. As can be noticed, the two voltages across the capacitor remain balanced.
2) Test 2: load transient.
   A load is injected to test the current control loop and ensure that the system does not lose control. This method involves applying a load change and monitoring the system's ability to maintain current regulation despite the disturbance. It verifies the robustness of the current control loop by checking if it can effectively handle the added load without compromising stability or performance.
   Fig. 16 presents an induced load variation through an electrical load.

V. Conclusions

In this paper, the implementation and effectiveness of digital control for a high-power multilevel interleaved GaN DC-DC converter, specifically designed for fuel cell traction applications, have been explored.

The experimental results confirm the viability of the proposed control scheme in achieving the desired voltage and current regulation, while also maintaining balanced capaci-

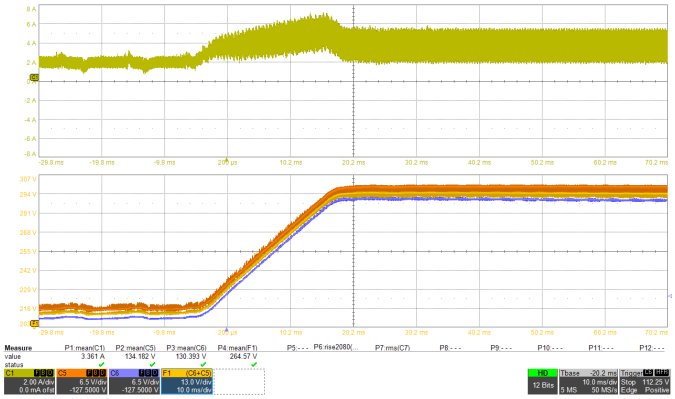


Fig. 14. Experimental results of a step voltage response with $V_{in} = 200V$ and $V_{dc} = 300V$. C1 is the current on the input side, C5 and C6 are, respectively, the voltages across the high side and low side of the DC-Link (C_P and C_N), and F1 is the output voltage, obtained as a sum of C5 and C6.

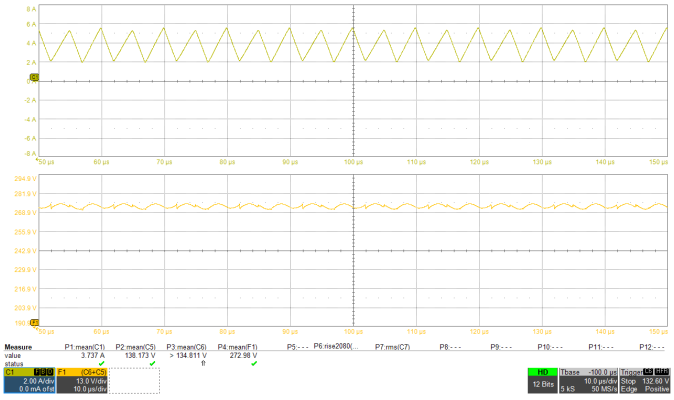


Fig. 15. Experimental results of a steady state operation with $V_{in} = 200V$, $V_{dc} = 270$V and $P_{out} = 800$W. C1 is the current on the input side, F1 is the output voltage, obtained as a sum of C5 and C6, the high side and low side capacitor voltages.

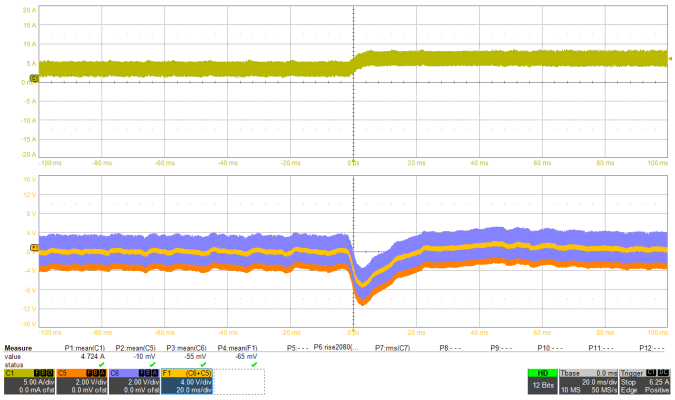


Fig. 16. Experimental results of a step current load injection with $V_{in} = 200V$ and $V_{dc} = 300V$. C1 is the current on the input side, C5 and C6 are, respectively, the AC coupled voltages across the high side and low side of the DC-Link (C_P and C_N), and F1 is the AC coupled output voltage, obtained as a sum of C5 and C6.

tor voltages and avoiding inductor saturation. Moreover, the digital control approach outlined in this study addresses the challenges associated with high switching frequencies and the synchronization of multiple interleaved switching cells. The proposed methodology offers a robust solution for controlling complex power converter systems, ensuring high efficiency and reliability in fuel cell traction applications.

The contributions of this research highlight the potential of advanced digital control techniques and GaN technology in pushing the boundaries of power density and efficiency for future fuel cell-powered electric vehicles. Further investigations will explore the scalability of the proposed system and its application to other high-power conversion scenarios.

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