Design of a 75kW Three-Level DC/DC GaN Converter for Automotive Fuel-cell Application

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***Abstract*—Nowadays, fuel cells represent a promising alternative to replace battery packs for electric vehicles where weight is a concern or where electrical charging is not possible. With respect to a battery pack, built up to 800V, the output voltage of fuel cell stacks is rather low (typically below 200V) and also it is strongly dependent on the load current. Therefore, the integration of a fuel cell in an electrical powertrain needs a DC-DC converter that must exhibit high efficiency and power density. Therefore, this paper presents the design and optimization of a 75 kW, multi-level DC-DC converter leveraging the benefits of the gallium-nitride (GaN) power devices and on the ceramic technology for the capacitors. The paper presents results regarding the GaN device selection with loss analysis, the DC link capacitor sizing and the design of magnetic components. The estimated power density of the converter is 41.7kW/L with a 99.1% overall maximum efficiency.**



***Index Terms*—GaN HEMTs, DC/DC converter, Automotive, Fuel-cell, Multilevel.**


## I. INTRODUCTION

Nowadays, fuel cells are receiving significant interest for automotive industry. They are considered a valid replacement of bulky and heavy battery packs in electrical powertrains serving trucks, buses, or commercial vehicles. Fuel cells (FC) are characterized by a low voltage output (up to few hundred volts) with a large variation depending on the load current, as well as slow dynamic response [1]. This variability in output voltage and slow response time pose significant challenges for their integration into automotive electrical systems, necessitating sophisticated power management solutions. Therefore, a boost DC/DC converter is usually employed as an electronic interface between the FC and the traction inverter, as shown in Fig.1. These converters play a crucial role in stabilizing the voltage output and managing the power flow from the fuel cell to the vehicle's traction inverter. The incorporation of energy storage elements for peak shaving is particularly important in mitigating the slow dynamic response of fuel cells, ensuring that sudden power demands can be met efficiently [2]. Most

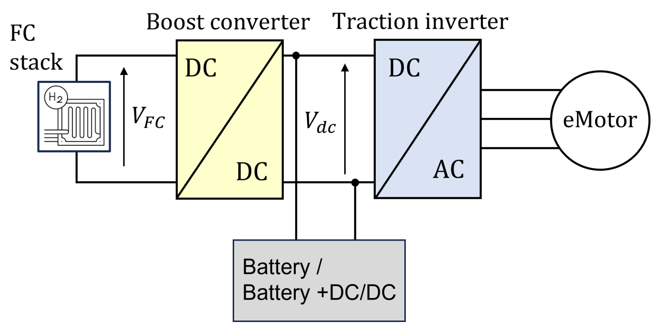



Fig. 1: FC powered electrical powertrain.

recent DC/DC converters are using SiC technology [3], and the reported overall converter power density is lower than 15kW/L. While Silicon Carbide (SiC) devices have shown promising results in terms of efficiency and thermal management, there is still room for improvement in power density, which is a critical factor in automotive applications where space and weight constraints are significant. The Gallium Nitride (GaN) devices represent an interesting solution for the DC-DC converter, as their switching frequency is superior to the one of the SiC counterparts, allowing an important reduction of the size of reactive elements to increase of the power density. GaN technology offers several advantages over SiC, including higher electron mobility and lower on-resistance, which translate to faster switching speeds and potentially higher efficiency. These characteristics make GaN particularly attractive for high-frequency applications, where the size of passive components can be significantly reduced. However, the the majority of the high-voltage commercially available GaN devices have limited breakdown voltage (650V). Therefore, a multilevel topology is needed to satisfy the trend of increasing the dc-link voltage in automotive applications (typically 800V) [4]. Multilevel topologies offer advantages in terms of reduced

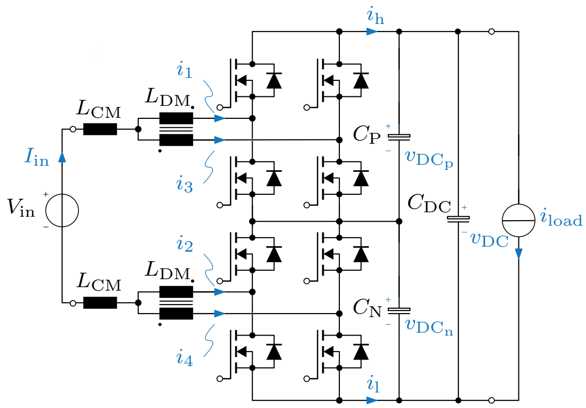



Fig. 2: Considered DC-DC converter structure.

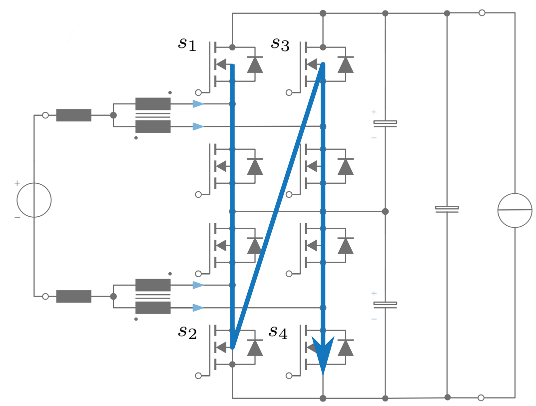



Fig. 3: N-type modulation technique.

voltage stress on individual components and improved output waveform quality, which can be particularly beneficial in high-voltage applications. Moreover, the GaN devices currently available in the market are characterized by relatively low current rating. This limitation presents a challenge for high-power applications typical in automotive traction systems. Therefore, to satisfy the power demand required by the typical automotive traction applications (>50kW) multiple devices in parallel or legs in interleaved configuration are needed. Interleaving techniques not only address the current handling limitations of individual GaN devices but also offer benefits such as reduced input and output ripple, improved thermal management, and enhanced overall system reliability through redundancy.

This paper proposes the design of a three-level, interleaved boost DC/DC converter (Fig.2) using 650V rated GaN high electron mobility transistors (HEMTs) for fuel-cell supplied automotive powertrains. The proposed design aims to leverage the advantages of GaN technology, multilevel topology, and interleaving techniques to achieve a high-performance power conversion solution that meets the demanding requirements of modern automotive electrical systems. The focus will be on optimizing power density, efficiency, and reliability while addressing the unique challenges posed by fuel cell power sources in vehicular applications.

This paper is organized as follows: In Section II is described the operating principle of the proposed DC/DC converter topology. In Section III the converter optimization and design is proposed and its performance are evaluated, all the results are obtained in simulation environment. In the end, Section IV conclude and summarize the work.

## II. Operating Principle

The converter electrical schematic is reported in Fig.2. It consists of two sets of 2-level full-bridge legs connected in series named upper and bottom respectively. To ensure a very low DC current ripple from the fuel cell the DC/DC converter uses for each input rail a coupled inductor $L_{\rm DM}$, to limit the differential mode (DM) components between the interleaved legs of each full-bridge, in series with an inductor $L_{\rm DM}$ for the common mode (CM) components. The dc-link consists of two types of capacitors, one connected to positive and negative rails $C_{\rm DC}$, to create a path for the DM high frequency current ripple components, and the other connected to each full-bridge output $C_{\rm P|N}$ for both DM and CM components, withstanding half the full dc-link voltage.

The converter is operated with an N-type interleaving method control (Fig.3) due to an higher overall converter efficiency, lower EMI noise emission and increased capacitor life [5]. As reported in Fig.4, the leg carriers and signals are phase shifted by 90° between each other. To better understand the converter operation, in Fig.5 and Fig.6 are reported the converter equivalent circuits and the waveforms corresponding to duty cycle $d$ = 0.4. The DM voltage $v_{\rm DM}$ moving average component is null and its high ripple is characterized by three level (+$V_{\rm DC}$/2, 0, -$V_{\rm DC}$/2) and a frequency equal to the switching one. Instead, the CM voltage $v_{\rm CM}$ moving average is different from zero and it is responsible of the converter power transfer, the high frequency ripple component is at two times the switching one due to the frequency doubling effect of the interleaved operation of the two legs shifted by 180° (upper or bottom). Similar considerations can be extend to the CM and DM current components (Fig.6(b)), except for the higher frequency doubling effect related to contribution of the interleaved operation of the four legs (shifted by 90°). This leads to a frequency ripple which is four times higher the switching frequency for the $i_{\rm CM}$ component and two times higher for the $i_{\rm DM}$ one. More details about the converter operation are more deeply described in [5], [6], [7] and [8].

## III. Converter Design

### A. Converter Specifications

The main converter specifications are reported in Table I and represent the starting point of the design. The large input voltage range is chosen to cover the entire fuel cell voltage variation. Moreover, the maximum continuous current $I_{\rm in,n}$ is limited to 200A to ensure a safe operation of the fuel-cell and the converter. Therefore, in Fig.7 is reported the DC/DC

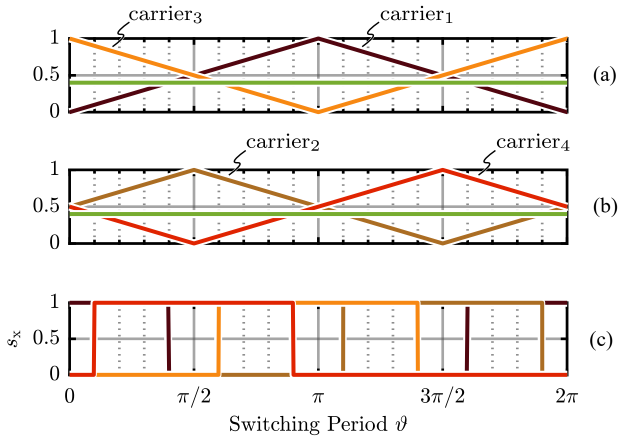



Fig. 4: (a) Leg 1 and 3 carrier waveform, (b) leg 2 and 4 carrier waveforms, (c) high side switch switching signals.

converter operating region for different $V_{\text{in}}$, highlighting the constant current and constant power region.

TABLE I: Converter specifications

| $P_{\text{n}}$ | $f_{\text{sw}}$ | $v_{\text{DC}}$ | $V_{\text{in}}$ | $I_{\text{in,n}}$ |
|---|---|---|---|---|
| 75kW | 100kHz | 800V | 250V-550V | 200A |
| **Power Density** | | **Maximum Efficiency** | | |
| $\geq$ 35kW/l | | $\geq$ 99% | | |

### B. Semiconductor and Heatsink

The majority of the commercially available GaN switches are typically characterized by a large conduction losses temperature dependency, the on-state resistance from 25°C to 150°C could be from 2 to 2.5 times higher dependently on the switch technology [9]. Therefore, for GaN-based converters the heatsink thermal performance drastically impacts on the overall converter efficiency much more than other semiconductor technologies (i.e. IGBT or SiC).

For this application, the selected GaN switch is the Direct Drive V08TC65S2A from VisIC manufacturer due to its excellent conduction and switching performance (Fig.8). It can be noticed from Fig.8(b) that the on-state resistance at 150°C is approximately two times higher the respect to the one at 25°C. To limit the temperature rise and ensuring low conduction losses an oversized heatsink could be selected to achieve low heatsink to fluid thermal resistance $R_{\text{th,h-f}}$. However, for traction application the weight drastically impact on the vehicle's range, therefore, the heatsink oversizing is not feasible. To ensure low switch losses combined with minimal heatsink weight (or volume) an optimization process has to be performed to combine the size and the thermal performance of the heatsink to the semiconductor losses.

The straight fin heatsink geometry is selected and, considering a uniform heat distribution, the $R_{\text{th,h}-\text{f}}$ consists of three main thermal resistance contribution as reported in [10]: fin, conductive, capacitive. The equation (1), provided by [10], is exploited to generate a large number of designs considering a fluid temperature of 65°C and a flow rate of 8l/min as initial specifications. It is also assumed a thermal resistance of the thermal interface material (TIM) $R_{\text{th,c}-\text{h}}$ equal to 0.005°C/W. The semiconductor losses are computed in PLECS environment for each value of $R_{\text{th,h}-\text{f}}$ generated and it is assumed a full-power operation with constant duty cycle equal to 0.5. In Fig.9 is depicted a cross-section of the converter and it is highlighted the switches thermal network. In Fig.10 are shown the simulation results, the best design is selected according to the Pareto optimatily between the semiconductor losses and heatsink weight.

$$R_{\text{th,h}-\text{f}} = R_{\text{th,fin}} + R_{\text{th,cond}} + R_{\text{th,cap}} \tag{1}$$

In Fig.11 and Fig.12 are reported the switches power losses and junction temperatures of the selected optimal design. It can be noticed that the majority of the converter losses are the conduction one and the maximum junction temperature is at full-load quite below the thermal limit. The semiconductor efficiency $\eta_{\text{semi}}$ for different power level and input voltage is shown in Fig.13, it is reported a maximum semiconductor efficiency equal to 99.16%.

### C. Magnetics

Starting from the converter waveforms described in Section II, it is possible to compute the inductors' flux ripple stresses. The CM and DM flux ripple waveforms ($\Delta\lambda_{\text{CM}|\text{DM}}(t)$) are computed by integrating the high frequency CM and DM components over the switching period $T$ according to (2).

$$\Delta\lambda_{\text{CM}|\text{DM}}(t) = \int_0^T v_{\text{CM}|\text{DM,HF}}(t)\, dt \tag{2}$$

In Fig.14 are reported the peak-to-peak flux ripple stresses respectively for different input voltages $V_{\text{in}}$. Is is worth noticing that corresponding to $V_{\text{in}} = 400V$ there is a singular point in which the CM component is zero and the DM is maximum. This means that if the input voltage is ideally constant to 400V the $L_{\text{CM}}$ inductor could be removed thus increasing the converter performance, power density reducing at the same time weight and costs. However, due to the high input voltage variability related to the fuel-cell operation the $L_{\text{CM}}$ and $L_{\text{DM}}$ inductors have to be designed to meet both the current ripple constraint in the worst case peak-to-peak flux ripple conditions.

The CM and DM inductors are selected from a rough optimization algorithm as in [11], [12]. The selected core database consists of both ferrite and powder cores for the DM coupled inductor and only powder cores for the CM one. The winding and core losses are computed according to (3) and (4) respectively [13]. The generated designs are reported in Fig.15 and, similarly to Section III-B, the inductor designs are selected according to the Pareto optimality between the inductor total losses and weight.

$$P_{\text{cond}} = 0.5 \cdot \sum_{\text{k}=1}^{n} R_{\text{ac}}(f_{\text{k}}) \cdot \hat{i}_{\text{L}}^2(f_{\text{k}}) \tag{3}$$

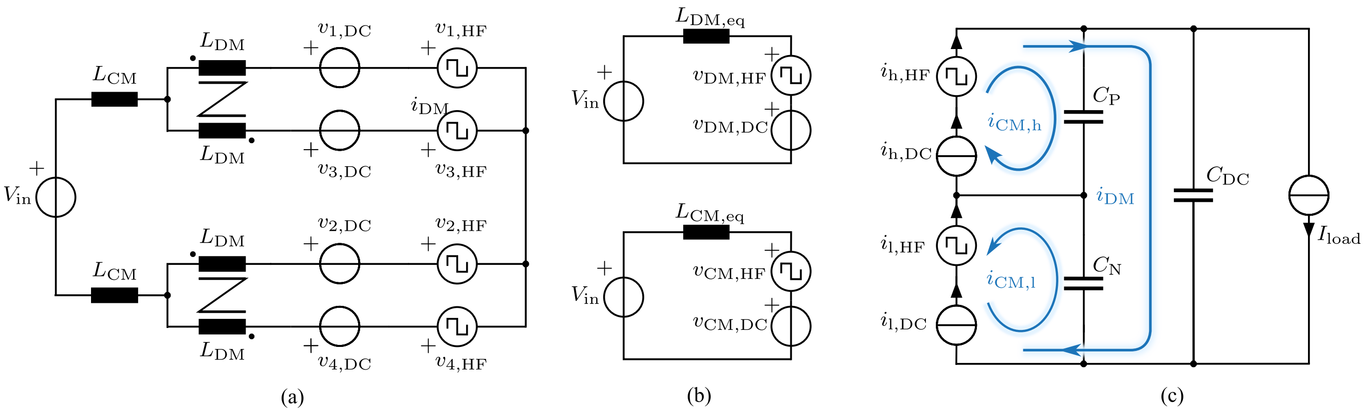



Fig. 5: (a) DC input equivalent model (b) CM and DM DC input equivalent model (c) DC output equivalent model

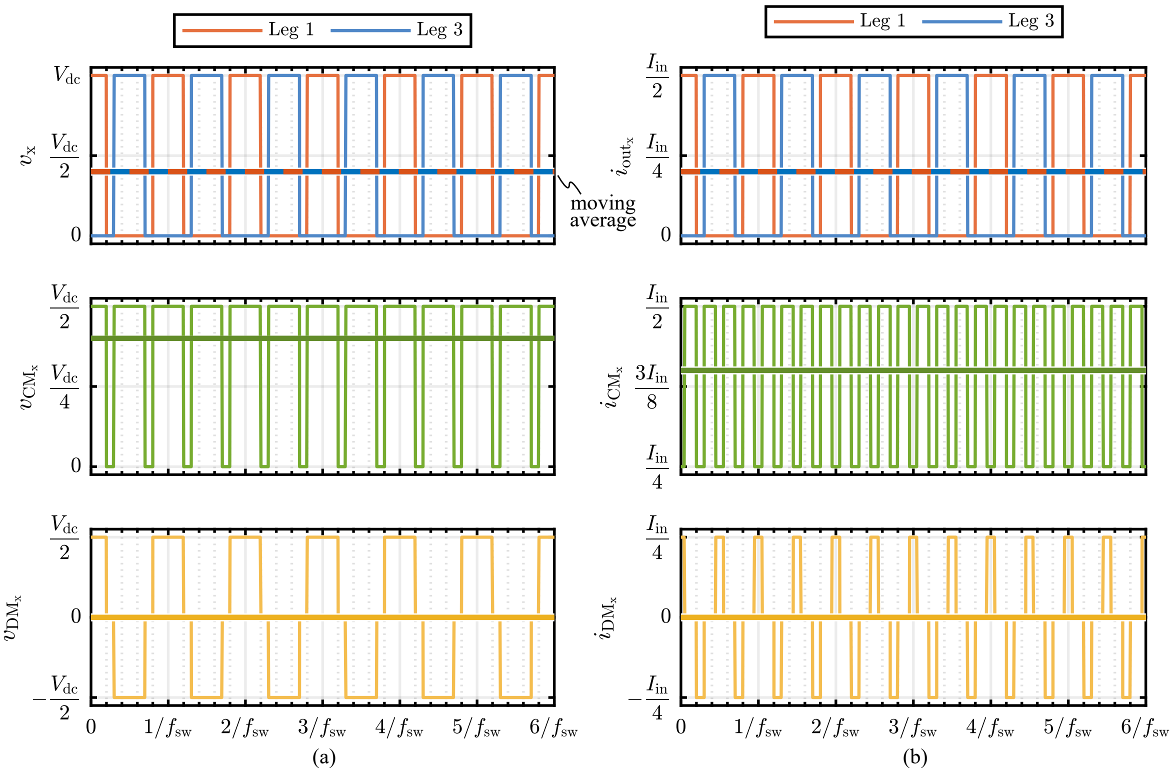



Fig. 6: Converter (a) voltage and (b) current waveforms with $d$ = 0.4.

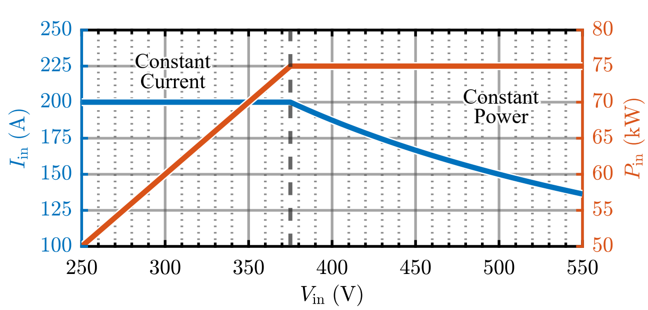



Fig. 7: Converter operating region.

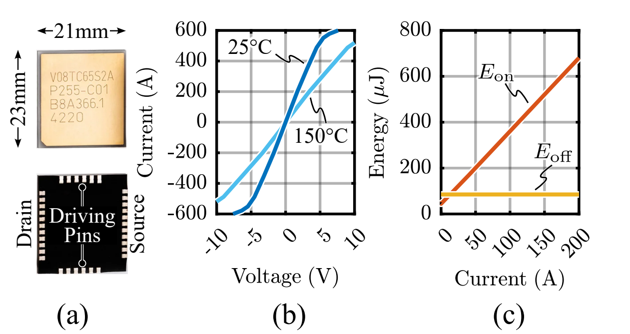



Fig. 8: VisIC V08TC65S2A GaN switch: (a) package and dimensions, (b) conduction characteristics, (c) switching losses.

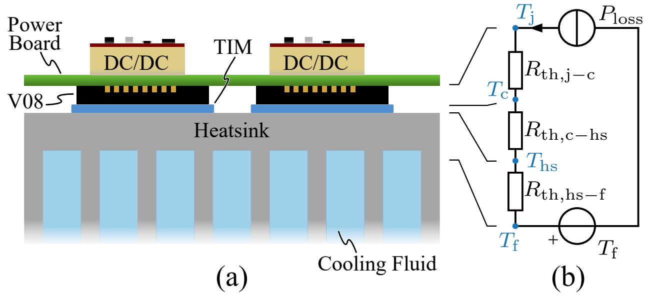



Fig. 9: (a) arrangement of the power devices on the heatsink (b) steady state switch thermal network.

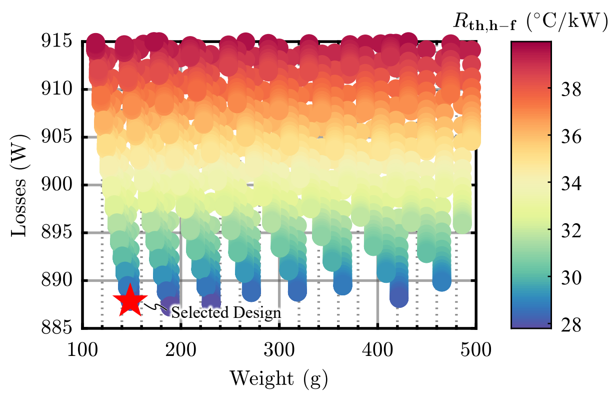



Fig. 10: Semiconductor-heatsink optimization results.

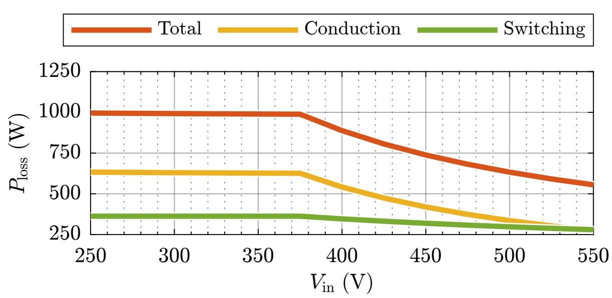



Fig. 11: Semiconductor power losses for different input voltage.

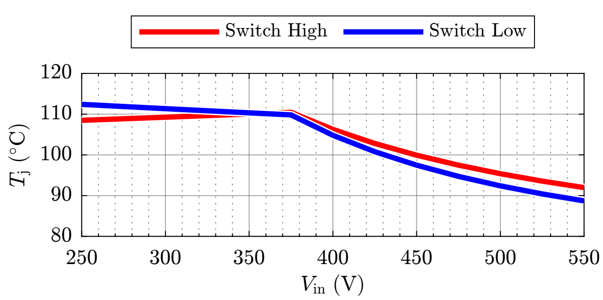



Fig. 12: High and low switch estimated mean junction temperature for different input voltage.

$$
\begin{aligned}
P_{\mathrm{core}} &= \frac{k_{\mathrm{i}}}{T}\int_0^T \left|\frac{dB(t)}{dt}\right|^{\alpha} \Delta B^{\beta-\alpha} dt \\
k_{\mathrm{i}} &= \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}
\end{aligned}
\tag{4}
$$

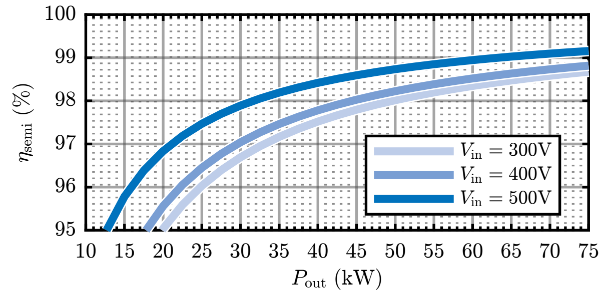



Fig. 13: Computed semiconductor efficiency for different power and input voltage.

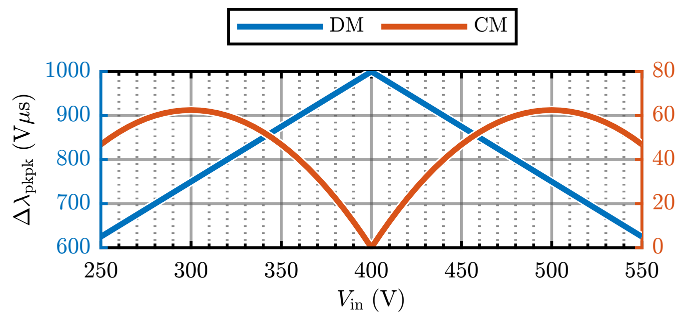



Fig. 14: DM and CM inductors flux ripple.

TABLE II: CM and DM inductor optimal designs.

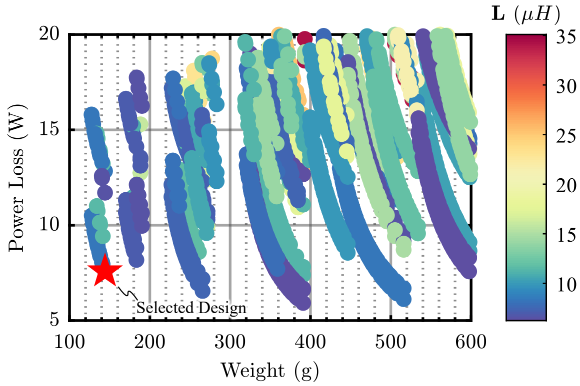
| CM INDUCTOR | | | |
|---|---|---|---|
| ***L*** | **Number of Turns** | $\boldsymbol{P_{\mathrm{loss,tot}}}$ | **Weight** |
| 8.42$\mu$H | 6 | 7.59W | 144g |
| **Core Shape** | **Core Part Number** | **Core Material** | $\boldsymbol{n_{\mathrm{p}}}$ |
| EE | PEH 4328A | High Flux 60 | 1 |
| **Winding Type** | **Winding Material** | $\boldsymbol{w_{\mathrm{Cu}}}$ | $\boldsymbol{h_{\mathrm{Cu}}}$ |
| Rectangular | Copper | 6.5mm | 3.2mm |
| **DM INDUCTOR** | | | |
| ***L*** | **Number of Turns** | $\boldsymbol{P_{\mathrm{loss,tot}}}$ | **Weight** |
| 574$\mu$H | 12 | 5.33W | 155g |
| **Core Shape** | **Core Part Number** | **Core Material** | $\boldsymbol{n_{\mathrm{p}}}$ |
| EE | 58/11/38 | 3F46 | 1 |
| **Winding Type** | **Winding Material** | $\boldsymbol{w_{\mathrm{Cu}}}$ | $\boldsymbol{h_{\mathrm{Cu}}}$ |
| Rectangular | Copper | 10mm | 2mm |

The results of the optimization algorithm are described in Table II as follows: $L$ is the inductance, $n_{\mathrm{p}}$ the number of cores in parallel, $w_{\mathrm{Cu}}$ the wire width and $h_{\mathrm{Cu}}$ the wire height. The selected designs are characterized by a ferrite core for the DM inductor the a powder core for the CM one.

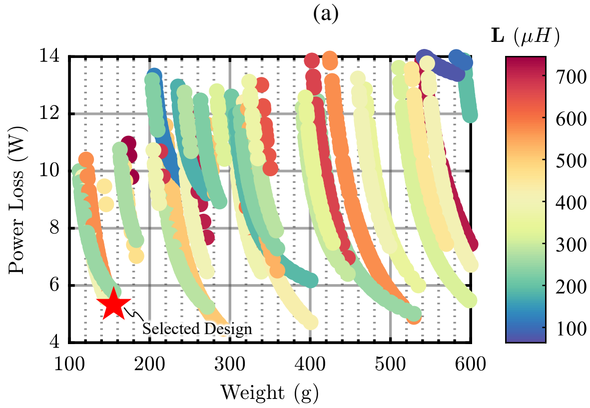
The cross-section of the inductor, the inductance versus current characteristic and the loss sharing are depicted in Fig.16.The big difference in the inductance characteristic between the two inductors is releated to the different core materials, in both cases the winding losses are dominant with respect to the core ones.

### *D. Dc-link*

The total dc-link charge ripple waveform ($\Delta Q_{\mathrm{DC}}(t)$) is computed according to (5) by integrating the high frequency ripple DC current waveform including both the CM and DM




(a)




(b)

Fig. 15: Inductor optimization results:(a) CM (b) DM.

components ($i_{\mathrm{DC,HF}}(t)$), previously shown in Fig.6. The peak-to-peak total charge ripple stress for different input voltage is reported in Fig.17.

$$\Delta Q_{\mathrm{DC}}(t) = \int_0^T i_{\mathrm{DC,HF}}(t)\,dt \tag{5}$$

The dc-link current ripple $i_{\mathrm{DC,HF}}$ harmonic spectrum for a specific operating point is shown in Fig.18. As mentioned in Section II, the current ripple harmonics from the DC link current are divided into two main groups due to the interleaving operation of converter. The first group (called not shared harmonics) are the CM components which independently affect the voltage ripple components in $v_{\mathrm{DC_P}}$ or in $v_{\mathrm{DC_N}}$. The second group (called shared components) are the DM ripple components, these simultaneously affect the voltage ripple components of $v_{\mathrm{DC_P}}$ , $v_{\mathrm{DC_N}}$ and $v_{\mathrm{DC}}$. As shown in Fig.2, the solution adopted for DC link consists of two sets of capacitors (i.e. ,$C_{\mathrm{P}} = C_{\mathrm{N}} = C_{\mathrm{P|N}}$ and $C_{\mathrm{DC}}$). The partition of the shared harmonics depends on the ratio k defined in (6). The charge ripple for the capacitors $C_{\mathrm{P}}$ , $C_{\mathrm{N}}$ and for the capacitor $C_{\mathrm{DC}}$ are provided by (7) and (8), respectively.

$$k = \frac{C_{\mathrm{DC}}}{C_{\mathrm{P|N}}} \tag{6}$$

$$\begin{aligned} Q_{C_{\mathrm{P|N}}}(t) = & \underbrace{\sum_{\mathrm{k=1}}^{n} \hat{Q}_{\mathrm{DC,ns}}(2h)\cdot \sin(\omega_{\mathrm{h}}t+\phi_{\mathrm{h}})}_{\text{Not Shared}} + \\ & + \underbrace{\sum_{\mathrm{k=1}}^{n} \hat{Q}_{\mathrm{DC,s}}(4h)\frac{1}{1+2k}\cdot \sin(\omega_{\mathrm{h}}t+\phi_{\mathrm{h}})}_{\text{Shared}} \end{aligned} \tag{7}$$

$$Q_{C_{\mathrm{DC}}}(t) = \underbrace{\sum_{\mathrm{k=1}}^{n} \hat{Q}_{\mathrm{DC,s}}(4h)\frac{k}{1+2k}\cdot \sin(\omega_{\mathrm{h}}t+\phi_{\mathrm{h}})}_{\text{Shared}} \tag{8}$$

Starting from the overall charge ripple previously computed for different input voltages, the peak-to-peak charge ripples are calculated using (7) and (8), as function of $k$ and $V_{\mathrm{in}}$, the results are reported in Fig.19(a) and Fig.19(b). The $C_{\mathrm{P|N}}$ and $C_{\mathrm{DC}}$ minimum values are then computed for each operating condition considering: $\Delta v_{\mathrm{DC_{P|N}}} = 3\% \cdot v_{\mathrm{DC}}/2$ and $\Delta v_{\mathrm{DC}} = 2\% \cdot v_{\mathrm{DC}}$. The goal is to minimize overall capacitive energy $E_{\mathrm{C}}$ (Fig.19(c)), computed as in (9), as a metric size of the dc-link bank. Therefore, the sharing coefficient $k = 0$ is selected. It is important to highlight that the optimal $k$ is strongly affected by the allowed maximum voltage ripples given as input.

$$E_{\mathrm{C}} = \frac{1}{2}C_{\mathrm{P}}v_{\mathrm{DC_P}}^2 + \frac{1}{2}C_{\mathrm{N}}v_{\mathrm{DC_N}}^2 + \frac{1}{2}C_{\mathrm{DC}}v_{\mathrm{DC}}^2 \tag{9}$$

At this point, according to the imposed voltage ripple constraints the required minimum capacitances are $C_{\mathrm{P|N}} \geq 9.8\mu$F and $C_{\mathrm{DC}} = 0\mu$F. The PLZT ceramic capacitor technology is selected due its excellent performance, in particular: high resonant frequency (MHz), RMS current capability and both gravimetric and volumetric power density and high temperature operation [14]. In particular, the 500V rated FA3 Ceralink® from TDK is selected, in Tab.III are summarized the capacitor main specifications.

TABLE III: CM and DM inductor optimal designs.

| FA3 PLZT Ceramic Capacitor | | | | |
|---|---|---|---|---|
| $\mathbf{V_{rated}}$ | $\boldsymbol{C_{\mathrm{nom}}}$ | $\boldsymbol{f_{\mathrm{res}}}$ | $\boldsymbol{I_{\mathrm{RMS}}}$ **at 85°C** | **ESL** |
| 500V | 3$\mu$F | ≃6MHz | 20A | 3nH |

## E. Converter Performance and Layout

In Fig.20 it is depicted the computed overall converter efficiency considering all the elements previously designed. It is reported a maximum converter efficiency equal to 99.10%, thus meeting the maximum efficiency converter requirement shown in Table I. Besides, in Fig.21 it is shown the 3D rendering of the designed DC/DC converter. The overall volume is 230x200x40 mm, therefore, the volumetric power density is approximately 41.7 kW/l exceeding the minimum power density requirements of 35 kW/l (Table I). The proposed DC-DC converter is currently under prototyping phase.

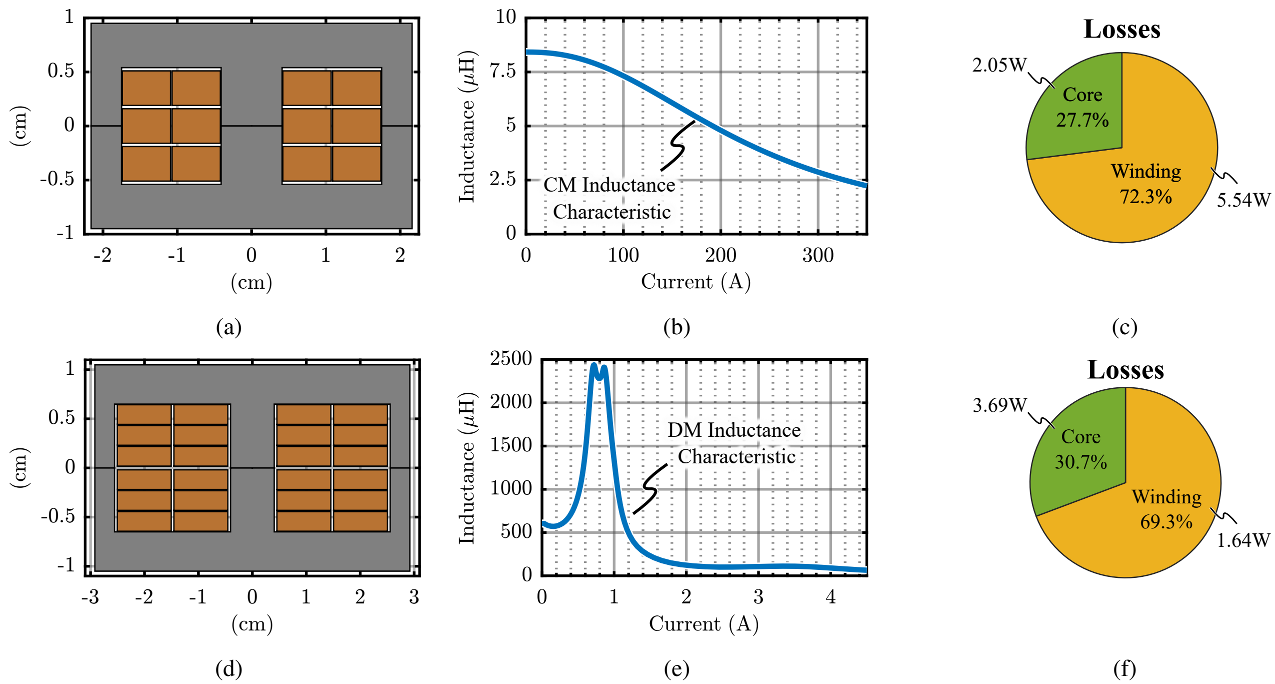



Fig. 16: (a) CM inductor cross-section drawing, (b) CM inductance vs current characteristic, (c) CM inductor losses distribution, (d) DM inductor cross-section drawing, (e) DM inductance vs current characteristic, (f) DM inductor losses distribution.

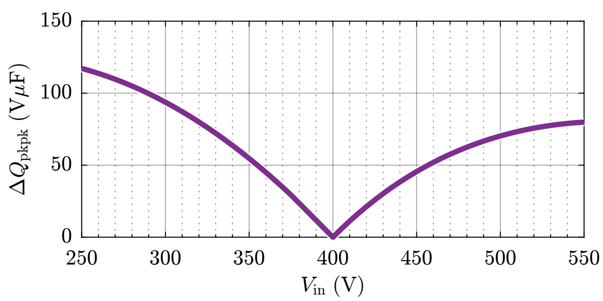



Fig. 17: Overall dc-link capacitor charge ripple.

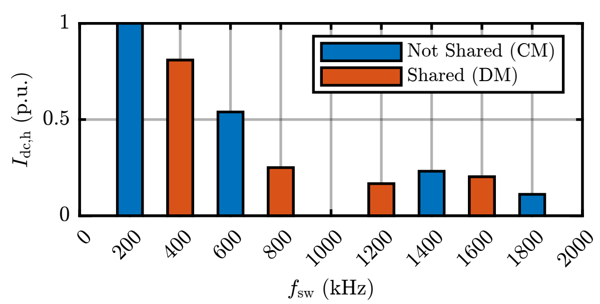


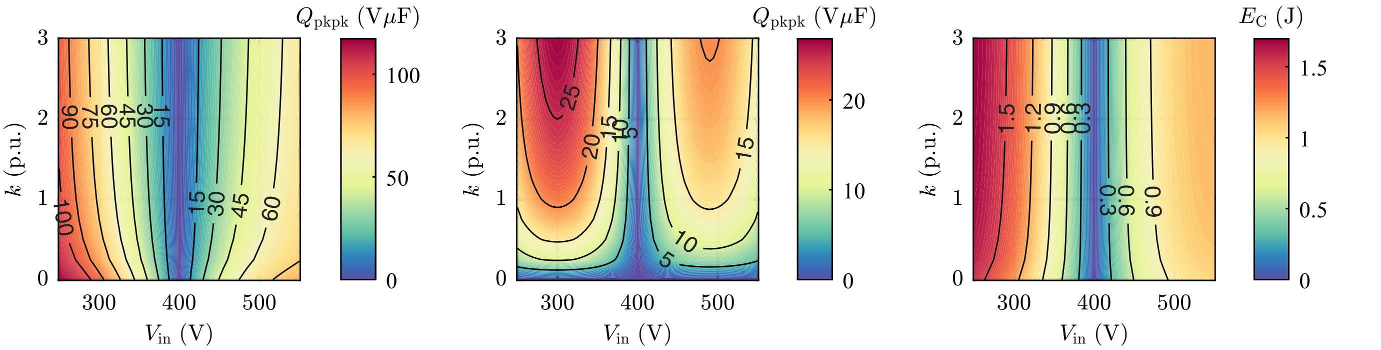

Fig. 18: Fourier harmonic spectrum of the dc-link current in which the CM (not shared) and DM (shared) components are highlighted.

## IV. Conclusions

This paper presents the design and optimization of a 75 kW, multilevel DC/DC converter utilizing GaN technology for fuel cell-powered automotive applications. The proposed converter addresses the challenges posed by fuel cells in electric vehicle powertrains, particularly their low voltage output and variable characteristics. By leveraging the advantages of GaN HEMTs, the converter achieves high efficiency and power density, crucial for automotive applications. The design process involved comprehensive optimization of several key components.

A thorough analysis was conducted to balance the trade-off between semiconductor performance and thermal management. The selected GaN devices, combined with an optimized heatsink design, enable high-frequency operation while maintaining junction temperatures well within safe limits. Both Common Mode (CM) and Differential Mode (DM) inductors were carefully designed and optimized. The DC-link capacitor configuration was optimized to meet stringent voltage ripple requirements while minimizing the overall capacitive energy. Advanced PLZT ceramic capacitors were chosen for their excellent performance characteristics, including high resonant frequency and superior power density. Moreover, a converter layout is proposed, combined with an estimation of the power loop inductance. The estimated power density is 41.7 kW/L representing a significant improvement over conventional designs and meets the stringent space constraints in automotive applications. A semiconductor maximum efficiency higher than 99% combined with a high switching frequency (100kHz) demonstrates the potential of GaN technology in high-power converters.

Future work will focus on the construction of a prototype to validate the simulated results experimentally. Unfortunately, the converter is currently under prototyping and therefore no




(a) (b) (c)

Fig. 19: (a) $C_{\mathrm{P|N}}$ peak-to-peak charge ripple stress map under different $k$ and $V_{\mathrm{in}}$, (b) $C_{\mathrm{DC}}$ peak-to-peak charge ripple stress map under different $k$ and $V_{\mathrm{in}}$, (c) Overall installed capacitive energy of the dc-link bank for different $k$ and $V_{\mathrm{in}}$.

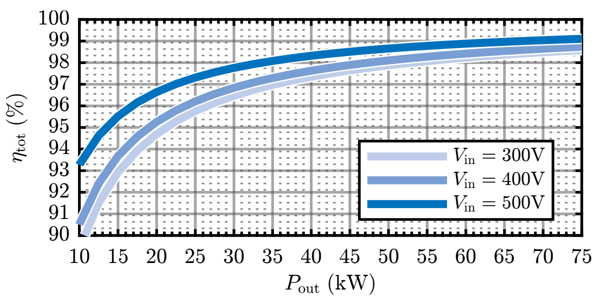



Fig. 20: Estimated overall converter efficiency for different power and input voltage.

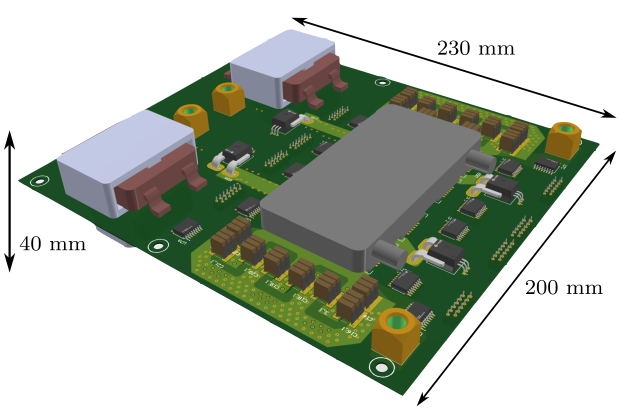



Fig. 21: 3D render of the designed DC/DC converter

experimental results have been available for this work. Additionally, further research into advanced control strategies and EMI mitigation techniques specific to GaN-based converters in automotive environments is anticipated to further enhance the performance and reliability of these systems.

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