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(Article begins on next page)

19 November 2026

Fast Simulator for the Estimation of Inverter DC-link Temperature in e-Drives Subjected to Highly Variable Working Cycles

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***Abstract*—Accurate estimation of losses and operating temperatures is extremely important for the design of traction inverters and its validation for specific operating conditions. Although several methods are already available in the literature to estimate the semiconductor power losses, the power losses and temperature evaluation of inverter DC-link capacitors are less explored. Therefore, this paper presents a fast simulation model of traction eDrive to provide accurate estimation of DC-link loss and temeperature, as well as DC link voltage ripple evaluation. The proposed model is implemented in Simulink and consists of both a loss model based on loss maps and a circuital model to estimate the dc-link voltage ripple. This model is very fast and therefore it is very useful when the eDrive is subject to long and highly variable driving cycles. Moreover, the model accounts for the influence of the main parts of the powertrain and allows a proper verification of the selected DC link capacitor.**

***Index Terms*—traction inverter, dc-link, simulation**

I. Introduction

The assessment of power losses and thermal behavior represents a critical challenge for the design of inverters for electric vehicles that are inherently subjected to the highly variable working cycles. In the literature, available papers deal with the estimation of the losses and junction temperature of traction power modules over a certain load cycle [1], [2]. However, these models do not focus on the DC-link capacitors that have to be included in a complex simulation model that includes the influence of the main part of the traction system. As a fundamental element of traction inverters, the DC-link capacitor bank typically represents a significant portion of the converter physical volume and mass [3]. Current state-of-art design practices [4] typically size the DC-link based on peak stress conditions (maximum current ripple scenarios), inevitably resulting in conservative oversizing of the capacitor bank for applications with highly variable working cycles. Although this conventional methodology, which is widely used in industrial applications where the load is quite constant, ensures operational safety margins, it leads to suboptimal resource utilization and larger component costs. Prior to prototype validation, designers require sophisticated simulation tools to evaluate the performance boundaries of proposed DC-link design. Various analytical frameworks for evaluating capacitor thermal cycling under predetermined operational profiles [5]–[8]. However, these investigations predominantly emphasize lifespan prediction rather than the sizing process. The design of the capacitor bank is typically done without considering its integration in the powertrain model and it often fails capturing the dynamic interaction with it. Previous investigations have explored DC-link sizing through mathematical formulations [9]. Although these analytical approaches provide fundamental behavioral aspects of DC-link capacitors, they do not suit well for long and variable load cycles. This research introduces an innovative rapid simulation framework for evaluating DC-link performance within the context of electric traction systems. In contrast to conventional analytical methodologies [9], the proposed approach utilizes pre-computed powertrain loss maps to enhance to reduce the simulation time, while preserving accuracy. Moreover, the simulation architecture incorporates the DC-link model within a more complete powertrain simulation, enabling thorough analysis of subsystem interactions. This framework encompasses both electrical and thermal domains, delivering precise estimation of power dissipation, thermal aspects, and voltage fluctuations under dynamic operating conditions.

The paper is organized as follows. Section I introduces the need of dc-link model to be integrated in the entire powertrain simulation. Section II presents the powertrain simulation framework. Section III presents the proposed DC-link design methodology, with the explanation of the loss map generation algorithm, the thermal parameter extraction procedures and the obtained simulation results.

II. Traction e-Drive Model

The proposed traction model is shown in Fig.1 and it consists of four main blocks: vehicle longitudinal dynamic model, eMotor, energy source and inverter. According to a specific driving cycle that imposes the speed and acceleration, the vehicle model provides to the eMotor the operating electrical torque T_{e} and rotational speed n_{mot}. The motor model provides to the inverter model the phase peak voltage

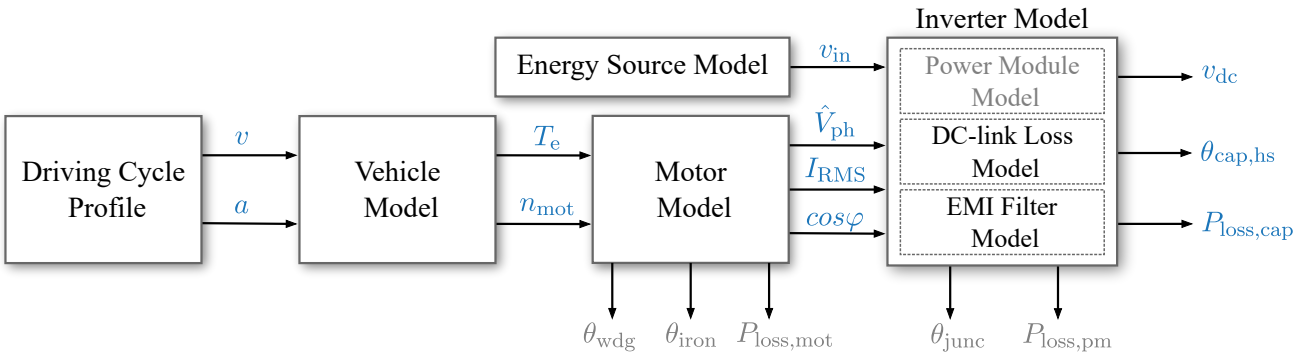


Fig. 1: Full traction e-Drive model.

$\hat{V}_{ph}$, motor RMS current I_{RMS} and power factor $cos\varphi$ to the inverter model. This block also provides the motor power losses $P_{loss,mot}$, the core mean temperature θ_{iron} and the winding mean temperature θ_{wdg} information, however, these variables are not considered in this work since they are not relevant for the DC-link design. The input voltage v_{in} is provides by the energy source model (battery). The three-phase traction inverter model receives as input the information coming from the energy source and motor models to compute the mean DC-link voltage v_{dc}, the hot-spot temperature of the capacitor bank $\theta_{cap,hs}$, the power losses $P_{loss,cap}$, the semiconductor junction temperature θ_{junc} and the semiconductor power losses $P_{loss,pm}$. The inverter model can be divided in three main components: the power module, the DC-link and the EMI filter. For this work, only the DC-link and EMI filter models are considered, while the energy source is modeled for simplicity as a constant voltage source.

In Tab.I are reported the main nominal specification of the selected inverter used in the next sections.

TABLE I
Inverter Main Nominal Specifications

Parameter	Description	Value
S	Apparent Power	150 kVA
I_n	RMS Phase Current	150 A
V_{dc}	DC-link Voltage	400 V
f_{sw}	Switching Frequency	30 kHz

A. Motor Model

The motor model is based on flux maps (current-to-flux linkage relationship) in the rotor (dq) frame, as in (1). These maps can be generated either through Finite Element Analysis (FEA) when the motor design is known, or through experimental measurements [10].

$$\begin{cases} \lambda_d = f(i_d, i_q) \\ \lambda_q = f(i_d, i_q) \end{cases} \quad (1)$$

The flux maps elaboration enables prediction of motor performance computing the motor control trajectories: Maximum Torque per Ampere (MTPA) below base speed and Maximum Torque per Volt (MTPV) for flux-weakening operation. The Maximum Torque per Speed (MTPS) is also computed starting from the flux maps, it represents the best torque production versus speed for a certain DC-link voltage and inverter current limit.

The motor model consists of multiple 2D Look-Up-Tables (LUTs) that take torque and speed as inputs and provide peak voltage and RMS phase current and power factor as outputs, as reported in Fig.2. A key advantage of this approach is its independence from specific torque control methods, as it relies directly on the machine's actual capabilities derived from flux map processing. This feature enables immediate voltage/current requirement determination without complex real-time calculations. For this work, the motor model uses experimentally obtained flux maps of a Brusa HSM1 traction motor.

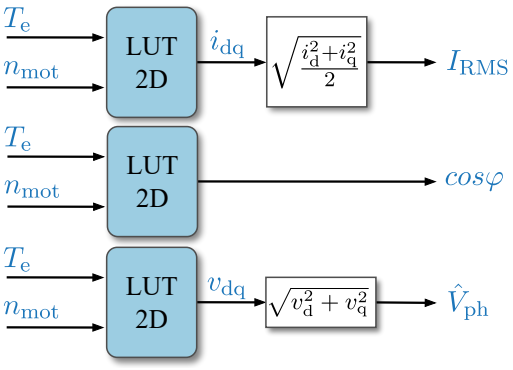


Fig. 2: Motor model main internal blocks.

B. DC-link Model

The DC-link model is part of the inverter block and it consists of two main parts: the loss model and the circuital model. The aim of the loss model block is to estimate the dc-bank losses (Fig.3a) and the hot-spot temperature. The inverter

model is based on a 4-dimensional (4D) loss map taking as input the motor model outputs to compute the losses which are sent to the DC-link thermal model to compute $\theta_{\text{cap,hs}}$, then the estimated hot-spot temperature is sent as feedback to the loss model to adjust the power losses according to the capacitor temperature. In general, this characteristic is related to the capacitor Equivalent Series Resistance (ESR) variation in temperature dependently on the capacitor technology [11]. Moreover, the thermal model also take as input θ_{amb} representing the ambient temperature where the DC-link is located. The modulation index M is computed starting from the DC-link voltage and phase peak voltage quantities.

The DC-link circuital model (Fig.3b) estimates the capacitor voltage variation under variable load conditions. Indeed, due to the limited dynamic response of the energy source [12], [13] and the decoupling behavior (low pass filter) of the EMI stage, the instantaneous load changes are supplied by the DC-link bank leading to a DC-link voltage variation. Therefore, the aim of this block is to check that the DC-link capacitance is sufficiently high to effectively provide the required instantaneous power and that the maximum and minimum voltage limits are not exceeded.

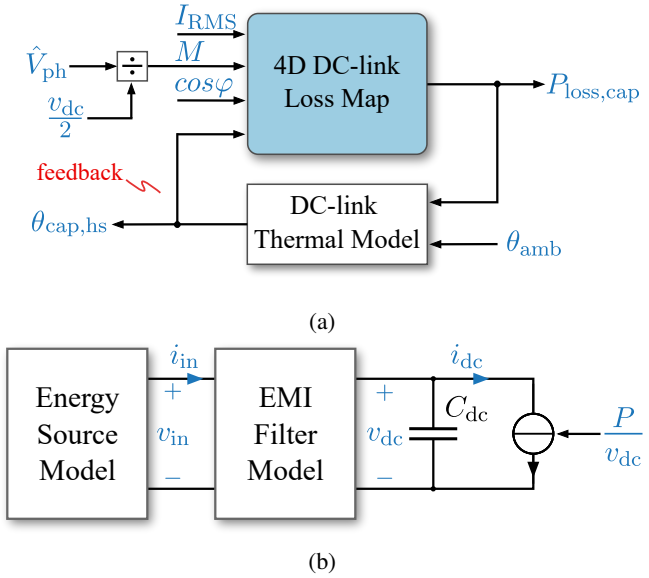


Fig. 3: (a) DC-link full 4D loss map model, (b) simplified circuital model for mean DC-link voltage estimation under variable load.

III. Proposed DC-link Design Methodology

The proposed DC-link design methodology is suitable for highly variable load aiming to highlight the advantages compared to the traditional design approach. For this reason, Table II reportes the main specifications, provided by datasheet, of the C4AQLBW5500M3JK discrete film capacitor [14]. The $V_{\mathbf{dc,n}}$ is the rated DC voltage, C^* is the nominal capacitance, I^*_{RMS} is the maximum continuative RMS current stress at the testing frequency f^*, R^*_{ESR} is the ESR at f^* and R_{th} is the hot-spot to ambient thermal resistance, while θ_{rated} is the nominal continuative operating temperature of the capacitor (Table II).

TABLE II
Selected Capacitor Main Datasheet Specifications

$\mathbf{V_{dc,n}}$	$\mathbf{C^*}$	$\mathbf{I^*_{RMS}}$	$\mathbf{R^*_{ESR}}$	$\mathbf{R_{th}}$	$\theta_{\mathbf{rated}}$	**Material**
500V	50μF	22.8A	2.6mΩ	18°C/W	85°C	PP

A. Traditional Design Approach

Usually, the design of DC-link capacitors must address two critical requirements: managing maximum RMS current stress and controlling peak-to-peak voltage ripple [4]. The RMS current influences power losses and capacitor temperature rise, while voltage ripple affects semiconductor device peak voltage and converter operation quality.

The RMS current flowing into the DC-link capacitor analytically expressed by neglecting the phase output switching ripple [9]. As example, Fig.4a shows the RMS current stress in the DC-link in the $M-\varphi$ plane at nominal load current.

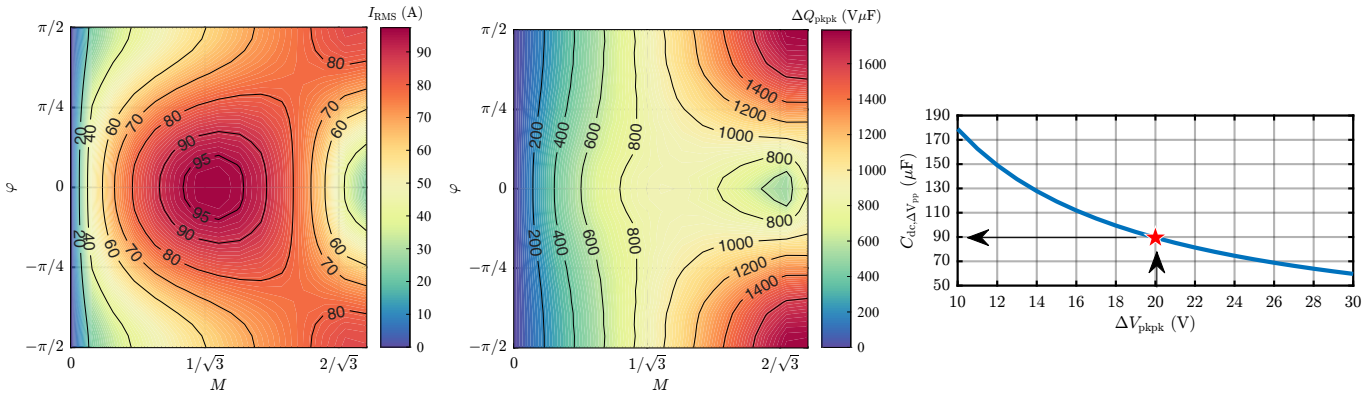
However, the peak-to-peak charge ripple $\Delta Q_{\text{C}_{\text{dc}},\text{pp,max}}$ requires numerical calculation as it is not straightforward to obtain an analytical formulation. The $\Delta Q_{\text{C}_{\text{dc}},\text{pp,max}}$ stress in the $M-\varphi$ plane is reported in Fig.4b. As previously mentioned, the minimum required DC-link capacitance C_{dc} is obtained, calculated by the maximum of two values as reported in (2).

$$C_{\text{min}} = \max[C_{\text{dc},\Delta\text{V}_{\text{pp}}}, C_{\text{dc},\text{I}_{\text{RMS}}}] \tag{2}$$

The voltage ripple-based minimum capacitance ($C_{\text{dc},\Delta\text{V}_{\text{pp}}}$) is calculated in (3) directly from the ratio between the worst case ripple and the maximum allowed peak-to-peak voltage ripple ($\Delta V_{\text{dc,pp,max}}$). In Fig.4c is reported the minimum required capacitance as a function of $\Delta V_{\text{dc,pp,max}}$, assuming as worst case a worst case peak-to-peak voltage ripple equal to the 5% of the nominal DC-link voltage resulting a $C_{\text{dc},\Delta\text{V}_{\text{pp}}}$ of 90μF.

$$C_{\text{dc},\Delta\text{V}_{\text{pp}}} = \frac{\Delta Q_{\text{C}_{\text{dc}},\text{pp,max}}}{\Delta V_{\text{dc,pp,max}}} \tag{3}$$

The current stress-based minimum capacitance $C_{\text{dc},\text{I}_{\text{RMS}}}$ calculation is reported in (6) as the the product of the selected capacitor capacitance and the ration between the total DC-link RMS current stress $I_{\text{C}_{\text{dc}},\text{RMS,max}}$ and the individual capacitor RMS current stress $I_{\text{RMS,cap}}$ considered located all at the switching frequency. This last value is obtained by manipulating (4) and (5) to maintain the same temperature difference ($\Delta\theta$) for the different frequency conditions. The capacitor equivalent series resistance at the switching frequency $R_{\text{ESR}}(f_{\text{sw}}$ is obtained from the ESR vs frequency curve provided by datasheet (Fig.5). Applying (6) it results $C_{\text{dc},\text{I}_{\text{RMS}}} = 233\mu\text{F}$.



(a) (b) (c)

Fig. 4: (a) Peak-to-peak charger ripple map in the M-φ plane, (b) DC-link RMS current map in the M-φ plane, (c) Minimum capacitance vs peak-to-peak voltage ripple.

$$\Delta\theta = P_{\mathrm{loss}} \cdot R_{\mathrm{th}} \tag{4}$$

$$P_{\mathrm{loss}} = R_{\mathrm{ESR}} \cdot I^2_{\mathrm{RMS,cap}} \tag{5}$$

$$C_{\mathrm{dc,I_{RMS}}} = C^* \frac{I_{\mathrm{C_{dc},RMS,max}}}{I^*_{\mathrm{RMS}}} \sqrt{\frac{R_{\mathrm{ESR}}(f_{\mathrm{sw}})}{R^*_{\mathrm{ESR}}(f^*)}} \tag{6}$$

Therefore, to satisfy (2) the number of selected capacitors in parallel n_{p} is equal to 5, resulting an overall installed DC-link capacitance (C_{dc}) of 250μF.

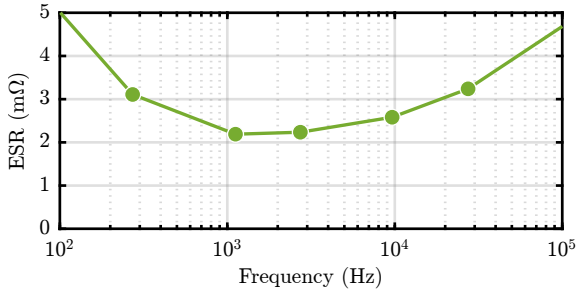


Fig. 5: ESR vs frequency variation of the selected C4AQLBW5500M3JK capacitor.

B. Proposed Design for Highly Variables Working Cycles

The previously presented traditional design approach consists of meeting both the voltage ripple and the thermal current constraints, considering a continuative RMS current stress on the DC-link at nominal load. However, if we take into account only the rated RMS current stress for highly variable working cycles, DC-link oversize will result due to the limited current capability of the capacitors.

The proposed DC-link design methodology takes as a starting point the minimum capacitance value to meet the peak-to-peak voltage ripple limit 3) and then checks the capacitor thermal constraint ($\theta_{\mathrm{cap,hs}} < \theta_{\mathrm{rated}}$), considering a realistic working cycle and taking into account the influence of the main part of the powertrain. If the thermal limit is not met, it is possible to add just the extra amount of capacitor in parallel to ensure a safe DC-link operation.

Therefore, to just satisfy the peak-to-peak voltage ripple constraint, only two selected capacitors are required in parallel, obtaining $C_{\mathrm{dc}} = 100\mu$F. A comparison between traditional and proposed design methods is provided in Fig. 6 for weight, volume, cost and losses, assuming the same thermal limits over the working cycle. It is possible to notice that there is a large decrease of the weight, volume and cost at the expense of higher losses. In any case, it is mandatory to ensure that these losses do not exceed over the working cycle the capacitor thermal limit.

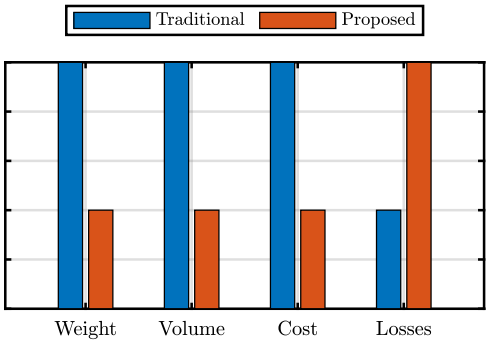


Fig. 6: Comparison for DC-link bank weight, volume, cost and power losses between the traditional and the proposed design approach.

C. DC-link Loss Map Generation

To ensure a fast powertrain simulation, a DC-link loss model based map is implemented, as described in Sec.II-B. The map creation process is described in Fig.7. The first step is to define the input parameters containing the capacitor characteristics and all the operating point which constitute the map. For each operating point, the capacitor DC current i_{dc} is extracted

and the Fast Fourier Transform (FFT) is computed. The FFT current values are used, combined with the ESR vs frequency capacitor characteristic (Fig.5), to compute the power losses according to (7). Then, the power loss value is loaded in the map and a new operating point is selected. This iterative procedure ends when the power losses are computed for all the operating point defined in input.

$$P_{\text{loss}} = \frac{n_{\text{p}}}{2} \sum_{k=1}^{n} R_{\text{ESR}}(f_{\text{k}}, \theta_{\text{cap,hs}}) \left(\frac{\hat{I}_{\text{C}}(f_{\text{k}}, M, cos\varphi)}{n_{\text{p}}} \right)^2 \quad (7)$$

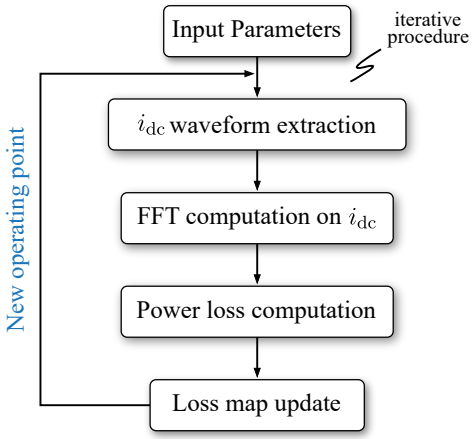


Fig. 7: DC-link map creation algorithm.

D. DC-link Thermal Parameter Estimation

The DC-link thermal model block consists of a first order Cauer network. The equivalent dc-link thermal resistance $R_{\text{th,eq}}$ is obtained in (8) by dividing the single capacitor thermal resistance R_{th} with n_{p}. Then, a corrective factor k_{exc} is applied to take into account the reduced available exchange area A_{exc} compared to the total one A_{tot} due to the thermal interaction between close capacitors ($k_{\text{exc}} = A_{\text{exc}}/A_{\text{tot}} \approx 0.8$). The computed $R_{\text{th,eq}}$ is equal to 10.8°C/W.

$$R_{\text{th,eq}} = \frac{R_{\text{th}}}{n_{\text{p}}} \cdot k_{\text{exc}} \quad (8)$$

The formula to estimate the dc-link equivalent capacitance $C_{\text{th,eq}}$ is reported by (9), considering only the dielectric material of the capacitor. The specific heat capacity (c_{p}) of the dielectric material is assumed equal to 1100 J/(kgK) [15] while the material weight (W_{mat}) is assumed to be as 80% of the total one, resulting in $C_{\text{th,eq}} = 139$ J/kg.

$$C_{\text{th,eq}} = c_{\text{p}} \cdot W_{\text{mat}} \quad (9)$$

E. Simulation Results

The proposed model (Fig .1) has been simulated in Matlab/Simulink for a WLTC driving cycle, as shown in Fig.8. The considered vehicle model has the following data: mass m = 2000 kg, friction model $F_{\text{road}} = a + bv + c\dot{v} + mgsin(\alpha)$, with α = 0°, a = 196.2 N, b = 0 Ns/m, c = 0.536 Ns^2/m^2 , gear ratio τ = 10, gear efficiency η = 94%.

The voltage source model is simply implemented considering a constant voltage source equal to 400V. The EMI filter model consists of an equivalent differential mode inductance $L_{\text{dm}} = 50\mu\text{F}$ and a resistance $R_{\text{dm}} = 20\text{m}\Omega$. The DC-link power loss map consists of 1728 points (12×12×12) and does not depend on the hot-spot DC-link temperature as the selected film capacitor does not have an ESR temperature dependency.

The main simulation results are shown in Fig.9, with focus on the output quantities of the vehicle, motor and DC-link models. It is possible to notice that the capacitance value is sufficiently high to take charge of the instantaneous power oscillation required by the load, generating an acceptable mean dc-link voltage oscillation of few volts (Fig.9f). Moreover, in Fig.9h it is reported the hot-spot temperature pattern over the driving cycle which satisfy the capacitors thermal limit thus confirming the feasibility of the designed DC-link.

The total simulation time is 1.94 s, without including map computation, with a computer equipped with Intel I9 processor. Although the loss map computation is not optimized and it takes approximately 3 minutes, however it is computed once for each DC-link design and can be used for all the next driving cycle simulations.

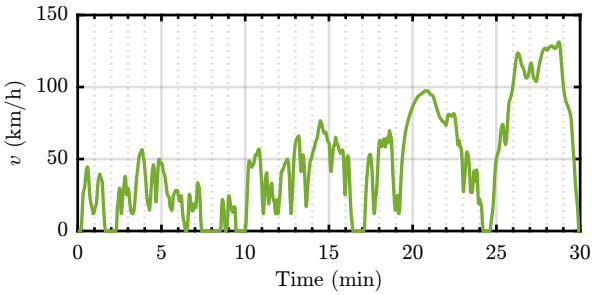


Fig. 8: Selected WLTC driving cycle.

IV. Conclusion

This paper has presented a comprehensive simulation framework for fast evaluation of DC-link performance in electric vehicle applications. The proposed model combines loss mapping and circuital analysis to accurately predict the DC-link behavior under variable operating conditions, while maintaining good computational efficiency.

The novel design methodology is specifically tailored for highly variable working cycles demonstrates substantial improvements over traditional approaches, achieving significant reductions in weight, volume, and cost while ensuring safe thermal operation. The proposed methodology addresses a critical gap in existing DC-link design approaches by providing a practical tool for evaluating capacitor performance within complete powertrain operation. Results from WLTC driving cycle simulations validate both thermal compliance and acceptable voltage ripple characteristics with the optimized design, while achieving simulation times of just 1.94

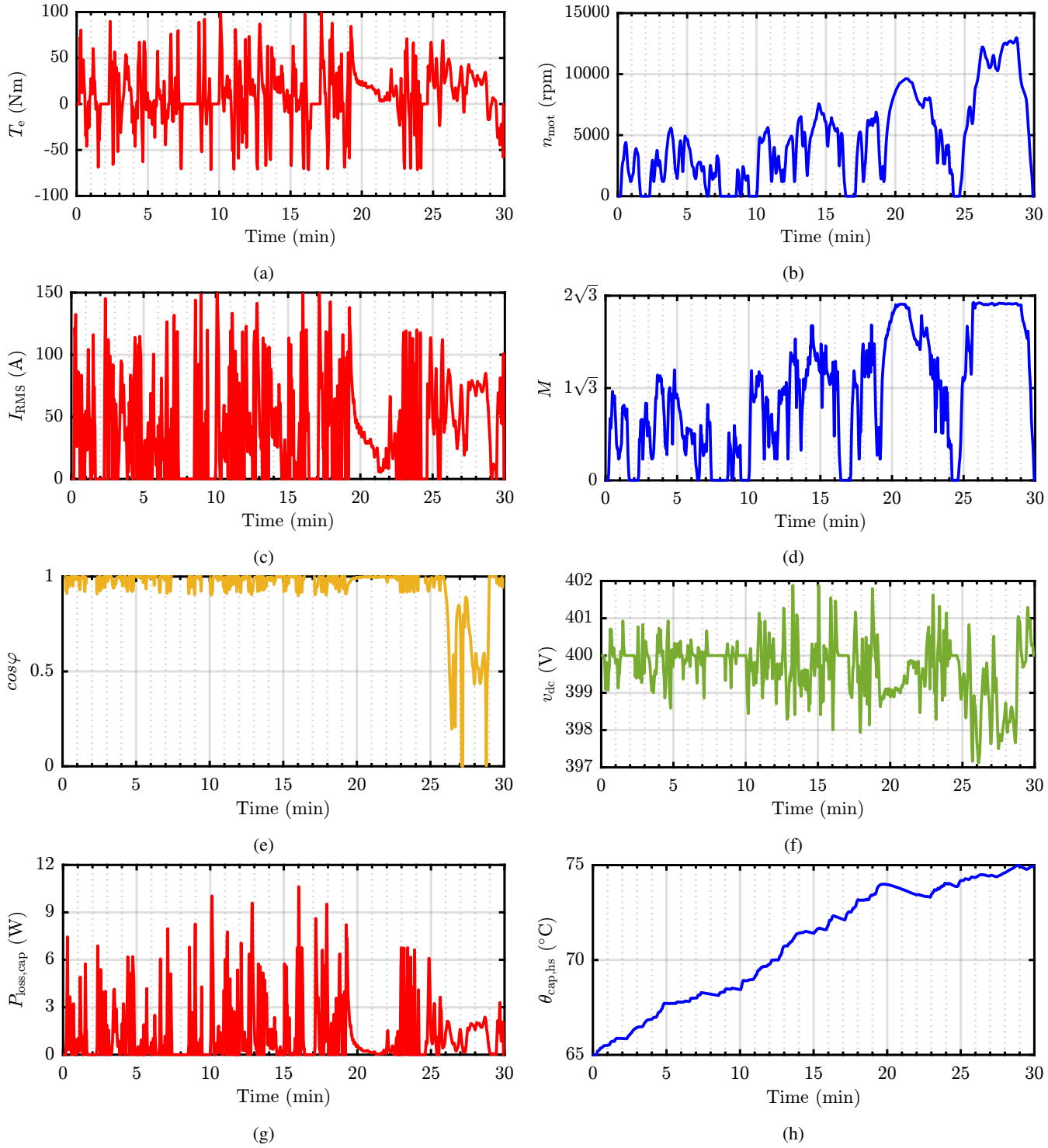


Fig. 9: Driving cycle simulation results: (a) motor electric torque, (b) motor mechanical speed, (c) motor RMS currents, (d) modulation index, (e) power factor, (f) DC-link voltage, (g) DC-link power losses and (h) DC-link hot-spot temperature.

s for complete cycle analysis. Future work will focus on extending the model to include additional capacitor technologies, implementing more sophisticated thermal models, and incorporating reliability prediction capabilities.

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