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ABSTRACT

A middle-contact three terminal architecture could pave the way for cost-effective and high energy yield perovskite/silicon tandem solar cells. However, it poses challenges because of the potential reduction in active area and the need for a highly transparent and conductive middle electrode, and smooth and defect free perovskite films. We present the development of such tandems, focusing on the perovskite composition and the optimization of the interfacial electrode layer in terms of electrical and optical properties and fabrication. The use of overlapping layouts for front and middle contact grids, as customary in microelectronics, is anticipated to conserve the active area.

Keywords: 3T-tandems, middle-contact, multi-scale approach, resistive losses, series-parallel interconnection

1. INTRODUCTION

The demand for higher-efficiency photovoltaic (PV) systems has driven advancements in tandem solar cells, which can surpass the Shockley–Queisser limit of single-junction technologies.[1] Among the possible approaches, perovskite/silicon (PVS) tandems stand out for their high power conversion efficiency (PCE), low-cost, and compatibility with silicon manufacturing processes.[2,3] As far as device architecture is concerned, the three-terminal (3T) PVS configuration is of great interest because it can achieve higher energy yield than two-terminal (2T) tandems, being free from current-matching constraints, and involves less system complexity than four-terminal tandems.[4,5] The simplest and most investigated approach to 3T tandems is to use bottom silicon cells with interdigitated back contacts.[5] On the other hand, the realization of middle-contact 3T tandems is attractive because it allows the exploitation of double-sided contact silicon cells, which are cheaper and more common in mass production.[6]

In this work, we describe the development of middle-contact 3T PVS tandems based on heterojunction silicon solar cells along two main lines of study. The first concerns tuning the perovskite energy band gap for various purposes, from reliability to aesthetics. To this end, devices with perovskite bandgaps ranging from 1.5 to 2.3 eV are discussed. As highlighted in our previous work,[7] 3T tandems with homojunction/Si bottom cells benefit from the highly conductive c-Si base, thereby minimizing lateral resistive losses. In contrast, heterojunction Si-based 3T tandems are more prone to resistive losses due to the thin, less conductive amorphous hydrogenated silicon layers. One approach to address this issue is depositing an intermediate ITO layer of suitable thickness between the perovskite and Si cell. Thus, the second line of the study concerns the development and optimization of the middle-contact ITO layer in terms of electrical and optical properties. Finally, we analyze the impact of series/parallel interconnection strategy for 3T tandem modules. While the independent parallel interconnection of the subcells delivers the highest efficiency, its complexity and cost might hinder scalability. Mixed series/parallel configurations offer a more practical alternative but require tailored strategies to address voltage matching depending on the perovskite bandgap.[8]

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2. DEVICE AND MODELING FRAMEWORK

A schematic drawing of the devices under study with details of the multilayer stack is depicted in Fig.1. The two subcells have reverse orientation (p/n over n/p) and the structure overall resembles that one of a heterostructure bipolar transistor (HBT). The devices under study use Formamidinium (FA)-based perovskite absorbers with bromide (FAPbBr, Eg=2.27 eV, thickness of 270 nm) or iodide halide (FAPbI, Eg=1.51 eV, thickness of 500 nm) and mixed perovskite (CsMAFAPbIBr, Eg=1.6 eV, thickness of 500 nm), hereafter referred to as HBT-Br, HBT-I, and HBT-3C, respectively. The bottom cell consists of a silicon heterojunction solar cell based on a p-type silicon wafer with the top surface passivated by a 20 nm ITO layer[9] (Fig.1.a). The tandem fabrication is developed at low temperature (< 200 °C) and involves the deposition of an additional ITO layer of optimized thickness by DC sputtering, followed by the deposition of the top n-i-p perovskite cell. Subsequently, an etching process is used to remove part of the perovskite layers and make the middle contact, resulting in the layout shown in Fig.1.b.

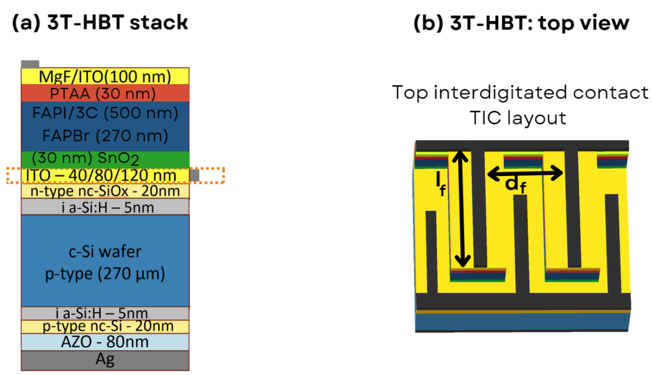

Figure 1. (a) Layer stack of the *intrinsic* 3T-HBT device. (b) Top view of the TIC layout of the 3T-HBT: d_f finger distance, l_f finger length.

Devices were designed by means of a hierarchical multi-scale modeling framework that combines: 3D optical simulations based on mixed Monte Carlo ray tracing and transfer matrix method to deal with surface texturing; quasi-1D drift-diffusion simulations of the structure in Fig.1.a (notice the lateral contact placed at the ITO intermediate layer); circuit-level simulations of the full solar cell, including the current collecting grids shown in Fig.1.b, in order to evaluate optical and electrical loss induced by the ITO intermediate layer (IL) and middle-contact grid.[7] Material models and physics-based simulations were calibrated and validated on the basis of External Quantum Efficiency (EQE) measurements of stand-alone in-house fabricated perovskite and Si sub-cells,[9–11] with the same layer stack as in the tandem design. Experimental data for sputter-deposited ITO layers of various thickness were used to calibrate the optical properties and sheet resistance. For the sake of circuit-level simulations, the current voltage (J-V) characteristics obtained from physics simulations are fitted through an equivalent circuit, which is then completed by lumped parasitic resistances associated to lateral current transport and metal grid layout.[7]

3. RESULTS AND DISCUSSION

We designed a set of devices with different perovskite layers, ITO IL thickness of 40 nm, and fully-textured[12] architecture with maximum *intrinsic* efficiency, i.e. not yet accounting for optical and resistive loss of the metal grids, of 34.5% (HBT-3C), 33.9% (HBT-I), and 31.2% (HBT-Br). Figure 2.a presents an example of EQE for the HBT-3C tandem. The textured surface is instrumental to reduce reflectance, particularly in the Si bottom cell, leading to enhanced near-infrared absorption. As a result, the bottom sub-cell photocurrent increases for both low-gap and high-gap HBT devices, and each HBT configuration surpasses the 2T detailed balance efficiency limit.

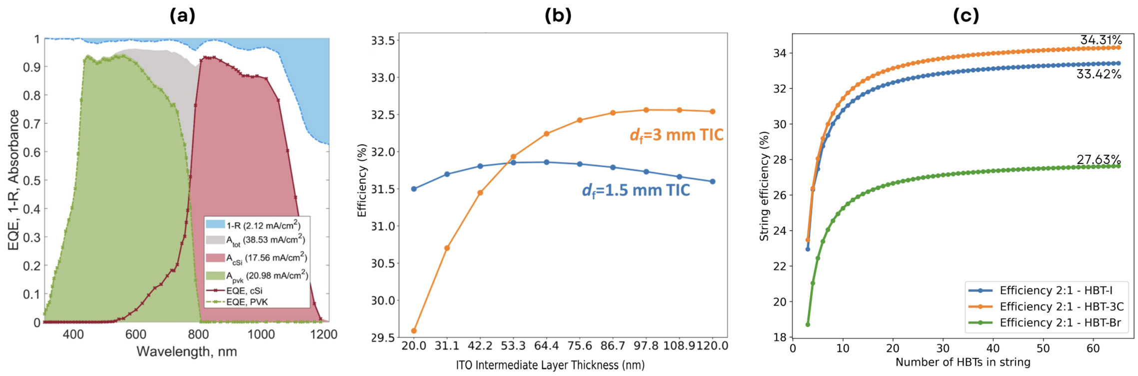

Figure 2. (a) EQE, Absorptance, Reflectance for a fully textured 3T HBT-3C tandem device with ITO IL of 40 nm. (b) Efficiency variation as a function of the ITO IL thickness for two different grid finger spacings (d_f = 1.5 mm and d_f = 3 mm) in a small-area HBT-3C (finger length, l_f=1.5 cm) with top interdigitated contact (TIC) layout. (c) Total efficiency of a series/parallel 2:1 string versus the number of HBT tandems.

The design of the metal grid layout is optimized acting on ITO IL thickness and finger spacing, as shown in Fig.2.b for a small-area tandem. Closely spaced fingers (1.5 mm) have low dependence on ITO IL thickness and the efficiency penalty is dominated by shadow loss. Mitigating these, require wider finger spacings (3 mm) which in turn demand for a thicker ITO IL to minimize resistive loss inherent to lateral current transport across it. An ITO thickness of about 80 nm or larger provides a minimum efficiency loss of about 2%, half of which must be attributed to the short circuit current reduction of the silicon bottom cell due to the increased optical loss. Higher efficiency are within reach by replacing the TIC layout with a one where the emitter and base grids overlap.[7] We anticipate that optimized grid design and ITO IL thickness will enable efficiencies exceeding 30% for areas up to 100 cm^2. Further details will be presented in a future publication.

Finally, we conducted an initial study to evaluate the impact of series/parallel interconnection schemes compared to the ideal case of parallel sub-cell interconnection in 3T tandems (which would require two independent maximum power point trackers). To this aim, at a first instance, we have excluded parasitic resistive effects, therefore the reference efficiency to evaluate the loss induced by the interconnection scheme is the *intrinsic* one. Figure 2.c illustrates how the efficiency scales with the number of connected tandems for a 2:1 series/parallel interconnection scheme (i.e. two silicon subcells connected in parallel to one top cell),[8] which represents the simplest configuration. HBT-3C (V_{mpp}^{PVK}= 1.2 V, V_{mpp}^{Si}= 0.6 V) and HBT-I (V_{mpp}^{PVK}= 1.1 V) demonstrate effective maximum power point voltage match, resulting in an absolute efficiency loss of approximately 1% compared to the parallel interconnection. In contrast, the HBT-Br (V_{mpp}^{PVK}= 1.7 V) faces significant voltage mismatch in the 2:1 configuration, leading to 4% efficiency reduction compared to the parallel interconnection. These losses can be mitigated by adopting alternative interconnection schemes, such as the 3:1 configuration,[8,13] which improves voltage alignment and restores more than 30% efficiency. This highlights the importance of tailoring interconnection schemes to the specific perovskite bandgap to minimize voltage mismatch and efficiency loss.

4. CONCLUSIONS

In this study, we have presented the development of three-terminal tandem solar cells made by integrating a perovskite cell with a double-sided contact heterojunction silicon cell. This architecture allows high efficiency designs for a wide set of perovskite bandgaps. Development and optimization of the middle-contact layer and a preliminary study of interconnection strategies show that this device architecture is promising for combining scalability and high efficiency.

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