Reliability-Constrained Design of a High-Gain Power Optimizer based on a Real Mission Profile

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***Abstract*—This article proposes a methodology for the design of a step-up solar optimizer based on the minimization of the cost-to-output energy ratio and constrained by reliability criteria. Real-world annual mission profiles are used in the optimization, allowing to a more accurate lifetime analysis and output energy estimation. The proposed approach is applied to the case study of an Input-Parallel-Output-Series power optimizer and exploits analytical and empirical loss and cost models for the converter components. The algorithm is implemented in Matlab and is based on the Particle Swarm Optimization (PSO) method, which discards the solutions not meeting the reliability requirements. The optimal solution found by the PSO is then compared with the exhaustive search in the variables space. A converter is designed based on the optimal solution, and its efficiency and accumulated damage are validated by LTSpice and Matlab simulations.**

***Keywords*—Design optimization, Reliability, Power optimizer, Particle Swarm Optimization.**

I. Introduction

Module-level power converters (MLPC), such as microinverters and power optimizers, are becoming widespread solutions to maximize the energy harvesting from small-scale distributed photovoltaic (PV) systems [1]–[3]. The shift from centralized or string configurations to MLPC, however, requires careful design considerations in terms of multiple conflicting objectives such as cost, power density, efficiency and reliability [4]. To assist the off-line design of power converters, deterministic or Artificial Intelligence (AI)-based optimization algorithms have been proposed [5].

Many works focus on the multi-objective optimization of MLPC in terms of weighted efficiency and power density [3], [6], volume [7] or cost [8], [9]. These works do not consider at all the converter reliability in the optimization: this may lead to a late re-design or costly replacements of faulty parts in the field.

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Other works take into account reliability requirements, expressed in terms of the Mean Time Between Failures (MTBF), within the objective function [10]–[12]. This approach, however, has two fundamental limitations: 1) it may result in noncompetitive design solutions from the cost point of view, and 2) it does not model the physical degradation of the converter components due to the repeated thermal stresses. The mission profile-based lifetime consumption (LC) of the power modules was considered in the objective function only in the large-scale PV systems design in [13], however it did not consider the cost implications of a reliability-oriented optimal solution. The inclusion of the mission profile in the optimization approach allows for a more accurate estimation of the converter working points, thermal stresses and expected harvested energy [14].

To overcome the above-mentioned limitations, this article proposes a new design optimization methodology based on the minimization of a modified definition of Levelized Cost of Energy (LCOE) including a mission-profile based lifetime estimation of the converter switches as a constraint. The methodology is applied to the case study of an asymmetric Input-Parallel-Output-Series Power Optimizer (IPOS-PO) [15]. The proposed methodology can be generalized to different converter topologies upon characterization of the electrical stresses of the target converter.

The rest of the article is divided as follows: Section II introduces the converter topology considered as case study of the proposed optimization algorithm, defines the objective function, and describes the modelling and constraints of the methodology; Section III illustrates the Particle Swarm Optimization (PSO) method adopted as search algorithm, presents the impact of different mission profiles on the optimal solutions and the simulation results of a converter designed according to the optimal variable set; finally, conclusions and future work are drawn in Section IV.

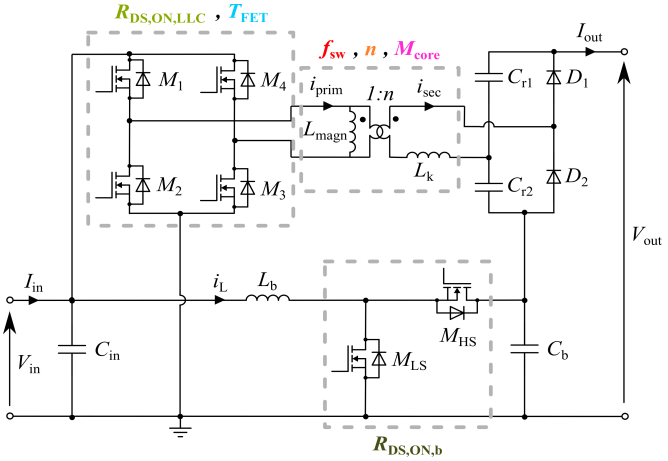


Fig. 1: Schematic of the IPOS-PO converter considered as case study for the optimization.

II. Proposed Optimization Methodology

A. Case study

Before describing the details of the proposed optimization algorithm, the converter topology adopted as case study is introduced. IPOS converters are recently becoming attractive solutions for applications requiring high voltage gains with reduced electrical stresses [16]. In this work, the target converter is the asymmetric IPOS–PO shown in Fig. 1, consisting of a fixed-gain resonant LLC with Voltage Doubler Rectifier and a synchronous boost operating in Boundary Conduction Mode responsible for the Maximum Power Point Tracking (MPPT). In general, for improved performance, the two stages are designed so that the largest fraction of power is processed by the LLC. The detailed description of the converter operation and the derivation of the electrical stresses are out of the scope of this work and can be found in [15]. It is worth noticing that the proposed algorithm optimizes the design of both the conversion stages simultaneously.

In this work, the reduced-order modelling approach [17] has been adopted to identify the minimum size of the solution space, in order to optimize the computational complexity and time. With this approach, the minimum set of variables significantly affecting the converter cost and output energy were identified and are highlighted in Fig. 1:

- for the low-voltage Field-Effect Transistors (FETs) M_{1-4} of the LLC, the conduction resistance $R_{\mathrm{DS,ON,LLC}}$ and technology T_{FET};
- for the LLC transformer, the operating frequency f_{sw}, turns ratio n and core material M_{core};
- for the high-voltage boost MOSFETs, the conduction resistance $R_{\mathrm{DS,ON,b}}$.

It is worth observing that the selected design variables exhibit multiple effects on the converter design: for instance, n determines, for a specific input voltage operation, the required voltage gains and the fraction of input power processed by each conversion stage, with significant impact on all the power devices. $R_{\mathrm{DS,ON,LLC}}$ not only has an impact on the cost, conduction and switching losses of the LLC FETs, but also on the magnetizing inductance requirement of the transformer, in turns affecting its size and cost. More detailed considerations on the modelling are provided in Section II-C.

B. Definition of the objective function

The LCOE is a widely adopted figure of merit to compare different technologies used in energy production in terms of the cost-to-benefit ratio over the system lifetime [18]. The complete definition of LCOE involves the computation of the Net Present Value (NPV) of the lifetime costs (including initial investment, operation and maintainance costs, and potential fuel costs) and the NPV of the total output energy produced during the lifetime [19]. In this work, it is of interest to optimize the design of the Parallel Power Optimizer (PPO) in Fig. 1, assuming that the topology, panel specifications and mission profile are design constraints.

The proposed design optimization is based on the search inside the N-dimensional solution space of the optimal variable set, i.e. the combination of design variables optimizing the objective function. As a consequence, all the cost contributions that are fixed independently of the converter design, such as the PV module or the installation costs, are not of interest in this discussion and are neglected from the objective function. Since one of the objectives of the proposed optimization is to ensure, through a reliability constraint, that the converter lifetime matches the PV module lifetime, no replacement costs are considered.

Thus, the system-level definition of LCOE is here reduced and simplified to take into account only the contributions of cost and power conversion losses related to the converter design. For this reason, the objective function is here explicitly called Converter Cost-Energy Ratio (CCER). Denoting by S the trial design solution and by M the mission profile, the definition of CCER becomes:

$$\mathrm{CCER} = \frac{C_{\mathrm{tot}}(S)}{E_{\mathrm{tot}}(S,M)} = \frac{C_{\mathrm{tot}}(S)}{\sum_{k=0}^{25\,\mathrm{yrs}} \left(P_{\mathrm{MPP},k} - P_{\mathrm{loss,tot},k}\right) \Delta t_k}, \quad (1)$$

where $C_{\mathrm{tot}}(S)$ is the cost of components of the design S, $E_{\mathrm{tot}}(S,M)$ is the total harvested energy at the output of the converter in a 25-year operation (for this case study), P_{MPP} is the PV module power and $P_{\mathrm{loss,tot}}$ is the total loss, dependent on both the specific design S and on the mission profile M. The minimization of the scalar objective function expressed in (1) is the goal of the proposed methodology.

The block diagram of the proposed optimization scheme is shown in Fig. 2. For any trial solution S^* inside the solution space, the corresponding CCER* is computed through cost models and loss models applied to the 25-year converter operation. For the converter transistors, the instantaneous losses and junction temperature profiles rely on electro-thermal models, considering the package-dependent thermal resistance $R_{\mathrm{th,j-amb}}$ and the temperature-dependent $R_{\mathrm{DS,ON}}(T_{\mathrm{j}})$. The trial solution S^* is discarded if the reliability criteria are not

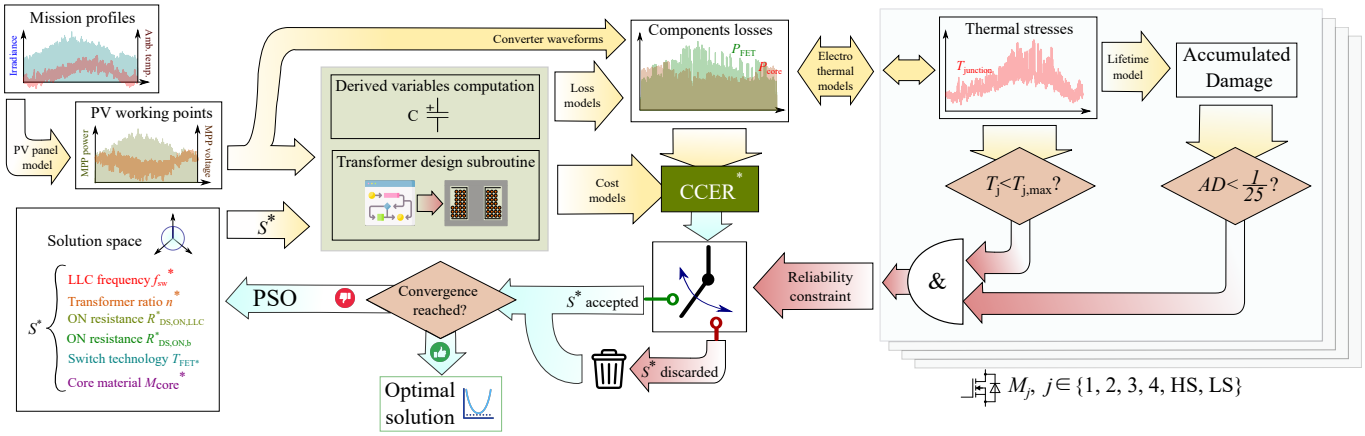


Fig. 2: Block diagram of the proposed optimization methodology. The Converter Cost-Energy Ratio (CCER*) of the trial solution S^* is highlighted in green.

met. The PSO algorithm is exploited to search within the solution space for the design that minimizes the objective function. Further details on the employed models and the reliability constraint are given in the next sections.

C. Modelling

As shown in Fig. 2, the proposed algorithm relies on multiple models to compute the objective function CCER* associated to a certain mission profile and trial solution S^*. A linear PV module model is used to derive the evolution of the working points from irradiance and panel temperature profiles. For simplicity, the MPPT efficiency is not taken into account. The analytical expressions of the converter waveforms in [15] are combined with the loss models for each component of the converter. It is worth noticing that the boost inductor L_b is sized according to the desired frequency window for the boundary conduction mode [15], independently of the rest of the design, and is thus assumed to be fixed. The same applies to the rectifier diodes D_1 and D_2, since their conduction losses only depend on the total power and not on the specific selection of n and f_sw.

For all the other components, specific cost models were derived from the analysis of commercial parts [20]. The computation of the total losses, instead, relied on well-established loss models. Table I lists the adopted loss- and cost models, whose empirical parameters are reported in Table II.

For the LLC switches M_{1-4}, commercial 60 V-rated Silicon MOSFETs and Gallium Nitride Field-Effect Transistors (GaNFETs) were both considered for the modelling. For the boost switches $M_{\mathrm{LS-HS}}$, instead, the 250 V voltage rating, set according to the maximum expected voltage stress, only Si MOSFETs were considered, since the adoption of 650 V-rated GaNFETs would not be justified in terms of increased cost for comparable conduction and switching performances. A double exponential function of the conduction resistance was found to well-fit the unit-price for both the LLC and boost switches, as shown in Fig. 3a. Since all the switches of the converter are assumed to turn ON at zero voltage, only the OFF switching losses are modelled through the OFF time t_OFF:

$$t_\mathrm{OFF} = R_\mathrm{gate} \cdot \frac{Q_\mathrm{sw}(R_\mathrm{DS,ON})}{V_\mathrm{Miller}}, \tag{2}$$

where R_gate, $Q_\mathrm{sw}(R_\mathrm{DS,ON})$ and V_Miller represent the gate resistance, the switching charge involved in the commutation, and the Miller plateau voltage, respectively [21]. The fitting of commercial components turn OFF time for the LLC switches is shown in Fig. 3b, highlighting the superior switching performances of GaNFETs for the same $R_\mathrm{DS,ON}$.

As shown in Fig. 2, for each trial solution S^*, the junction temperature profiles of the corresponding six converter transistors are computed. To do this, the temperature increase due to the switch losses is taken into account in the algorithm through the simplified electro-thermal circuit shown in Fig. 4. The instantaneous junction temperature T_j is fed back through the non-linear function $\alpha_\mathrm{R}(T_\mathrm{j})$, modelling the increase of conduction resistance with increasing temperature. No heat sink is adopted in the converter, thus the junction-to-ambient thermal resistance $R_\mathrm{th,j-amb}$ was selected from the worst-case values of the switches datasheets. Notice that, since the time-step of the mission profiles is significantly longer (1 min) than the typical thermal time constants of the discrete components (without heat sink), any thermal capacitance is neglected from Fig. 4.

Film capacitors were selected for both C_in and C_b, with different voltage ratings, i.e. 63 V and 300 V, respectively. Their minimum capacitance value is, at each iteration of the algorithm, computed from the design equations in [15]. Both the cost and conduction loss models were derived by fitting the price per unit and Equivalent Series Resistance (ESR) as functions of the capacitance value.

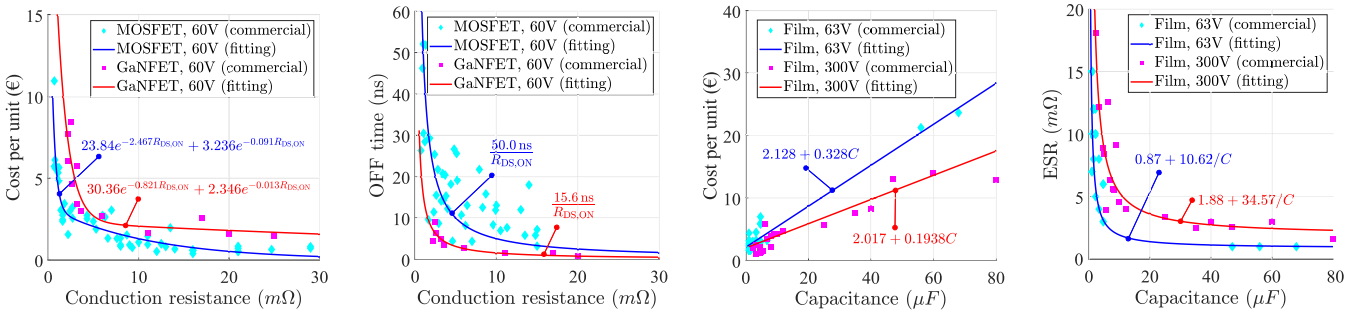
As shown in Fig. 2, a specific subroutine of the algorithm was developed to extract the main geometry- and

TABLE I: List of the main cost and loss models adopted in the optimization algorithm.

Component	Primary variables	Derived variables	Cost model	Loss model
LLC FETs M_{1-4}	$R_{\mathrm{DS,ON,LLC}}$, T_{FET}, f_{sw}	t_{OFF}, α_{R}	$b_1 e^{d_1 R_{\mathrm{DS,ON,LLC}}} + b_2 e^{d_2 R_{\mathrm{DS,ON,LLC}}}$	$R_{\mathrm{DS,ON,LLC}} \alpha_{\mathrm{R}}(T_{\mathrm{j}}) I^2_{\mathrm{RMS}} + \frac{1}{2} t_{\mathrm{OFF}} f_{\mathrm{sw}} V_{\mathrm{OFF}} I_{\mathrm{ON}}$
Boost FETs $M_{\mathrm{LS-HS}}$	$R_{\mathrm{DS,ON,b}}$	t_{OFF}, α_{R}	$b_3 e^{d_3 R_{\mathrm{DS,ON,b}}} + b_4 e^{d_4 R_{\mathrm{DS,ON,b}}}$	$R_{\mathrm{DS,ON,b}} \alpha_{\mathrm{R}}(T_{\mathrm{j}}) I^2_{\mathrm{RMS}} + \frac{1}{2} t_{\mathrm{OFF}} f_{\mathrm{sw}} V_{\mathrm{OFF}} I_{\mathrm{ON}}$
Input capacitor C_{in}	f_{sw}, n	C_{in}, $ESR(C_{\mathrm{in}})$	$c_1 + c_2 \cdot C_{\mathrm{in}}$	$ESR(C_{\mathrm{in}}) I^2_{\mathrm{RMS}}$
Boost capacitor C_{b}	n	C_{b}, $ESR(C_{\mathrm{b}})$	$c_3 + c_4 \cdot C_{\mathrm{b}}$	$ESR(C_{\mathrm{b}}) I^2_{\mathrm{RMS}}$
Transformer core and bobbin	f_{sw}, n, M_{core}	L_{magn}, AP, N_1, V_{eff}, α_{SE}, β_{SE}, ρ_{SE}	$g_1 + g_2 AP^{\frac{1}{2}}$	$\frac{\pi}{4} K_{\mathrm{core}} V_{\mathrm{eff}} (AP) \rho_{\mathrm{SE}} f_{\mathrm{sw}}^{\alpha_{\mathrm{SE}}} \Delta B^{\beta_{\mathrm{SE}}}$
Transformer windings	f_{sw}, n	d_{s}, ω_{Cu}, N_1, N_2, R_{p}, F_{p}, R_{s}, F_{s}	$g_3 + \omega_{\mathrm{Cu}} \cdot \left[g_4 + g_5 e^{g_6 d_{\mathrm{s}}} \right]$	$R_{\mathrm{p}} F_{\mathrm{p}} I^2_{\mathrm{p,RMS}} + R_{\mathrm{s}} F_{\mathrm{s}} I^2_{\mathrm{s,RMS}}$

TABLE II: Empirical parameters of the cost models in Table I.

Parameter	Value	Parameter	Value	Parameter	Value
b_1	23.84 €(Si) / 39.36 € (GaN)	d_3	$-0.0393\,\mathrm{m\Omega^{-1}}$ (Si)	g_1	0.704 €
b_2	3.236 €(Si) / 2.346 € (GaN)	d_4	$-0.003\,\mathrm{m\Omega^{-1}}$ (Si)	g_2	2.83 €/cm^2
b_3	7.62 € (Si)	c_1	2.128 €	g_3	0.5 €
b_4	2.791 € (Si)	c_2	0.328 €/μF	g_4	19.04 €/kg
d_1	$-2.467\,\mathrm{m\Omega^{-1}}$ (Si) / $-0.821\,\mathrm{m\Omega^{-1}}$ (GaN)	c_3	2.017 €	g_5	1323 €/kg
d_2	$-0.091\,\mathrm{m\Omega^{-1}}$ (Si) / $-0.013\,\mathrm{m\Omega^{-1}}$ (GaN)	c_4	0.194 €/μF	g_6	$-886\,\mathrm{cm^{-1}}$



(a) (b) (c) (d)

Fig. 3: Cost and key parameters of the loss models for some of the converter components, extracted from the analysis of commercial parts. (a) Cost per unit of 60 V Silicon MOSFETs and GaNFETs as function of $R_{\mathrm{DS,ON}}$. (b) Turn-OFF time of 60 V Silicon MOSFETs and GaNFETs as a function of $R_{\mathrm{DS,ON}}$. (c) Cost per unit of 63 V film capacitors (C_{in}) and 300 V capacitors (C_{boost}) as a function of the capacitance. (d) Equivalent Series Resistance (ESR) of 63 V and 300 V film capacitors as a function of the capacitance.

material-related parameters of the transformer core, such as the area product AP, the number of primary turns N_1, the effective volume V_{eff} or the Steinmetz Equation coefficients α_{SE} , β_{SE} , ρ_{SE} [22]. The cost model was derived from commercial EE and ETD cores, for their widespread adoption in power electronics applications and their availability in different sizes and materials. For the transformer windings, the cost model for Litz wire coils is based on the overall windings weight ω_{Cu} and diameter d_{s} of the copper strands [23]. The loss model takes into account the increase of the winding resistance due to the proximity effect through the coefficients F_{p} and F_{s} [24]. To limit the impact of the AC losses in the windings, the strand diameter is selected to be $1/3$ of the skin depth. For a specific variable set S^*, the most impactful degrees of freedom on the transformer losses and cost are AP and N_1, from which many derived variables follow. At each iteration of the PSO algorithm, thus, the transformer design subroutine is responsible for identifying the domain of all

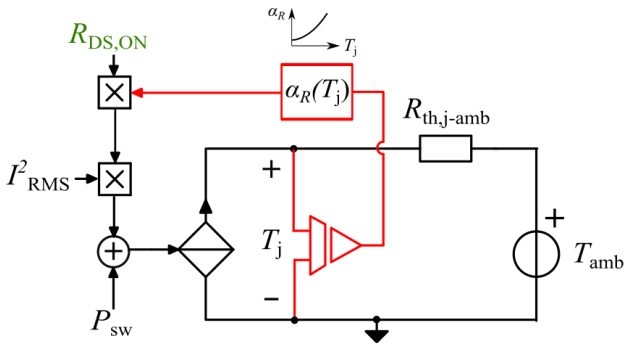


Fig. 4: Steady-state electro-thermal circuit considered in the optimization algorithm for the computation of the temperature-dependent losses of the converter switches.

the potential solutions $\{AP^*,\ N_1^*\}$, intersecting the following constraints:

- for a specific AP^*, N_1 must be sufficiently large to keep the flux density ΔB across the magnetic cross-section A_e lower than the maximum desired value (in this case, the ΔB_{max} associated to $100\,\mathrm{mWcm^{-1}}$ loss density [25]):

$$N_1 > \frac{V_{in,max}}{2 f_{sw} \Delta B_{max} A_e (AP^*)} \tag{3}$$

- for a specific AP^*, the primary and secondary coils, with conductor cross section A_{cond} must fit in the available window area A_w [26]:

$$N_1 < \frac{K_w A_w (AP^*)}{2 A_{cond}} \tag{4}$$

- the operation of the LLC switches in Zero-Voltage Switching (ZVS) requires a certain magnetizing inductance L_{magn}, resulting in a triangular magnetizing current superimposed to the resonant sinusoidal current [15], [27]. For a specific AP^* and inductance factor A_L, N_1 should be large enough to obtain the required L_{magn}:

$$N_1 > \sqrt{\frac{L_{magn}}{A_L (AP^*)}}\,. \tag{5}$$

The intersection of (3), (4) and (5) defines the domain of all the potential solutions $\{AP^*,\ N_1^*\}$. The subroutine is responsible for searching the optimal solution $\{AP_{opt},\ N_{1,opt}\}$ that minimizes the *ad hoc* cost-output power ratio CPR_T objective function:

$$CPR_T(AP,\ N_1) = \frac{C_{core} + C_{bobbin} + C_{coils}}{P_{rated} - P_{core} - P_{windings}}\,, \tag{6}$$

where the numerator consists of the sum of the core, bobbin and coils costs, whereas the denominator is obtained by subtracting the total transformer losses from the rated input power.

Additional constraints are added in the transformer design subroutine: the transformer temperature should never exceed $T_{max} = 100\,^\circ\mathrm{C}$, and the maximum flux density should be kept below the saturation B_{sat}.

D. Constraints

In order to limit the 6-dimensional solution space, the range of the design variables are constrained: $f_{sw} \in [50\,\mathrm{kHz},\ 500\,\mathrm{kHz}]$, $n \in [3.2,\ 4.0]$, $R_{DS,ON,LLC} \in [1\,\mathrm{m\Omega},\ 20\,\mathrm{m\Omega}]$, $R_{DS,ON,b} \in [10\,\mathrm{m\Omega},\ 150\,\mathrm{m\Omega}]$, $T_{FET} \in \{\mathrm{Si},\ \mathrm{GaN}\}$, $M_{core} \in \{\mathrm{N27},\ \mathrm{N87},\ \mathrm{N97}\}$.

Contrarily to other works [9], in which the converter topology is a degree of freedom, here the IPOS topology in Fig. 1 is given as constraint, as well as the PV module [28].

As mentioned in Section I, one of the novelties of this article is the inclusion of a mission profile-based reliability constraint on the converter switches. Electrolytic capacitors, which are among the most critical components in terms of reliability [29], are not adopted in this converter. The reliability constraint consists of a set of two conditions to be satisfied by each converter switch: the junction temperature must never exceed the maximum datasheet value $T_{j,max}$, and the accumulated damage (AD) due to the repeated thermal stresses in one year must be low enough to ensure a 25-years lifetime. The lifetime computation follows the approach described in [30]. Firstly, the yearly junction temperature profiles are decomposed into elementary thermal cycles applying the rainflow counting method; then, the lifetime model expressed in (7) [31] is applied to derive the number of cycles to failure $N_{f,i}$ associated to each thermal stress; finally, all the damage contributions are summed up to compute the Accumulated Damage (AD), as expressed in (8):

$$N_{f,i} = A \cdot \Delta T_{j,i}^{B} \cdot \exp\left(\frac{C}{\overline{T}_{j,i} + 273}\right) \tag{7}$$

$$AD = \sum_i \frac{N_i}{N_{f,i}}\,, \tag{8}$$

where $A = 4.9283 \cdot 10^{13}$, $B = -5.2776$, $C = 812$ and N_i is the number of cycles counted for the specific thermal stress i [31]. The trial solution S^* is discarded in case at least one of the converter switches exceeds $T_{j,max}$ or its $AD > \frac{1}{25}$, meaning that the converter is likely to fail before 25 years.

III. Results

A. Impact of mission profile on optimal solution

A PSO search algorithm was chosen among other metaheuristic approaches because of its low complexity and the limited number of user-defined parameters [5]. The algorithm was implemented in Matlab considering a population of 30 solutions moving in the 6-dimensional solution space: the algorithm stops when the objective function CCER converges to a stable value within $\pm 0.5\%$.

Table III reports the results of the optimization algorithm for three different mission profiles, i.e. Aalborg (Denmark), Arizona (USA), and Turin (Italy). Independently of the mission profile, the PSO always converges to $n = 4$: according to [15], this transformer ratio ensures that, at the rated PV panel voltage $V_{in} = 36.5\,\mathrm{V}$, around 83% of the total input power is processed by the LLC stage, while only around 17% by the boost. A strongly unbalanced power splitting,

TABLE III: Results of the optimization algorithm for three different mission profiles: Aalborg (Denmark), Turin (Italy), Arizona (USA).

Mission profile	f_{sw}	n	M_{core}	T_{FET}	$R_{DS,ON,LLC}$	$R_{DS,ON,b}$	CCER
Aalborg	290 kHz	4	N97	Si	10 mΩ	130 mΩ	9.69 €/MWh
Arizona	240 kHz	4	N87	Si	10 mΩ	50 mΩ	3.43 €/MWh
Turin	250 kHz	4	N87	Si	13 mΩ	120 mΩ	6.19 €/MWh

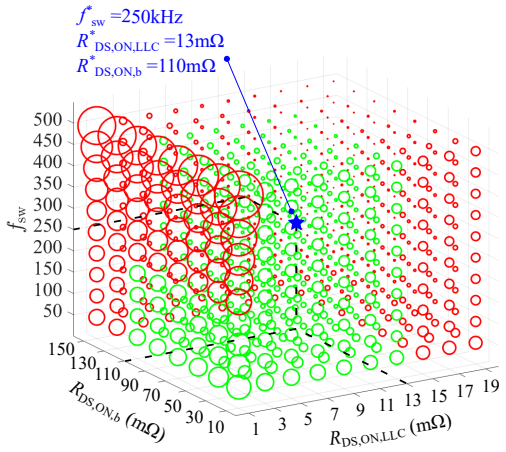


Fig. 5: Results of CCER with a constrained exhaustive search ($n = 4$, T_{FET} =Si, M_{core} =N97), for Turin mission profile. The markers size is proportional to the corresponding CCER. The optimal solution is highlighted with a blue star, while the red markers identify discarded solutions.

indeed, significantly reduces the current and voltage stresses on the boost switches, in terms improving their reliability, and helps reducing the size and cost of the filtering capacitors. In addition, the optimal variable sets always prefer Silicon MOSFETs over Gallium Nitride FETs: for the same $R_{DS,ON}$, the improved switching performances of the latter are not sufficient to justify the larger cost.

For the latter case, a constrained exhaustive search was performed by fixing transformer ratio $n = 4$, core material $N87$ and switch technology T_{FET} =Si, and sweeping the remaining design inputs. The results are graphically shown in Fig. 5, in which the size of the circular markers at each triplet of coordinates is directly proportional to the corresponding CCER. The green and red markers represent acceptable and non-acceptable solutions, respectively. It is relevant to observe that three different regions of the variable space do not satisfy the reliability constraints: 1 mΩ MOSFETs fail for $f_{sw} \geq 250$ kHz due to the high switching losses, whereas $R_{DS,ON,LLC} \geq 15$ mΩ and $R_{DS,ON,b} \geq 130$ mΩ are both unacceptable regions because of the high conduction losses. The minimum CCER solution is highlighted in blue and is consistent with the optimal solution found by the PSO (refer to Table III). Despite the larger conduction losses, the reduced cost of higher $R_{DS,ON}$ transistors is decisive to decrease the objective function. As a result, the minimum CCER is found in correspondence of the highest $R_{DS,ON,b}$ and $R_{DS,ON,LLC}$ still

TABLE IV: Selected components of the converter design for the Arizona case, used for the simulation results.

Component	Part number
LLC switches M_{1-4}	IPB090N06N3
Transformer core	ETD 44/22/15, N97
Transf. primary coil	5 turns, 2400x44 µm
Transf. secondary coil	20 turns, 600x44 µm
Rectifier diodes D_{1-2}	STTH30R04
Boost switches M_{HS-LS}	IPB600N25N3
Boost inductor L_b	74437529203330
Boost capacitor C_b	R75MW51004030J
Input capacitor C_{in}	4x CB182D0475JBC

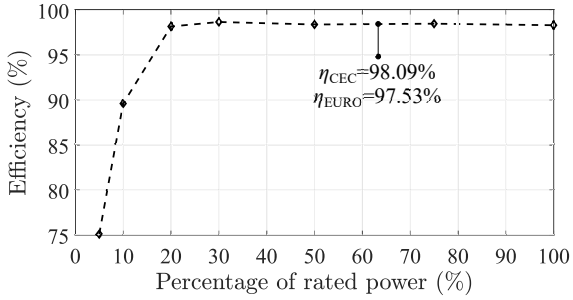


Fig. 6: Simulation results of converter efficiency as a function of operating power, at the rated voltage $V_{in} = 36.5$ V.

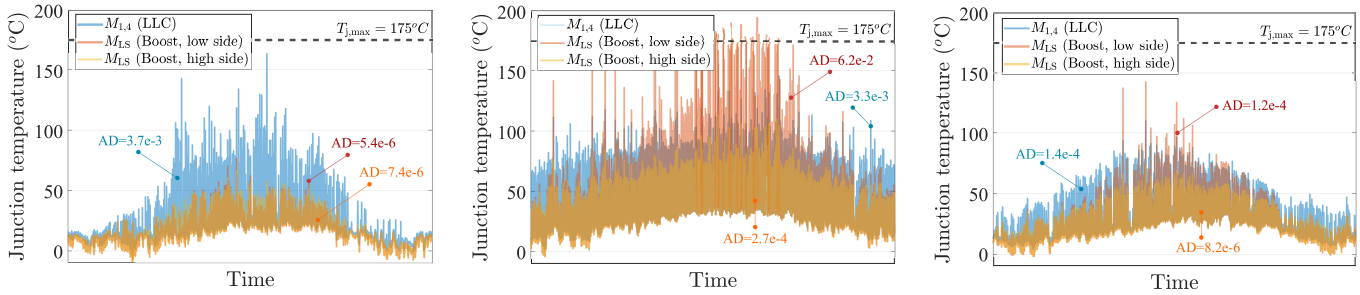
meeting the reliability constraints. In addition, independently of the mission profile, the PSO always converges to $n = 4$: according to [15], this transformer ratio ensures that, at the rated PV panel voltage $V_{in} = 36.5$ V, around 83% of the total input power is processed by the LLC stage, while only around 17% by the boost. A strongly unbalanced power splitting, indeed, significantly reduces the current and voltage stresses on the boost switches, in terms improving their reliability, and helps reducing the size and cost of the filtering capacitors.

B. Simulation results of optimal solution

From the worst-case solution of Table III, which corresponds to the harshest environment conditions (Arizona), a converter was designed with the components in Table IV and simulated in Matlab and LTspice. The transformer was designed according to the procedure illustrated in Section II.

Fig. 6 shows the simulated converter efficiency as a function of the output power at the rated input voltage condition, $V_{in} = 36.5$ V, and assuming 25 °C ambient temperature. The simulations were performed in LTspice with Spice models for both the active and passive devices. The calculated California Energy Commission (CEC) and European (EURO) efficiency are 98.09% and 97.53%, respectively.

Fig. 7 shows the annual junction temperature profiles for the selected converter transistors, referred to Aalborg (Fig. 7a), Arizona (Fig. 7b) and Turin (7c) mission profiles. The resulting annual AD is also reported for each temperature profile. The results were extracted in Matlab considering the electro-thermal circuit in Fig. 4. It is worth noticing that the selected MOSFET for the boost low-side switch does not meet



(a) (b) (c)

Fig. 7: Annual profile of the switches junction temperatures corresponding to three different mission profiles. (a) Aalborg (Denmark); (b) Arizona (USA); (c) Turin (Italy).

the reliability constraint in the Arizona mission profile: its worst-case junction-to-ambient thermal resistance is indeed higher than the one considered in the optimization ($62\,\mathrm{K/W}$ against $40\,\mathrm{K/W}$), and its $R_{\mathrm{DS,ON,b}}$ is slightly larger than the recommended $50\,\mathrm{m\Omega}$. A more conservative components selection and a proper thermal design at a layout level would be essential to meet the reliability constraint with a sufficient safety margin. Notice that, in general, a higher ambient temperature in the mission profile (Turin or Arizona) shifts the MPP of a PV panel to lower voltages, thus increasing the gain requirement of the boost and the electrical stresses of its devices.

IV. Conclusions

This article proposes a new optimization methodology for the design of power converters that is based on the minimization of the cost-energy ratio and that includes a mission profile-based reliability constraint. The proposed methodology is suited for power converters designed for photovoltaic applications, where cost, efficiency and reliability are crucial tradeoffs. The approach is applied to the specific case study of an asymmetric IPOS power optimizer consisting of a LLC and a synchronous boost stage. At each step, the proposed algorithm exploits multiple analytical and empirical models to compute the cost and losses of the trial converter solution, and discards it if at least one of the converter switches does not meet the reliability constraints. The PSO method is used to search for the optimal solution inside a 6-dimensional solution space. The algorithm is run for three different mission profiles, highlighting that the optimal solutions privilege a strongly unbalanced power splitting between the two stages and Silicon devices over Gallium Nitride ones. From the worst case optimal solution, a converter is designed and simulated, showing a California Energy Commission efficiency above 98%. The future steps of this work include the design of a physical prototype and its experimental validation.

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