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Advanced digital readout and signal processing techniques for radiation sensors

By

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

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This thesis will present the work performed for two different and separated projects.

In the context of the ALICE experiment at CERN, the ZDC detector upgraded its readout system in order to be able to acquire data in all collisions in self-triggered mode without dead time at the expected luminosity offered by LHC in Run 3. The ZDC operating conditions in Pb–Pb collisions are extremely challenging due to the presence of ElectroMagnetic Dissociation processes that increase the need for high readout rate and the large signal dynamics (from a single neutron to ≈ 60 neutrons). The new acquisition chain is based on a commercial 12 bit FMC digitizer mounted on a commercial VME carrier board. The signals produced by the ZDC channels are digitized, the samples are processed through an FPGA that, thanks to a custom trigger algorithm, flags for readout the relevant portion of the waveform and extracts information such as timing, baseline average and event rate. When running in self-triggered mode the ZDC system is able to sustain a readout rate of ≈ 2.5 Mevents/s not only meeting the bandwidth request, but taking into account a safety factor of 2, for the channels of the most exposed calorimeters. My contribution consisted of the development of the FPGA readout firmware used for data taking, of the commissioning of the hardware at CERN and of the constant supervision of the data taking stability and performance of the ZDC detector during Pb–Pb collisions. The architecture of the detector and, more specifically, of the new readout system will the presented in chapter 2. Thanks to the new Continuous Readout Mode and the LHC increased luminosity, the ZDC detector was able to acquire more events than during Run 1 and Run 2 combined. A report of the data taking periods, the performance of the new readout system and a showcase of the acquired data for each period and data taking condition will be presented in chapter 3. It will be shown that the energy spectra resolution improved w.r.t. the previous readout system. Run 1 and Run 2 had a resolutions of the 1 neutron signal of about 20%, meanwhile, during Run 3, the detector constantly achieved 16%. The ZDC time resolution allows the ALICE data analysis team to more easily reject parasitic collisions.

In the context of the NUSES collaboration and the PBR space mission, the INFN microelectronics team undertook the realization of the MIZAR ASIC. This 64-channel custom IC built in 65-nm CMOS technology designed for readout of SiPMs signals is expected to be used as a technology demonstrator for the use of such detector in space for the study of Extensive Air Showers produced by Ultra-High Energy Cosmic Rays and Ultra-High Energy tau Neutrinos. The integrated ADC is configurable to operate with a resolution between 8 and 12 bit at a 200 MHz sampling rate. The power budget of the system is 5 mW/channel. Given the extreme data bandwidth constraints due to the earth-space link, an elaborate multi-layer trigger system was implemented into the ASIC in order to reject as much noise as possible without affecting the data. This resulted in a configurable double threshold for each channel and a hitmap generator. The resulting hitmaps are sent to an FPGA for real time evaluation of the patterns. The configuration of the ASIC parameters, the hitmap trigger decision and the data packet formation are all managed by a readout FPGA. My contribution for the collaboration consisted of the complete development of the FPGA readout firmware, i.e. of the design of the hitmap evaluation algorithm, the configuration logic and the data handling machinery. This will be presented in detail in chapter 4. The performance of the designed readout system were asserted with simulations and in laboratory by means of an ASIC emulator developed with a second FPGA board. All the performed tests and the results obtained will be discussed in chapter 5.