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Impact on Linearity of a Wideband Design Strategy for an Integrated GaN Doherty Power Amplifier

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***Abstract*—This paper presents the design and linearity characterization of an integrated Doherty amplifier for 5G applications in the FR1 bands, implemented on a 150 nm GaN/SiC HEMT technology. It achieves 5G real-case-scenario performance over a 41% state-of-the-art fractional bandwidth, with 37 dBm saturated output power, 19 dB small-signal gain, and power-added efficiency above 20% over 6 dB back-off. The impact of the wideband combiner strategy on the linearity of the amplifier is analyzed in terms of baseband impedance and AM/PM. The characterization is then presented, with continuous wave and modulated signals for 100 MHz and 200 MHz instantaneous bandwidths. In presence of a 256-QAM 200 MHz input signal, the predistorted amplifier presents at 4.15 GHz an EVM of 2.9%.**

***Index Terms*—5G, AM/PM, Doherty power amplifier, EVM, GaN, linearity, MMIC, wideband.**

I. Introduction

The use of complex modulation schemes in 5G architectures results in signals with a high peak-to-average power ratio (PAPR), requiring the power amplifier (PA) to operate efficiently at output power back-off (OBO), i.e., away from saturation. The Doherty power amplifier (DPA) is one of the most popular solutions for back-off efficiency enhancement.

A distinctive feature of 5G systems is the wide modulation bandwidth, while even wider RF bandwidths are necessary to allow system interoperability in the modern telecommunication world where different standards coexist. These aspects are particularly critical for DPAs, where the combiner is implemented with quarter-wave transmission lines, inherently narrowband. Wideband hybrid DPA demonstrators are present in the literature with single-stage configurations [1], [2] and therefore limited gain which is not suitable for real scenarios.

Another aspect of 5G architectures is the use of a large number of antennas in multiple input/multiple output configurations. The introduction of digital pre-distortion blocks in front of the PAs, necessary to make the system achieve the necessary linearity requirements, results in bulky and expensive systems. Therefore understanding the impact of the design strategies on the system linearity has become even more crucial today to allow the next generation of PAs to be efficient and linear at the same time.

In terms of semiconductor technology, GaAs MMIC implementations are limited to the watt-level and cannot reach several watts of output power [3], making them unsuitable for high-power applications. Conversely, GaN, from its initial development [4] to more recent technological improvements [5], has emerged as the best tradeoff between design complexity, achievable output power and thermal handling [6], making it the preferred choice for high-efficiency PA solutions.

This work presents the design and experimental characterization of an integrated GaN DPA aiming to achieve real-case scenario performance for power and gain in the 5G FR1 frequency bands N77 (3.3-4.2 GHz) and N79 (4.4-5 GHz). It adapts the wideband strategy of [7] and extends its validity. The impact of the design choices necessary to achieve the state-of-the-art fractional bandwidth of 41% presented in detail in [8], are here analyzed in terms of their impact on linearity. The linearity of the implemented chip is characterized in terms of amplitude and phase distortion (AM/AM and AM/PM) and Error Vector Magnitude (EVM).

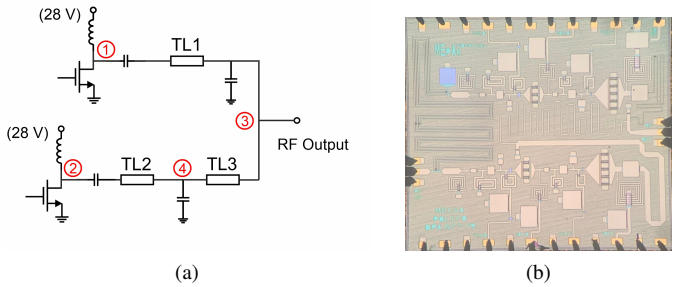


Fig. 1: Combiner schematic with possible bias insertion points highlighted (a) and manufactured $(3.7\times3.3)\,\mathrm{mm}^2$ chip (b).

II. Design

The selected technology is a 150-nm-gate-length GaN/SiC process by WIN Semiconductors, which delivers approximately 4 W/mm at 28 V. To achieve a wide bandwidth a symmetric topology is adopted, with identical transistor size for the Main and Auxiliary amplifiers and equal input power splitting. Two $10\times100\,\mu\mathrm{m}$ transistors are combined as final stage power devices. Their optimum load is close to the target output impedance of $50\,\Omega$, which is beneficial for synthesising wideband matching. The small signal analysis of a single device shows a gain of about 15 dB after stabilization, so a

6×75 µm driver is inserted in each branch to achieve an overall DPA gain of about 20 dB.

To overcome the bandwidth-limiting behaviour of a Doherty combiner, this design applies to a two-stage architecture the combiner topology from [7], which was proved to achieve more than 80% of bandwidth in a hybrid single-stage DPA. This topology foresees a λ/4 impedance inverter on the Main branch and two λ/4 sections on the Auxiliary branch shown in Fig. 1 as TL_1, TL_2, and TL_3, respectively. The output parasitics are embedded in the combiner design.

Some limitations are found in the application to an integrated design of the hybrid-proved strategy. To effectively cover a 80% relative bandwidth a distributed approach must be adopted. It is verified that in the adopted integrated technology the characteristic impedances for the target load and output power are already close to the feasibility limit with characteristic impedances $Z_1 = 76\,\Omega$, $Z_2 = 114\,\Omega$ and $Z_3 = 150\,\Omega$, corresponding to a width of 32 µm, 6 µm and 2 µm respectively. This values must then be increased to embed the parasitic.

To partially overcome these limitations, the target back-off and saturation loads are selected according to a trade-off between output power, efficiency and bandwidth. To cover the 41% relative bandwidth the final characteristic impedances selected are $Z_1 = 103\,\Omega$, $Z_2 = 54\,\Omega$ and $Z_3 = 87\,\Omega$ corresponding to 9 µm, 80 µm and 20 µm widths respectively.

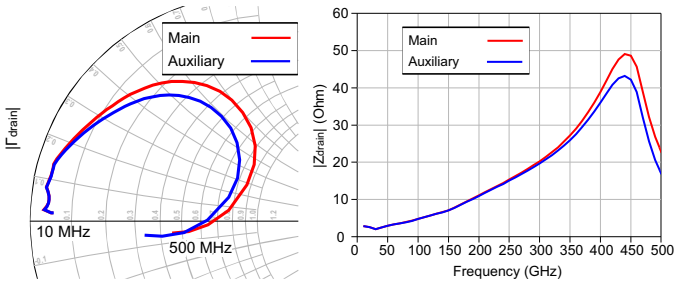
The high characteristic impedances also limit the choice of the bias feeding insertion point. In fact, the high-impedance lines required can only be synthesized if no DC current needs to flow through them, which forces the insertion of the DC feed and block right at the devices' drain in positions 1 and 2 of Fig. 1. Alternatively, a single feeding point could be utilized and positions 3 and 4 could also be considered.

In the proposed design the use of λ/4 feeding lines is prevented by the space constraints, therefore each device is separately biased at its drain through a large lumped inductor. A DC blocking capacitor is inserted right after, allowing to synthesize the thin combiner lines. The resulting combiner achieves a uniform load modulation for the Main, whose intrinsic load is modulated by a factor 1.6 over the whole bandwidth, close enough to the target load modulation factor 2 of an ideal 6 dB Doherty.

The RF feeding choke insertion at the device drain allows the application of the original combiner configuration and therefore wideband performance, but prevents from minimizing the baseband impedance [9]. According to [10] values of baseband impedance that deviate from the short circuit condition can prevent good linearity performance, especially if they have a large imaginary component.

Fig. 2 shows the baseband impedances presented at the drain of the final stage power devices. The maximum values in magnitude observed in the 10 MHz-500 MHz frequency range are 43 Ω and 49 Ω for the Main and Auxiliary, respectively. Due to the adopted biasing method, the baseband impedances deviate from the ideal short circuit and present a significant imaginary component at hundreds of MHz. They cannot be controlled either on or off chip, due to the presence of the RF choke and the fact that the operating frequencies are almost comparable (only 1 order of magnitude higher) to the foreseen modulation bandwidth.

The simulated AM/PM is lower in magnitude than 25 ° over the whole bandwidth, and the circuit is optimized for gain flatness. A further optimization of these parameters is not possible due to a tight trade-off between bandwidth and efficiency, in addition to the baseband impedance considerations introduced. Nevertheless, the achieved AM/PM control is typically considered acceptable to grant the linearizability of the circuit, considering also that this parameter becomes less indicative as the modulation instantaneous bandwidth increases.



(a) (b)

Fig. 2: Baseband impedances seen at the drain of the Main (red) and Auxiliary (blue) final stage power devices: (a) normalized to 50 Ω on the Smith Chart and (b) magnitude on cartesian plot.

III. Experimental Characterization

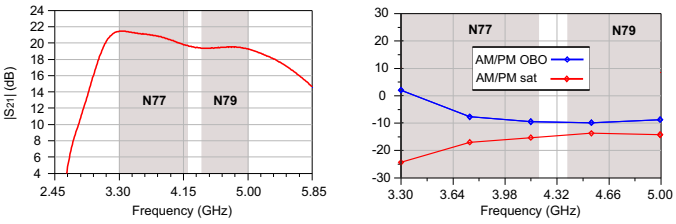
The characterization is performed at the nominal bias point: $V_{G,M}$=-2 V, $V_{G,A}$=-3 V, V_{DD}=28 V, I_D=36 mA.

Fig. 3a shows over the whole design bandwidth a minimum $|S_{21}|$ of 19 dB and a variation of 3 dB, while the variation over the single N77 and N79 is of 2 dB and 0.5 dB, respectively. The gain flatness performance is quite good, especially in the upper band. Fig. 3b shows the measured AM/PM under single-tone continuous wave (CW) excitation, which is in magnitude below 10 ° and 25 ° at 6-dB OBO and saturation, respectively.

The CW characterization is performed over the band from 3.3 GHz to 5 GHz and is discussed in detail in [8]. It shows a minimum of 37 dBm saturated power and saturated and 6 dB back-off PAE values higher than 20%. Overall, the 41% fractional bandwidth is maintained with uniform performance at the implementation level.

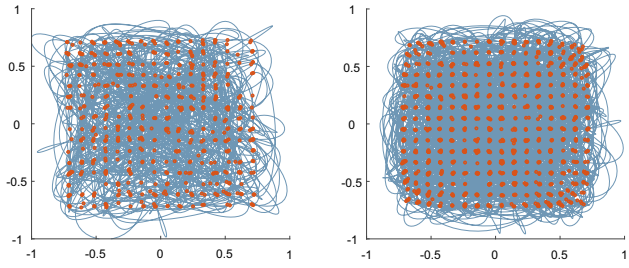
The system-level linearity of the DPA is assessed exploiting a Keysight N5242B PNA-X and its embedded direct digital predistortion (DPD) routine, with a maximum of 5 iterations. A 256-Quadrature Amplitude Modulation (QAM) modulation with increasing instantaneous bandwidth (50 MHz, 100 MHz and 200 MHz) is considered.

Fig. 4 compares the output constellations with 100 MHz and 200 MHz bandwidth at 4.15 GHz, extending the characterization presented in [8] with 50 MHz bandwidth. After DPD,



(a) (b)

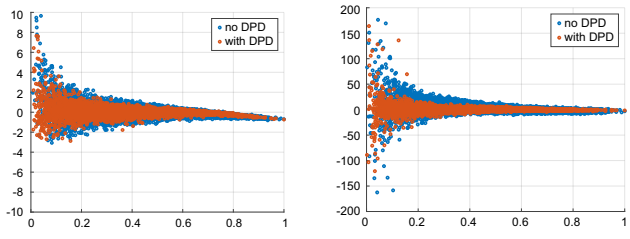
Fig. 3: Measured (a) small signal $|S_{21}|$ and (b) AM/PM in single-tone CW versus frequency.



(a) (b)

Fig. 4: Measured output constellations of a 256-QAM signal at 4.15 GHz, with (a) 100-MHz and (b) 200-MHz instantaneous bandwidth. After DPD, ACPR of -35 dBc and -25 dBc and EVM of 5% and 2.9%, respectively.

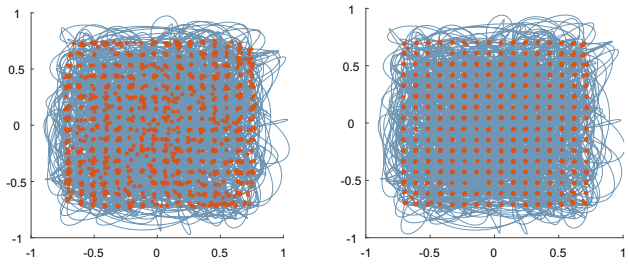
at an average output power of about 33 dBm and average efficiency of about 22%, the DPA shows EVM of 5% and 2.9%, respectively. These results demonstrate that for increasing modulation bandwidth, up to a factor of four compared to the initially adopted one, the PA maintains comparable linearity performance. This conclusion is further supported by the AM/AM and AM/PM characteristics for the 200-MHz case, shown in Fig. 5 at 4.15 GHz, both before (blue) and after (red) DPD.



(a) (b)

Fig. 5: Measured (a) AM/AM and AM/PM (b) under 256-QAM 200-MHz signal excitation at 4.15 GHz.

Fig. 6 shows the constellations with 200 MHz bandwidth at 3.5 GHz and 4.8 GHz, respectively. At 33 dBm average output power and 24% average efficiency, the EVM is 4.3% and 1.2%, respectively. The linearity in the N79 band is higher than the one in the N77, which can be attributed to the better gain flatness and gain symmetry, as presented in Fig. 3a. Fig. 3b also shows how the AM/PM is larger in magnitude for lower frequencies in a CW characterization. Therefore the gain flatness and AM/PM linearity parameters show their consistency with the system-level modulated results.



(a) (b)

Fig. 6: Measured output constellations of a 256-QAM 200-MHz signal at (a) 3.5 GHz and (b) 4.8 GHz. After DPD, at average output power 33 dBm and average efficiency 24%, EVM is 4.3% and 1.2%, respectively.

Overall, the system-level characterization shows that the linearity performance of the DPA is not sufficient for its use without external predistortion, but an effective linearization of the chip is possible in the presence of a 5G modulation with increasingly wide instantaneous bandwidths.

The achieved CW performance is compared to the state of the art of sub-6 GHz DPAs in Table I, where the proposed DPA exhibits the widest bandwidth among two-stage architectures with comparable gain. The linearity performance is not included in the table since uniform data and testing conditions are not always available in the referenced works.

TABLE I: Comparison with state-of-the-art GaN MMIC DPAs for 6 dB OBO.

Ref.	Freq. (GHz)	BW (%)	G_{SS} (dB)	P_{sat} (dBm)	PAE_{sat} (%)	PAE_{6dB} (%)
[11]	2.14	–	19.6	41	56	40
[12]	4.4-5.1	15	17.5	41	45	40
[13]	3.2-4.7	38	8	29	35	31
T.W.	**3.3-5.0**	**41**	**19**	**37**	**20**	**20**

CONCLUSIONS

The paper has presented the design and characterization of an integrated Doherty power amplifier, focusing on the impact of the design choices necessary to achieve the state-of-the-art 41-% fractional bandwidth on the linearity performance. The complete linearity characterization in terms of AM/AM, AM/PM and EVM is presented. The DPA achieves 5G real-case-scenario performance of 37 dBm saturated output power, 19 dB small-signal gain, and PAE above 20% over 6 dB back-off. In presence of a 256-QAM 200-MHz modulating signal, the predistorted DPA presents at 4.15 GHz an EVM of 2.9%.

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