AMBEATion: New Algorithm for Generation IC Matched Structures with Respecting Linear and Non-linear Gradient Parameter Effects

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***Abstract*— This paper presents an innovative algorithm designed by AMBEATion consortium for optimizing the position of the critical structures in semiconductor integrated circuits (IC). The consortium, includes global semiconductor companies and leading universities, aims to address this challenge. The algorithm showcased its efficacy through testing on 6 600 diverse cases, particularly focusing on the 3rd order of the non-linear gradient of the environment. The results reveal high-quality matched performance, exemplified by minimal threshold voltage mismatches for current mirrors. The algorithm's versatility makes it a recommended solution for varied applications. It emphasizes the need for configuring control parameters efficiently within the modified Simulated Annealing (SA) methodology, highlighting its significance in achieving optimal computational efficiency and performance across different technological domains.**

Keywords*— IC layout optimization, Simulated Annealing, matching of the critical structures, semiconductor development.

I. INTRODUCTION

At the present time, the high demand for the best electrical performances of the Analog and Mixed-Signal integrated circuits (AMS ICs) is required. To achieve the highest quality of the electrical performances in the ICs, the physical designs (layouts) of the semiconductor devices should be designed accordingly.

The semiconductor devices can be categorized into two primary types: active and passive components. Active components predominantly consist of Metal-Oxide-Semiconductor (MOS) transistors and bipolar transistors (BJT). Passive components are exemplified by resistors and capacitors. Both active and passive components undergo common modeling and monitoring during process development and manufacturing through parametric testing [1]. This development yields measured data directly describing attributes such as resistances, capacitances, gate capacitances, threshold voltages, or limitations of the tested components, such as voltage classes and maximum drain currents. These parameters and their statistical ranges define the properties and potential applications of the components, serving as crucial information for IC designers. Adhering to this data, IC designers can make informed decisions in selecting the necessary components to achieve the desired properties in their integrated circuits.

Analog integrated circuit blocks, including components like analog-to-digital converters, digital-to-analog converters, operational amplifiers, voltage references, voltage comparators, and filters, as well as their sub-parts like differential pairs, current mirrors, and resistance dividers, heavily rely on the electrical performance of basic components. This performance is significantly influenced by the layout of semiconductor devices [2-3]. When there is a discrepancy between the desired value set by the analog circuit front-end designer and the actual value on a specific silicon wafer after the fabrication process, this phenomenon is referred to as parametric mismatch [4].

Parametric mismatch is generally categorized as either random mismatch or systematic mismatch. Random mismatch, often process-dependent, arises from factors such as random dopant fluctuations [5-6], lithography edge roughness [7], or grain boundary effects [8-9]. It impacts key component properties like threshold voltage (V_{th}), mobility F(μ), and gate capacitance (C_{ox}). Typically modeled as a Gaussian distribution, random mismatch scales inversely with the square root of the active device area [10]. To halve mismatch, the area must quadruple, presenting a trade-off between area and matching accuracy [11]. This trade-off can conflict with other performance criteria, such as speed, parasitic capacitance, parasitic resistance, and silicon area.

On the other hand, systematic mismatch depends on the position of matched components on a silicon wafer and can be well-understood through the concept of layout environment effects. This category includes effects like lithography and etch effects, such as a well proximity effect (WPE) [12] and topography steps [13], as well as mechanical stress effects like local stress asymmetries and shallow trench isolation (STI) [14]. Systematic variations may reach the same level as random variations, and if a random mismatch is reduced by increasing the area, the systematic mismatch can become dominant [15]. Additionally, increasing the area accentuates the gradient effect of higher orders, emphasizing the need to find optimal solutions that reduce systematic mismatch, especially for higher orders.

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II. STATE-OF-THE-ART

While there are existing methodological proposals [16] aimed at mitigating systematic mismatch, their effectiveness remains limited. The commonly employed approach is the use of a common centroid layout pattern. Unfortunately, this pattern can only reduce linear gradient effects when each device utilizes 2N unit cells [17-18]. Recent research introduces a methodology [19] capable of addressing asymmetrical patterns but is restricted to linear process gradients. To that knowledge, there is currently no deterministic methodology capable of eliminating systematic mismatch for a random number of unit cells. Therefore, it is crucial to develop an algorithm that can identify an appropriate solution based on accurate assessments of the IC layout matched structure [20].

The primary objective of this paper is to present an innovative algorithm for generating IC matched structures that appropriately account for both linear and non-linear gradient parameters [21]. This algorithm relies on the meta-heuristic simulated annealing methodology (SA) [21], which has been improved through the adaptation of its control parameters based on statistical analysis. Additionally, in layouts where a common centroid cannot be achieved, the proposed method can determine the placement that minimizes deviation from an ideal common-centroid arrangement.

Importantly, none of the prior works detail how to configure the control parameters of the modified SA algorithm to reduce computation time for finding the right solution without employing other algorithms. For instance, heuristic algorithms like genetic evolution algorithm, differential evolution algorithm, etc., have not been explored for this purpose in previous research.

III. NEW ALGORITHM

Let's evaluate the arrangement of L instances, where the instances can be MOS transistors, capacitors, resistors, diodes, and other critical components. In this paper, M_1, M_2, …, M_L MOS transistors are considered, where each MOS transistor (M_1, M_2, …, M_L), consists of many N_1, N_2, …, N_L nominal unit elements M_U. All these nominal units are connected in parallel within the IC. Subsequently, each MOS transistor is characterized by the expression:

$$M_i = M_U N_i \quad (1)$$

where i = 1, 2, …, L.

The entire set of MOS transistors units should be laid out in a matrix with a predefined number of rows (*row*) and columns (*clm*). The matrix may not have an ideal aspect ratio due to constraints predetermined by the location on the silicon wafer. For the cases where the total number of unit elements (M_U) is not a multiple of the number of rows and columns, the remaining vacant spaces in the matrix are filled with dummy transistors (M_D).

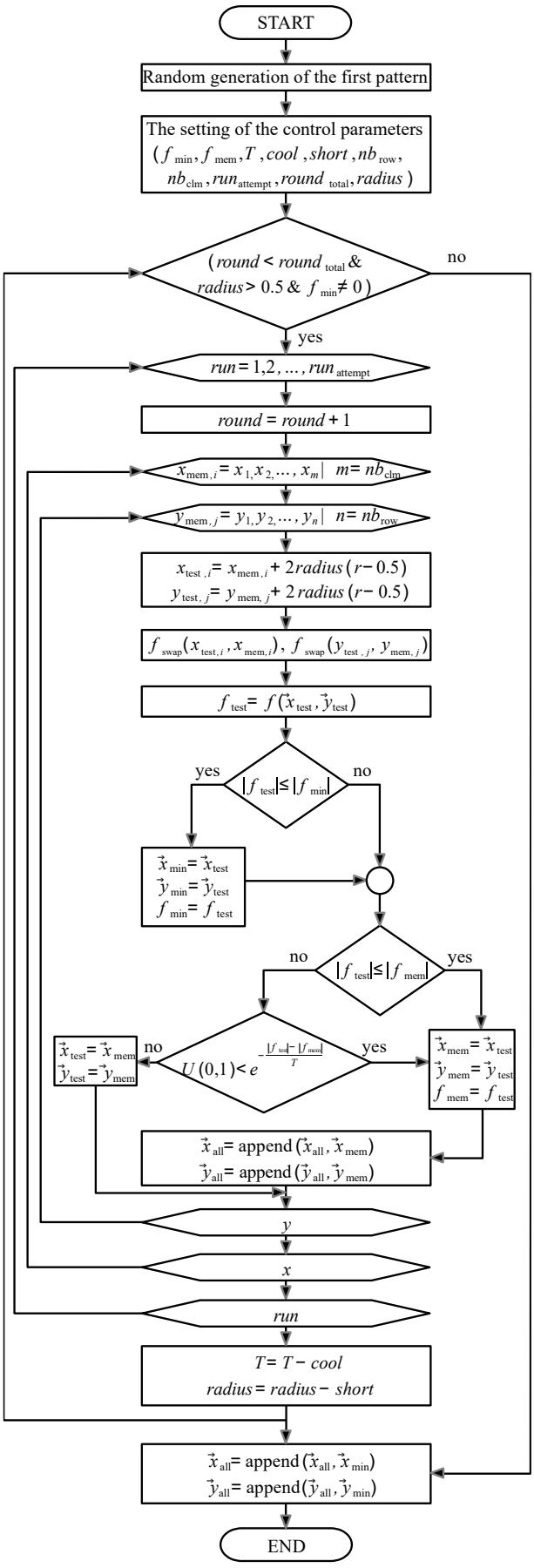


Fig. 1. New algorithm to correctly generate/optimized IC matched structures

The total number of the nominal unit elements that should be properly laid out is given by the expressions (2, 3):

$$M_{\text{U\_Total}} = row \,.\, clm \tag{2}$$

resp.

$$M_{\text{U\_Total}} = \sum_{i=1}^{L}(M_i) + M_{\text{D}} = \sum_{i=1}^{L}(M_{\text{U}}\, N_{\text{i}}) + M_{\text{D}} \tag{3}$$

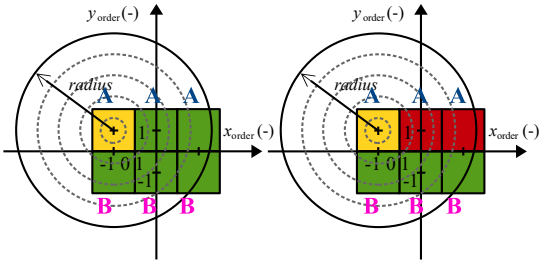
In the initial step of the new modified Simulated Annealing (SA) algorithm, the user specifies the desired number of rows (*row*) and columns (*clm*) for the layout matrix, denoted as "START" (Fig. 1). This step holds significant importance because it determines the aspect ratio of the matched structure on the silicon chip and establishes the count of dummy transistors. Subsequently, the algorithm randomly generates a pattern, a sequence of MOS transistors utilized in the designated matrix. Alternatively, the random generation can be substituted with a non-random arrangement of components, such as common-centroid, interdigitated, cross-coupled, etc. At this stage, we obtain the initial matrix filled with a randomly generated pattern, which will be optimized to achieve the best solution in the shortest time possible.

The input control parameters of the SA algorithm are temperature (*T*), cooling (*C*), temperature stabilization as (run_{attempt}), radius *r* and short *sh*. As the first input control parameter that will be studied is radius *r*.

The radius *r* delineates the exploration area within which the SA algorithm can execute swapping operations. An illustration of the swapping components is provided in the subsequent figures (Fig. 2 and Fig. 3). In the first figure (Fig. 2), the scenario is depicted where the radius *r* from the reference component "A" (highlighted in yellow) encompasses all components. This implies that all components are eligible to participate in the swapping operation, where x_{order} signifies the placement order of instances in the horizontal direction, and y_{order} signifies the placement order in the vertical direction. Determining the initial value of the *r* parameter is crucial, and it is derived as:

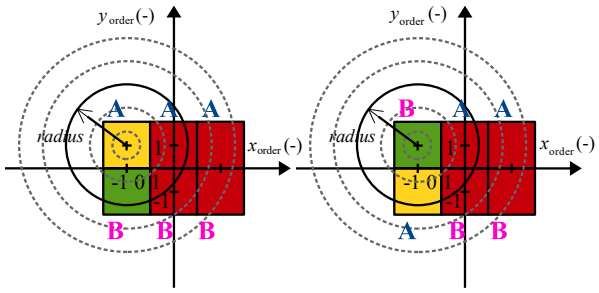
$$r_{max} = \sqrt{x_{\text{range}}^2 + y_{\text{range}}^2} \tag{4}$$

where x_{range} is a range of the instances in the horizontal direction, y_{range} is a range of the instances in the vertical direction.



(a) **(b)**

Fig. 2. The illustration identifies instances eligible for swapping with the reference one (highlighted in yellow) based on the current radius (solid line), where (a) encompasses all possible instances. Subsequently, (b) involves a filtering procedure to prevent self-swapping (highlighted in red), as it is not meaningful and would introduce additional computation time.



(a) **(b)**

Fig. 3. Swapping operation II, (a) before swapping of the selected components (yellow and green colour rectangles), (b) after swapping of the selected components (yellow and green colour rectangles)

In Fig. 3 is shown swapping process of two components on the reduced exploration radius. During the initial round of the new SA algorithm, the radius attains its maximum value as determined by function (4). In subsequent rounds of the algorithm, the radius parameter undergoes reduction by:

$$r_i = r_{i-1} - sh \tag{5}$$

where *sh* is defined as:

$$sh = \frac{r_{\text{max}} - r_{\text{min}}}{\frac{i_{\text{total}}}{run_{\text{attempt}}}} \tag{6}$$

where i_{total} is maximum number of SA iteration, r_{min} is minimal *r* distance ($r_{\text{min}} = 0.5$), run_{attempt} denotes the maximum number of iterations for a specific configuration of the *T* and *C* parameters. The radius value is adjusted when the current run counter equals run_{attempt}, as indicated in Fig. 1.

The shortening process is depicted in Fig. 3, where each round of the SA algorithm (indicated by dotted circles) demonstrates a progressively reduced radius. The solid circle represents the current round of the SA algorithm, while the dotted circles indicate the potential radius parameters for the previous and next rounds. The figure also illustrates a swapping operation in the third round of the SA algorithm. Fig. 3a showcases the situation before the components are swapped, and Fig. 3b illustrates the situation after the swapping of components "A" and "B."

The swapping process follows a specific methodology. In each round of the SA algorithm, one reference component is selected. From this reference component, another component is randomly chosen within the specified range determined by the radius parameter. Subsequently, the algorithm verifies the name difference between the reference and the randomly selected components. If their names are different, the swapping operation is executed.

The two remaining parameters, namely temperature (*T*) and cooling rate (*C*), follow the fundamental principles of the SA algorithm as defined in [21].

IV. Experimental Results and Discussion

To validate the efficacy of the new algorithm, it has undergone testing and comparison across 6 600 distinct test cases, specifically focusing on optimization of the 3rd order of the non-linear gradient of the environment. Patterns were generated from three instances, *A, B, C*, and dummies *D*, with modules ranging from 0 to 10. Various topologies were considered, altering the number of rows from 1 to 6. In each

test case, instance A served as the reference instance. Below are two examples illustrating the final matched patterns for current mirrors (CM) with a high level of matched performance. The ultimate mismatch of threshold voltages for the CM, as defined in [20], is zero microvolts in the first case (Example I) and four microvolts in the second case (Example II). It is very good results as confirmed in [21].

An example I:

- 9x A, 6x B
- 3x rows, 5x columns

A	B	A	B	A
B	A	A	A	B
A	B	A	B	A

Fig. 4. Example I shows the pattern found for the following conditions: 9xA, 6xB, 3x rows and 5x, columns.

An example II:

- 9x A, 3x B, 3x C
- 3x rows, 5x columns

A	C	A	B	A
B	A	A	A	C
A	C	A	B	A

Fig. 5. Example II shows the pattern found for the following conditions: 9xA, 6xB, 3xC, 3x rows and 5x, columns.

This paper introduces an innovative algorithm designed to identify an optimal pattern for critical structures, not solely within the semiconductor development path of integrated circuits but also applicable in scenarios where consistent high performance is demanded across an area. This innovative methodology is highly recommended for a broad range of applications, including positioning discrete components on printed circuit boards.

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