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A waveform engineering approach for class F operation in a class C biased peaking branch of GaN MMIC Doherty power amplifiers

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This paper presents a novel design strategy to enhance the performance of a Doherty Power Amplifier using a nonlinear driver stage in the Peaking branch. To implement a class F harmonic termination for the peaking final stage, a third harmonic voltage component is injected at the input by a driver stage, allowing the phase of the third harmonic current at the output of the final stage to be reversed compared to its normal evolution. This enables a class F design strategy for a class C biased device. The paper details the theoretical foundation of the proposed approach together with a thoroughly experimental verification of its applicability at both device and circuit level. The prototype for X-Band applications is implemented on the 120 nm gate-length GaN-on-SiC technology from WIN Semiconductors. The MMIC delivers over 36 dBm of output power and 40% efficiency at 10 GHz. Additionally, when tested with modulated signals having 10 MHz channel bandwidth and 6 dB Peak-to-Average Power Ratio, the linearity threshold of Adjacent Channel Power Ratio of – 30 dBc is achieved with an average output power exceeding 32 dBm and efficiency greater than 32%.

Wireless communication systems have undergone significant advancements over the past few decades, revolutionizing the way we connect and interact with the world. The ever-growing demand for high-speed internet and seamless connectivity has posed severe challenges to network infrastructures, which must accommodate increasing data rates and reduced latency. In particular, the introduction of technologies such as massive Multiple-Input Multiple-Output (MIMO)[1], beamforming techniques[2,3], and time-varying envelope signals with large Peak-to-Average Power Ratio (PAPR)[4] has triggered extensive research on the critical circuits of transmit/receive modules, with the power amplifier (PA) being especially important[5,6]. High-performance PAs capable of handling large-PAPR signals while maintaining high average efficiency and low distortion is essential for deploying green and sustainable wireless networks[7,8]. Over the years, various PA schemes have been proposed to address these challenges, with the Doherty Power Amplifier (DPA) emerging as one of the most popular choices. Its relatively simple and robust architecture, along with excellent output back-off (OBO) efficiency, makes it highly suitable for today's standard requirements[9,10]. In the last two decades, the DPA has been extensively studied and, since the original concept introduced in [11], numerous innovations have been implemented to adapt and optimize the original scheme for solid state technologies and the stringent demands of upcoming wireless standards[12–18]. To this end, a range of techniques and guidelines based on the DPA operating principle have been proposed to enhance its performance in terms of efficiency[17,19], gain[20], bandwidth[18,21–23], linearity[24–28] and other critical aspects[29–31].

The design strategy proposed in this work aims to enhance the DPA performance, particularly in terms of efficiency, output power and gain, by employing a suitable input-output waveform engineering approach in the Peaking branch. Indeed, while a class C bias for the Peaking device is necessary to keep it off during low power region, it inherently shows some drawbacks with respect to the class AB Carrier device. These include a lower gain and a reduced maximum fundamental current component, often asking for an uneven input splitter and a larger active devices to fully modulate the Carrier load to achieve the targeted Output Back-Off (OBO). These drawbacks lead to a deterioration of the gain and Power-Added Efficiency (PAE) of the overall DPA. The architecture proposed in[32] partially addresses such issues by introducing a driver stage only in the Peaking branch, which allows for a sensible reduction of the active periphery needed and higher gain by unbalancing the

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input splitter towards the Carrier device. However, nothing was said about the nonlinear interaction between driver and final stage and how this crucial aspect can be exploited to further improve the performance of the Peaking branch and thus of the overall DPA.

Considering the well-known mechanisms of harmonics generation in a device as a function of its current conduction angle, it is easy to verify that for a simple class C biased device any output harmonic terminations different from a short circuit can only reduce the achievable performance, due to the in-phase generation of higher harmonics[33]. On the other hand, effective improvements can be achieved if the harmonic impedances at the gate terminal are properly controlled [34,35]. However, input harmonics reach detectable levels only when the signal is strong enough to excite the input nonlinearities, making this strategy unsuitable for maximizing the performance of the Peaking branch throughout the entire Doherty region. Moreover, the use of a second harmonic to control the input voltage as proposed in [34,35], could lead to reliability concerns, as the resulting asymmetrical voltage waveform may approach the gate-to-source junction breakdown. On the other hand, some methods based on the active second harmonic injection at the output of the device have demonstrated their efficacy in a DPA architecture, either using an external source at 2 f_0[36] or reciprocally injecting the component generated by the Carrier and Peaking devices at saturation[37]. To overcome the limitation of having benefits only near the saturation and to avoid the use of an external signal source, the approach proposed here integrates a double-stage Peaking branch, where a class F operation for the class C biased device is achieved by a suitable injection at its input of the third harmonic generated by the nonlinear driver preceding it.

This approach has been validated through the design of a 2-way DPA with 6 dB of OBO in X-Band, adopting the NP12 technology process from WIN Semiconductors (120 nm gate-length GaN-on-SiC). For the Carrier branch, a single stage class F configuration was employed. The good agreement between measurements and simulations confirmed the validity of the proposed method, with the prototype demonstrating strong performance across the frequency range of 9.6–10.4 GHz achieving a peak power of 36 dBm and an efficiency greater than 40% at 10 GHz.

Starting from the preliminary results reported in[38], this contribution provides a detailed description of the theory underlying the proposed approach, its experimental validation at the device level, a step-by-step design strategy for implementing it within a DPA architecture, and a comprehensive experimental characterization of the realized prototype including small-, large-, and modulated-signal performance.

Theoretical foundation for a class F-C device

Referring to the simplified model of the active device reported in Fig. 1, assumed as a voltage-controlled current source (i.e., FET), the following considerations can be made. Moreover, for simplicity and without losing validity, the intrinsic plane is assumed as a reference plane for the following formulation.

When a purely sinusoidal voltage waveform is injected at the input, the drain current waveform is expected to be a truncated sinusoid. Limiting the analysis to the first three harmonics, as typically done in practical high-frequency implementation, the drain current can be expressed as

$$i_D(t) = I_{d,0} + \sum_{n=1}^{n=3} I_{d,n} \cdot \cos(n \cdot \omega t) \tag{1}$$

where the Fourier coefficients $I_{d,n}$ are real numbers and their value depends on the selected bias point[33]. Consequently, each Fourier coefficient of the drain to source voltage waveform ($V_{ds,n}$) can be obtained by multiplying the correspondent impedance, properly synthesised through the matching network at each frequency, i.e.,

$$V_{ds,n} = -Z_n \cdot I_{d,n} \tag{2}$$

where $Z_n = R_n + j \cdot X_n$, with $R_n > 0$ since only passive elements are accounted for in the matching network.

In a class F design strategy, the second harmonic current component is shorted, while the loads at fundamental and third harmonic are synthesized such that the drain voltage waveform, which can be written as

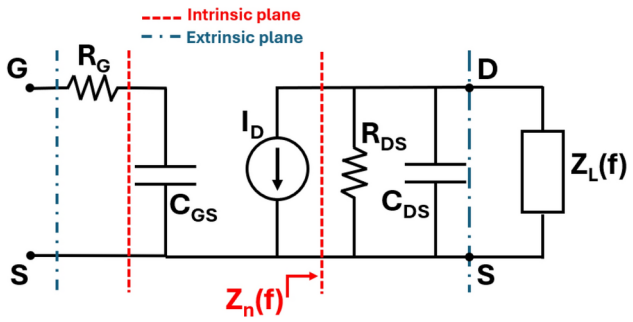


Fig. 1. Simplified representation of an FET, where the intrinsic and the extrinsic plane of the device are highlighted.

$$v_{DS}(t) = V_{DD} - I_{d,1} \cdot |Z_1| \cos(\omega t + \angle Z_1) - I_{d,3} \cdot |Z_3| \cos(3 \cdot \omega t + \angle Z_3) \quad (3)$$

is close to a square wave, where V_{DD} is the drain bias voltage. Moreover, to maximize the performance at a given frequency, both impedances Z_1 and Z_3, at the intrinsic current generator plane, should be purely resistive[33]. However, when considering only passive terminations, this is possible if and only if $I_{d,1}$ and $I_{d,3}$ are opposite in phase, which limits the applicability of the class F approach to devices biased between class B and class A[33]. In contrast, for a class C bias, $I_{d,1}$ and $I_{d,3}$ are both positive, making a class F strategy unsuitable as it would only reduce performance compared to a simple tuned-load harmonic termination (i.e., all harmonics in short circuit). To solve this issue, some approaches based on the synthesis of proper input harmonic terminations to exploit the nonlinearities generated at the gate port of the device have been proposed. However, even if from the one hand an active device biased in class C exhibits strong input nonlinearities, which could be controlled by synthesizing proper terminations to realize a class F configuration, on the other hand such harmonics are significant only when the input signal amplitude is sufficiently high, typically near device saturation. Therefore, the performance benefit of a class F-C design strategy are remarkable only towards the end of the power dynamic, while for lower input power there would be a performance degradation due to the in-phase generation of the third component with respect to the fundamental one. Given that modern wireless communication systems are based on non-constant envelope signals, the PA has to provide significant performance across a wide input dynamic range and not only at saturation. Therefore, summing up these considerations, it is evident that such a strategy is not appropriate for implementing the Peaking branch of a DPA. When the Peaking branch turns on, at the onset of the Doherty region, its input nonlinearities are not strong enough to allow the right harmonic generation at the output, resulting in reduced efficiency and output power over a relevant part of the OBO range.

To address this challenge, a novel approach based on the injection of a third harmonic component directly at the input of the Peaking device through a suitable nonlinear driver is here proposed.

When a third harmonic is present at the device's input, the gate-voltage waveform is no longer purely sinusoidal and can be written as

$$v_{GS}(t) = V_{GG} + V_{GS,1} \cdot [\cos(\omega t) + h_3 \cdot \cos(3\omega t)] \quad (4)$$

where V_{GG} is the gate bias voltage, $V_{GS,1}$ is the amplitude of the fundamental component, and h_3 is the ratio between the third harmonic and the fundamental component $V_{GS,3}/V_{GS,1}$. Now, as graphically reported in Fig. 2, depending on the sign and magnitude of h_3, different gate voltage waveforms can be shaped. In particular, if such a ratio is negative, which means that $V_{GS,1}$ and $V_{GS,3}$ are opposite in phase, the gate voltage becomes similar to a square wave. Consequently, once amplified by the device, it will result in a truncated squared drain current waveform at the output, which owns a third harmonic component opposite in phase with respect to the fundamental one. This enables the implementation of a class F configuration across a device biased in class C for a wider input dynamic range. In practical design of an MMIC DPA, (4) can be satisfied by properly design a nonlinear driver for the device in the final stage of the Peaking branch, also biased in class C. This configuration ensures that the Peaking branch remains inactive during the low power region of the DPA, therefore preserving a significant part of the overall efficiency.

Experimental verification of the theory

Before designing the DPA, the proposed concept was experimentally verified by analyzing the behavior of a 6×100 µm GaN device from the WIN Semiconductors NP12 process. The characterization was performed using a low-frequency large-signal setup[39–41]. The measurements were carried out at a fundamental frequency of f_0 = 2 MHz, allowing the reactive parasitic elements and the intrinsic capacitances of the transistor to be

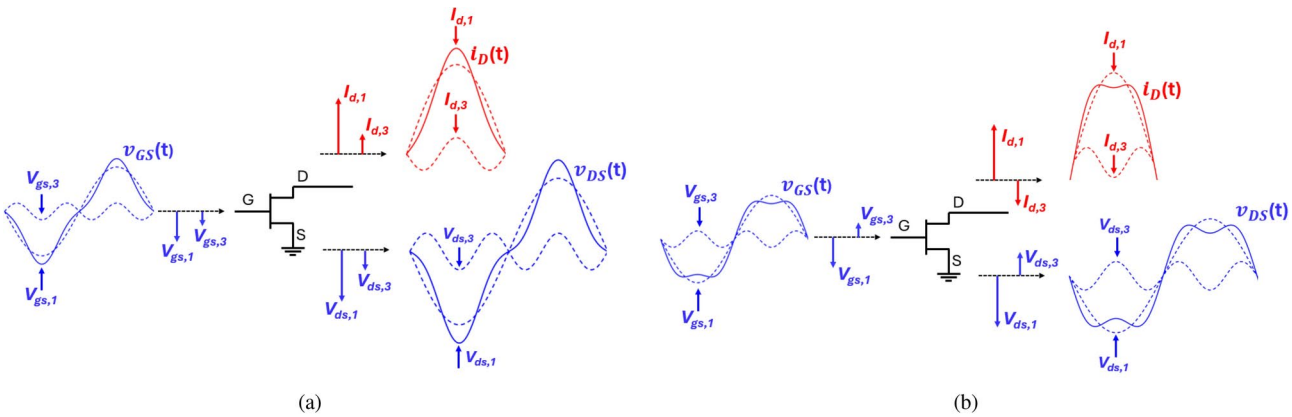


Fig. 2. Graphical representation of the gate-to-source and drain-to-source voltages and drain current waveforms in the case of (**a**) positive and (**b**) negative value of h_3.

neglected. This setup enables direct control and monitoring of voltages and currents at the current-generator plane, where the theoretical analysis was established.

As a first step, a class C tuned-load characterization was carried out. Since the pinch-off voltage of the transistor is − 2 V, the bias condition was set to $V_{GG} = -2.5$ V, V_{DD} = 28 V. The second and third harmonic loads were implemented by passive terminations to be as close as possible to a short circuit (6.6 Ω at $2f_0$ and 6.1 Ω at $3f_0$), whereas the fundamental load was swept to identify the optimum condition for maximum power. The input signal was sinusoidal and different amplitudes were investigated from low power to saturation. The results, reported in Fig. 3, pointed out that R_{opt}^{TL} = 114 Ω is the optimum load, leading to an output power of 34.3 dBm (2.7 W) with 71% drain efficiency for the highest level of input amplitude investigated. Given the optimum load for the tuned-load condition, the class F optimum resistance at f_0 can be estimated as[33]

$$R_{opt}^{F} = 1.15 \cdot R_{opt}^{TL} \tag{5}$$

which results in R_{opt}^{F} = 131 Ω. This condition was investigated under class F operation, i.e., by keeping the 2^{nd} harmonic load close to a short circuit (6.6 Ω) and by setting the 3^{rd} harmonic to a high impedance (480 Ω). The input signal was designed according to (4), by injecting a 3^{rd} harmonic component in addition to the fundamental with the magnitude of h_3 fixed to 0.1. The latter was initially estimated from simulations using the nonlinear model of the 6x100 µm device.

Afterwards, $V_{GS,1}$ and $V_{GS,3}$ were set to 4.1 V (high power), and 0.41 V, respectively, and the phase of h_3 ($\varphi_{G,3}$) was swept from 0° to 360° with a step of 10°. From the results, reported in Fig. 4, it is clear, as suggested by the theoretical analysis (see Fig. 2b), that $\varphi_{G,3}$ = 180° provides the best output power, i.e., 34.9 dBm (3.1 W), with a drain efficiency of 81.3%. This corresponds to a gate voltage waveform flattened on both peaks because of the 3^{rd} harmonic being opposite in phase to the fundamental (Fig. 4b). The load line (Fig. 4c) has the typical shape of class F operation as clearly seen by the drain waveforms (Fig. 4d).

Figure 4 also shows the results for the worst case, i.e., $\varphi_{G,3}$ = 0°, for which the gate voltage waveform is not flattened, thus leading to a non-optimal load line. It is also interesting to observe that, for a given $V_{GS,1}$, an in-phase third harmonic increases the peak of the gate voltage, which can produce a premature forward conduction of the transistor Schottky junction, as clearly visible in the inset of Fig. 4c. The opposite phenomenon is associated with $\varphi_{G,3}$ = 180°, since the out-of-phase 3^{rd} harmonic lowers the peak-to-peak value of the gate voltage for the same $V_{GS,1}$.

The same measurements were repeated for a lower input power, i.e., $V_{GS,1}$ = 2.2 V, $V_{GS,3}$ = 0.22 V. The results are shown in Fig. 5, from which the same considerations can be drawn, suggesting the beneficial impact of the 3^{rd} harmonic injection on a wide power range, as mandatory for a DPA operation.

The measured efficiency improvement with $\varphi_{G,3} = 180°$ of about 5% in Fig. 4a and 4% in Fig. 5a could be considered marginal to justify the slightly higher circuit complexity needed to fulfill such a condition. To clarify this point and thus to demonstrate its relevance in a Doherty architecture, Fig. 6 shows the measured output power and efficiency for three different input power levels, i.e. at $V_{GS,1}$ = 2.2 V (low power), $V_{GS,1}$ = 3.2 V (medium power) and $V_{GS,1}$ = 4.1 V (high power), when the value of h_3 is swept from 0 to 0.4 with a step of 0.02, and its phase is fixed to either $\varphi_{G,3}$ = 180° or $\varphi_{G,3}$ = 0°. Please note that in Fig. 6c the measurement with $\varphi_{G,3}$ = 0° has been limited to $h_3 = 0.22$ because of further increasing h_3 produces a higher voltage peak value, which causes the forward conduction of the Schottky junction, leading to significantly high gate currents that may damage the device, as already shown in the inset of Fig. 4c. On the one hand, these results clearly show that the presence of an out of phase third harmonic increases both features for every input power level, which confirms the theoretical findings. On the other hand, Fig. 6b shows how the efficiency improvement is more visible and remarkable, about 10%, in the medium power region, where the contribution of the Peaking branch in the overall Doherty performance is of primary importance. In the low power region (Figs. 5 and 6a), the current conduction angle is still too low to see either benefits or drawbacks of the injection of an additional third harmonic component, whereas when the device is close to saturation (Figs. 4 and 6a), the drain current waveform is strongly affected by the gain compression and its shape is mainly determined by the output terminations, regardless the input

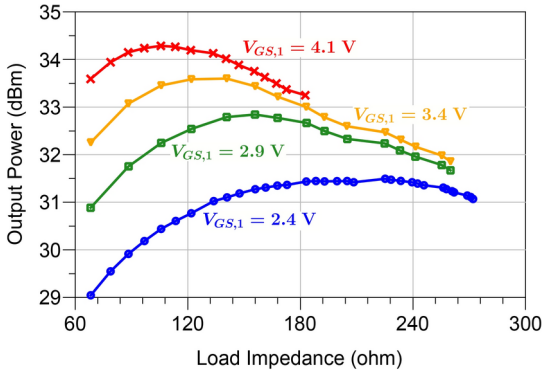


Fig. 3. Output power versus load impedance at fundamental frequency (2 MHz) for bias $V_{GG} = -2.5$ V, $V_{DD} = 28$ V. The input voltage is a sinusoid whose amplitude is indicated in the plot for each curve.

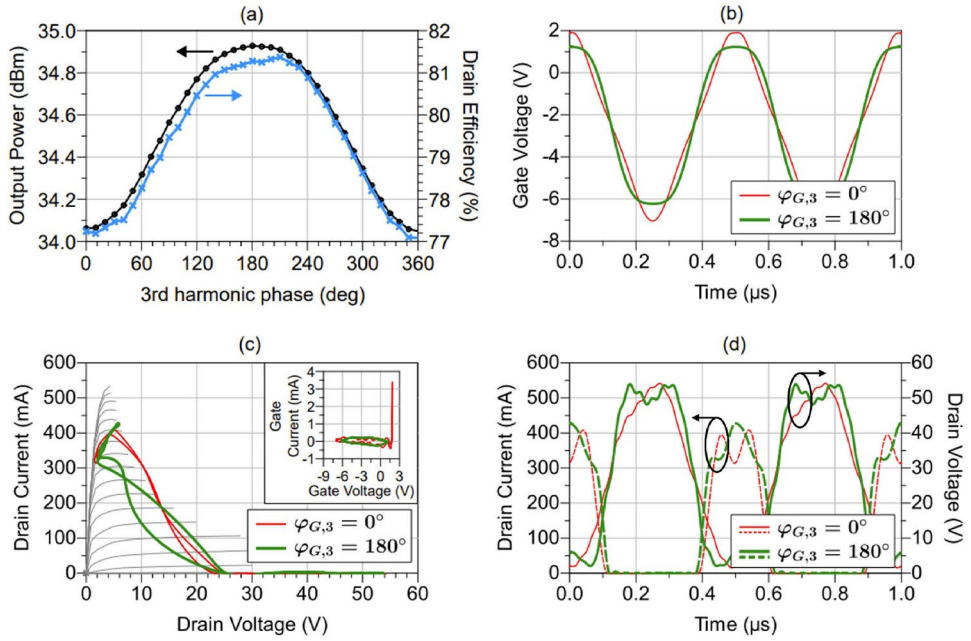


Fig. 4. Results of the input 3^{rd} harmonic phase sweep under class F output terminations at high power. The bias point is $V_{GG} = -2.5$ V, $V_{DD} = 28$ V. The gate voltage has amplitude at fundamental frequency $V_{GS,1}$ = 4.1 V and $h_3 = 0.1$. (**a**) Output power and efficiency vs phase; (**b**) Gate voltage waveform for $\varphi_{G,3} = 0°$ and 180°; (**c**) Load line for $\varphi_{G,3} = 0°$ and 180°; (**d**) Drain waveforms for $\varphi_{G,3} = 0°$ and 180°.

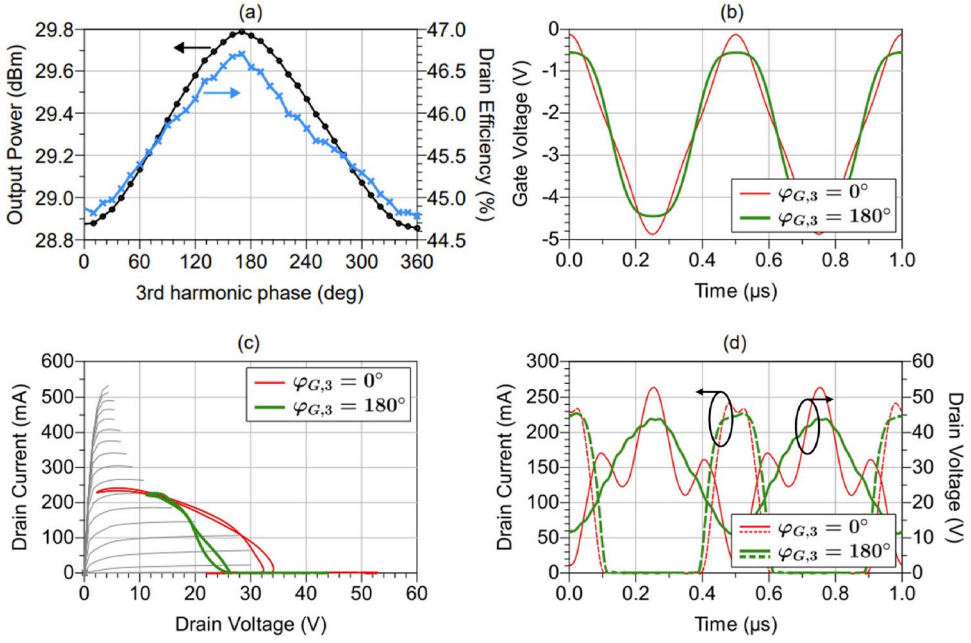


Fig. 5. Results of the input 3^{rd} harmonic phase sweep under class F output terminations at low power. The bias point is $V_{GG} = -2.5$ V, $V_{DD} = 28$ V. The gate voltage has amplitude at fundamental frequency $V_{GS,1}$ = 2.2 V and $h_3 = 0.1$. (**a**) Output power and efficiency vs phase; (**b**) Gate voltage waveform for $\varphi_{G,3} = 0°$ and 180°; (**c**) Load line for $\varphi_{G,3} = 0°$ and 180°; (**d**) Drain waveforms for $\varphi_{G,3} = 0°$ and 180°.

harmonic injection. Despite these factors, an enhancement in both output power and efficiency was obtained across the entire operating range, as summarized in Table 1 for $h_3 = 0.1$.

A similar investigation was carried out also for deeper class-C bias conditions, i.e., $V_{GG} = -3.0$ V, and − 3.5 V, always keeping $V_{DD} = 28$ V. The results showed a behavior similar to the one already discussed, except for the optimum value of the magnitude of h_3, which is higher as the gate bias voltage is lowered. For the sake of

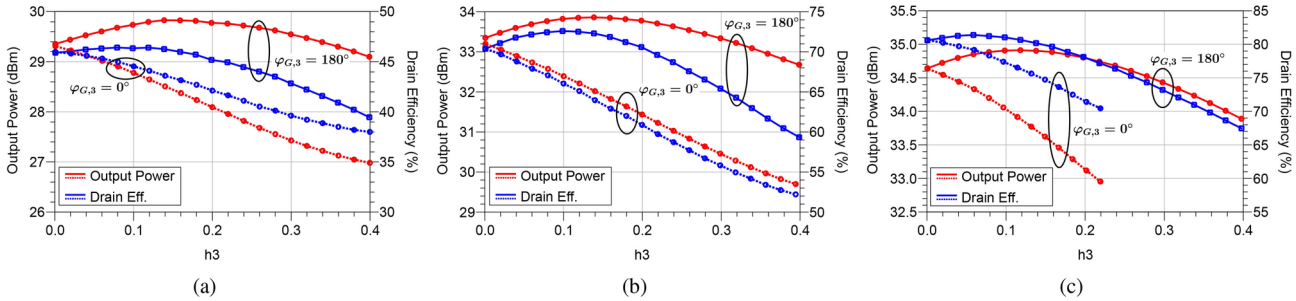


Fig. 6. Output power (red lines) and drain efficiency (blue lines) versus magnitude of h_3 at (**a**) low power ($V_{GS,1}$ = 2.2 V), (**b**) medium power ($V_{GS,1}$ = 3.2 V) and (**c**) high power ($V_{GS,1}$ = 4.1 V), for $\varphi_{G,3}$ = 180° (continuous lines) and $\varphi_{G,3}$ = 0° (dotted lines).

$V_{GS,1}$	h_3	$\varphi_{G,3}$	Output Power	Drain Eff.
4.1 V	0.1	0°	2.57 W	77.2%
4.1 V	0.1	180°	3.09 W	81.3%
3.2 V	0.1	0°	1.74 W	66%
3.2 V	0.1	180°	2.4 W	72.5%
2.2 V	0.1	0°	0.78 W	44.8%
2.2 V	0.1	180°	0.95 W	46.5%

Table 1. Class F-C performance varying $V_{GS,1}$ and $\varphi_{G,3}$.

V_{GG}	R^F_{opt}	$\varphi_{G,3,opt}$	h_3	P^{TL}_{sat}	P^F_{sat}	ΔP_{sat}
−2.5 V	131 Ω	180°	0.12	2.78 W	3.15 W	+ 13.3%
−3 V	131 Ω	180°	0.14	2.70 W	3.12 W	+ 15.6%
−2.5 V	131 Ω	180°	0.16	2.58 W	3.06 W	+ 18.6%

Table 2. Class F-C performance varying V_{GG}.

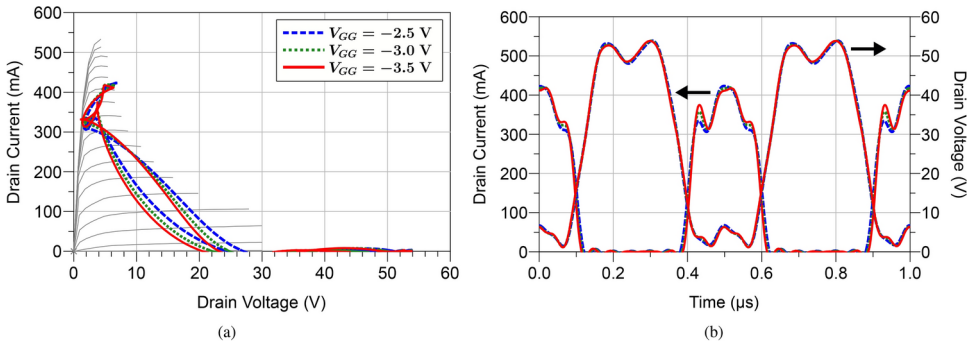


Fig. 7. Measured load lines under class F-C operation for three gate bias voltages: $V_{GG} = -2.5$ V, −3.0 V, and −3.5 V. Input and load terminations are reported in Table 2 for each bias. (**a**) Load lines; (**b**) Drain waveforms.

brevity, not all data are reported, although a brief summary of the performance in all the investigated bias points is reported in Table 2. It is worth mentioning that the optimum load at fundamental, identified by measurements at power levels close to saturation, remains the same in all the selected bias points. As a matter of fact, despite the different gate bias, when operating close to saturation, the self-biasing effect pushes the transistor to operate under similar dynamic conditions, providing similar performance under the same load terminations. This can be observed by looking at the class F-C load lines and waveforms reported in Fig. 7. They were measured considering the conditions reported in Table 2 and using an input power level that drives the transistor close to

saturation. The differences among the different bias conditions are clearly very small, which is consistent with the results reported in Table 2.

Finally, Fig. 8 shows the results of power sweep measurements performed for each V_{GG} under three different conditions:

- Tuned-load terminations with $R_{opt} = 114\,\Omega$.
- Class F terminations with $R_{opt} = 131\,\Omega$ and no harmonic injection i.e., $h_3 = 0$.
- Class F terminations with $R_{opt} = 131\,\Omega$ and harmonic injection with optimum h_3 (see Table 2).

Data are reported in watt to make the difference in performance between the different conditions clearer. The class F-C with the optimum value for h_3 clearly shows the best performance in all bias conditions, providing more output power than the other investigated cases for the entire power range. Focusing on the results for $V_{GG} = -3.5$ V, it can be observed that when $h_3 = 0$ the performance drops to levels lower than the class C tuned-load case. This is the result of the wrong phase relationship between the fundamental and the 3^{rd} harmonic of the drain current waveform, that can be corrected by properly engineering the gate-voltage waveform. It is also interesting to note that, moving V_{GG} towards the transistor threshold voltage, the class F condition with $h_3 = 0$ performs better when compared with the tuned-load class C, towards the saturation. As a matter of fact, by increasing V_{GG} the class B bias condition is approached. This, together with the self-biasing mechanism, leads the transistor to operate under a dynamic nonlinear condition closer to the conventional class F operation, which translates to an improvement of the overall performance.

Prototype design

To validate the proposed theory also at the circuit level, a 2-way DPA with 6 dB of OBO for X-Band applications (from 9.6 to 10.4 GHz) was developed exploiting the 120 nm gate-length GaN-on-SiC technology from WIN Semiconductors. The NP12 process operates at a drain bias voltage of 28 V, with knee and pinch-off voltages of about 5 V and −2 V, respectively. The Carrier branch adopts a single stage class F configuration, while the Peaking branch employs a two-stage architecture. The driver is specifically designed to inject a third harmonic component at the input of the final stage, as previously discussed. This section will provide a detailed, step-by-step discussion of the design.

Peaking amplifier design strategy

The Peaking branch uses a 6 × 100 µm device in the final stage driven by a 2 × 100 µm. The active periphery of the driver was carefully chosen to provide the required input power to saturate the final stage, while providing good efficiency. The 6 × 100 µm device can deliver approximately 33 dBm of saturated output power, which would lead to an overall DPA with about 36 dBm output power, assuming 6 dB OBO. Both devices were made unconditionally stable using a classical lumped network consisting of parallel R-L and series R//C components at the gate. The stability network of the 6 × 100 µm was carefully optimized to maximize the gain within the third harmonic frequency range (i.e., 28.8–31.2 GHz). Unlike typical approaches, the reduction of the losses in this frequency range is mandatory to ensure sufficient margins for achieving the correct h_3 value. The final

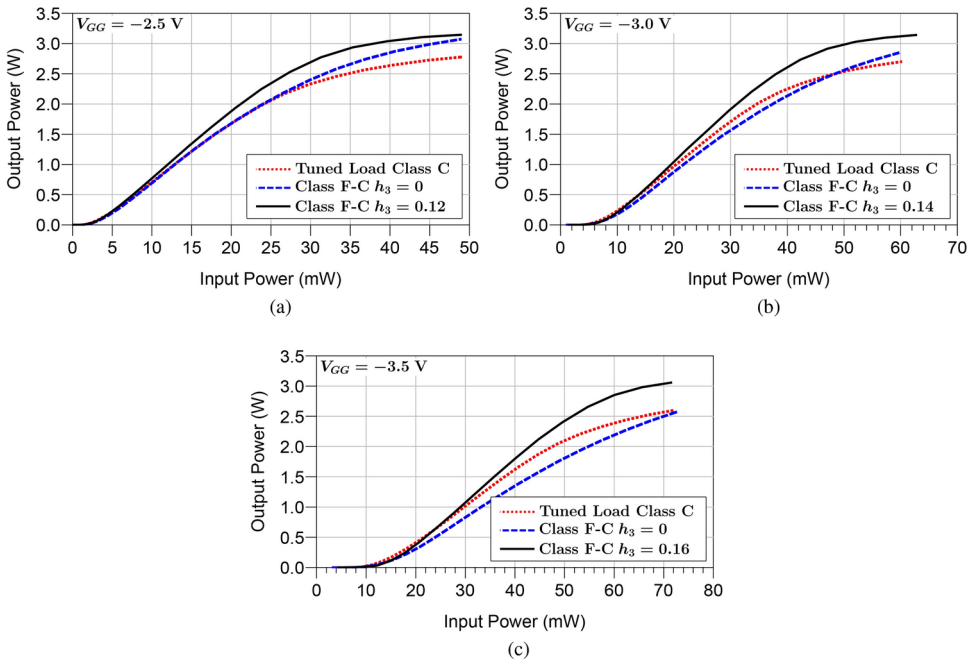


Fig. 8. Measured output power versus input power for the conditions indicated in the legend. Bias is (**a**) $V_{GG} = -2.5$ V (**b**) $V_{GG} = -3.0$ V (**c**) $V_{GG} = -3.5$ V always with $V_{DD} = 28$ V.

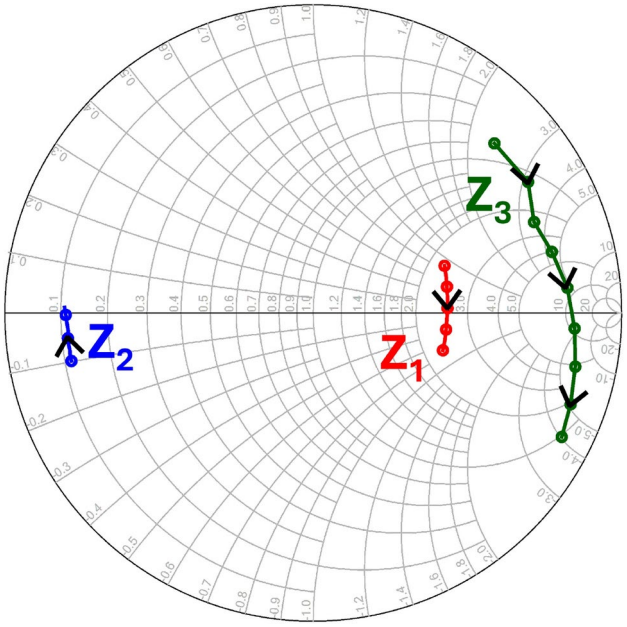


Fig. 9. Synthesised fundamental, second and third harmonic loads at the intrinsic current generator plane of the final stage of the Peaking branch (9.6–10.4 GHz).

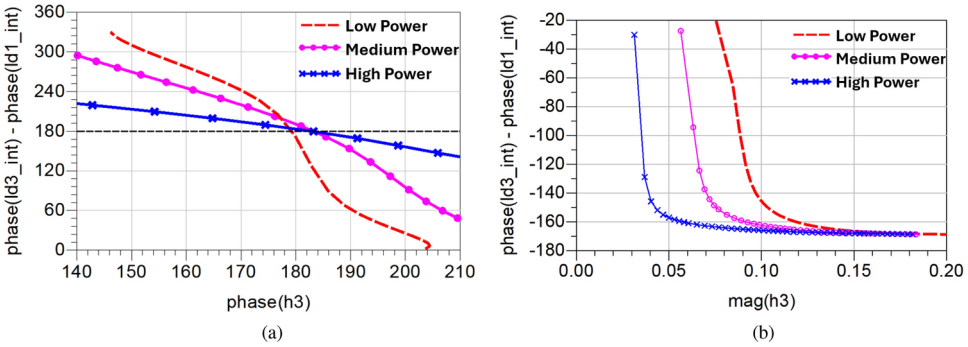


Fig. 10. Identification of the optimal h_3 through a two-tone (10 and 30 GHz) power source at the input of the class C biased 6×100 µm matched and stabilized device. In (**a**), the amplitude of h_3 is fixed to 0.1 and the phase is swept. In (**b**), the phase is fixed at its optimal value to achieve out-of-phase current generation, while the amplitude ratio is swept.

stage operates in class C with $V_{GG,PF} = -2.6\,V$ and its output matching network (OMN) was designed to synthesise, at the intrinsic current generator plane, the class F harmonic termination with an optimum resistance of $R_{OPT} = 131\,\Omega$ at the fundamental frequency. The OMN design was based on a semi-lumped strategy adopting capacitors and short-circuit transmission lines. Figure 9 illustrates the synthesised intrinsic loads on a Smith chart for a fundamental frequency across the frequency range from 9.6 to 10.4 GHz, demonstrating successful class F configuration behaviour.

The design of the driver stage started emulating its behavior using a two-tone power source at fundamental and third harmonic frequencies (i.e., 10 GHz and 30 GHz). Since direct access to the intrinsic gate-to-source plane was not available, the goal was to determine the phase and amplitude relationship between the voltage components at the extrinsic plane to achieve the required out-of-phase relationship between the intrinsic current components $I_{d,1}$ and $I_{d,3}$ for a class F waveform shaping. Initially, the amplitude ratio between the two components was fixed to $h_3 = 0.1$ while the phase was swept. The optimum value to obtain the out-of-phase current components condition was found to be approximately 180°, as shown in Fig. 10a for low, medium and high power values. Then, the phase was fixed and the amplitude ratio was varied, as shown in Fig. 10b for the same power levels. A magnitude of h_3 of about 0.1 was sufficient to achieve an approximately 180° phase shift for every power level, consistently with the results reported in the previous section. It is important to highlight that it is not mandatory to satisfy the 180Â° condition at every design frequency at the extrinsic gate-to-source terminal, but it is crucial to identify the value that causes the phase reversal of the third harmonic component of the drain current at the output to achieve a proper class F working condition. In other words, the phase and

amplitude of h_3 must be determined at the extrinsic plane to compensate for parasitic effects and to ensure the proper generation of the drain current components.

The 2×100 µm device was biased in class C with $V_{GG,PD} = -3.2\,V$, to ensure that the Peaking branch remains off during the DPA's low power region. An interstage matching network (ISMN) was then developed between final and driver stages. This network has to transform the final stage input impedance into the optimum load of the 2×100 µm device at fundamental frequency (i.e., $R_{OPT,D} = 550\,\Omega$, identified through load-pull simulations), to short circuit the second harmonic component and, crucially, to control the third harmonic impedance in order to provide the previously identified optimal h_3. During the synthesis of the ISMN, the amplitude ratio and the phase relationship between the third harmonic and fundamental gate-to-source voltage components at the input of the device in the final stage were monitored in order to achieve the out-of-phase generation of the currents at the output. Figure 11 shows the synthesised loads at both extrinsic and intrinsic current-generator plane of the driver transistor for an available input power of 16 dBm from 9.6 to 10.4 GHz fundamental frequency band. In Fig. 12 the simulated drain voltage and current waveforms, and load lines at the intrinsic current-generator plane of the 6×100 µm device are reported for different input power at 10 GHz, clearly demonstrating a class F working condition. This was accomplished through the out-of-phase generation of the third harmonic drain current (Fig. 12a) obtained with the proper control of the third harmonic gate voltage (Fig. 12b). Notably, the third harmonic voltage component does not lie perfectly in the phase opposition region, since it was measured at the extrinsic plane.

The two stage Peaking branch was finalized by designing an input matching network (IMN) to match it to $50\,\Omega$. The circuit diagram of the final Peaking branch is reported in Fig. 13. Each drain bias stub in the OMN and ISMN is approximately $\lambda/2$ long at $2f_0$ to provide a short circuit condition at the second harmonic. The other elements (i.e., capacitors and transmission lines) are optimized to control the impedances synthesised at fundamental and third harmonic. To quantify the improvement achieved with the proposed design strategy, Fig. 14 shows the performance of the Peaking branch in the class F-C configuration together with those of an analogous architecture, in which no waveform engineering strategies are applied, i.e. a typical tuned-load approach. The circuit topologies of the ISMNs and OMNs are those shown in Fig. 13, where the values of the components are slightly tuned to short circuit the harmonics. The simulated output power, gain and efficiency of the chains are shown in Fig. 14b. A clear improvement is observed over the entire input power range and throughout the targeted band.

Carrier branch design

For the Carrier amplifier, the same 6×100 µm device was adopted. It was biased in class AB ($V_{GG,C} = 1.8\,V$ and $I_D = 30$ mA) and made unconditionally stable by using the same network topology used for the devices in the Peaking branch. A class F design strategy was also adopted to maximize the delivered output power and the efficiency, exploiting the favorable phase relationship between the fundamental and the third current harmonic of the class AB[17]. The OMN was synthesised using the same topology adopted for the Peaking final stage, while the values of the components were slightly tuned to compensate for the different parasitics associated to the different biasing condition. Furthermore, in this case, also the load modulation was carefully verified. Indeed, given the target OBO of 6 dB, the OMN should exhibit, at the intrinsic plane, $2R_{OPT} = 262\,\Omega$ in back-off condition and $R_{OPT} = 131\,\Omega$ at saturation. Unlike the Peaking branch, the Carrier branch did not incorporate a driver stage. Instead, a simple IMN was designed to match the input impedance to $50\,\Omega$.

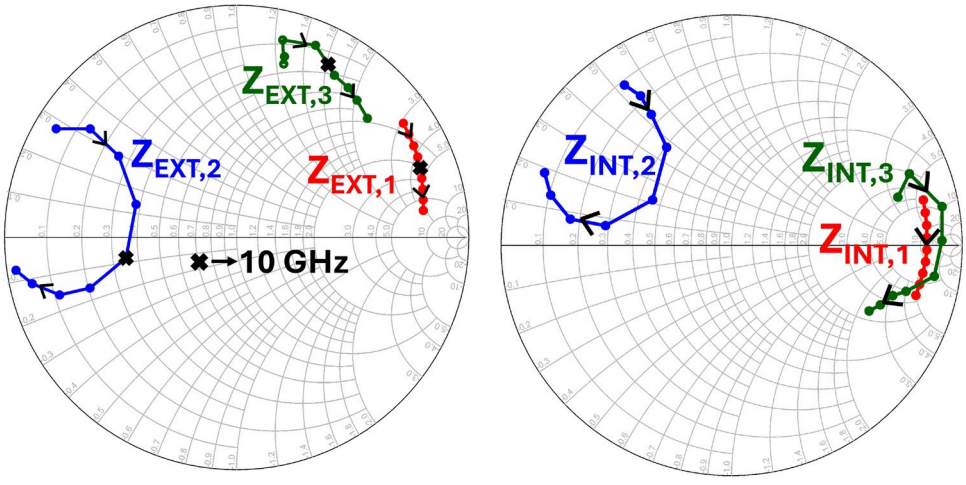


Fig. 11. Synthesised fundamental, second and third harmonic loads at the extrinsic plane (**a**) and at the intrinsic plane (**b**) of the driver stage of the Peaking branch at an available input power of 16 dBm (9.6–10.4 GHz).

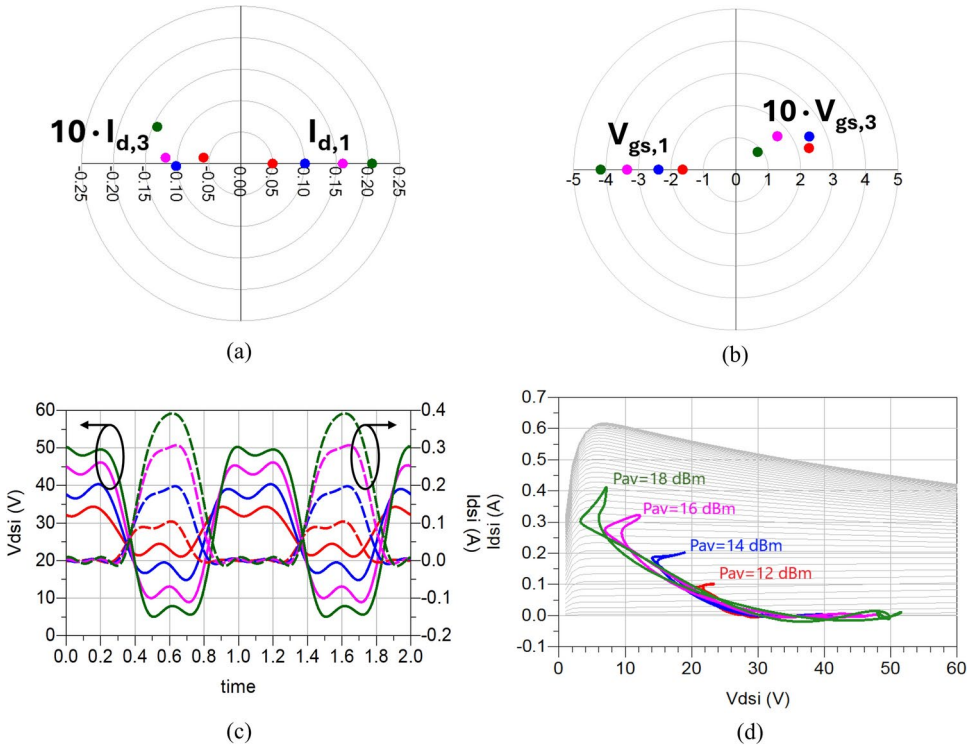


Fig. 12. (**a**) Polar diagram of the drain current components and (**b**) gate voltage components; (**c**) voltage and current waveforms together with the (**d**) loadlines at the intrinsic current generator plane of the device in the Peaking final stage for different values of available input power, demonstrating a class F working condition.

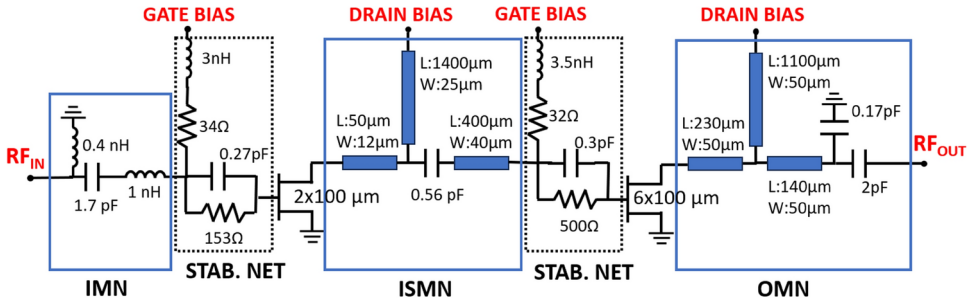


Fig. 13. Schematic of the two stage class F-C Peaking branch.

DPA integration

The Carrier and Peaking branches were combined as shown in Fig. 15.

The output combiner was synthesised adopting the methodology proposed in[42], optimizing the characteristic impedances of the $\lambda/4$ elements to avoid the need of a post-matching network. In particular, fixing the output load to $R_L = 50\,\Omega$ and considering the value of the optimum back-off impedance $2R_{OPT} = 262\,\Omega$ of the Carrier device, the characteristic impedance Z_1 of the first $\lambda/4$ section is given by

$$Z_1 = \sqrt{2R_{OPT} \cdot R_L} \simeq 115\,\Omega \tag{6}$$

Then, accounting for the 6 dB OBO, the values of the other two characteristic impedances can be easily determined. A feasible choice is to fix the characteristic impedance of the $\lambda/4$ number two to $Z_2 = 50\,\Omega$ and calculate the value of the other as

$$Z_3 = \sqrt{R_{opt} \cdot \frac{Z_2^2}{2R_L}} \simeq 58\,\Omega \tag{7}$$

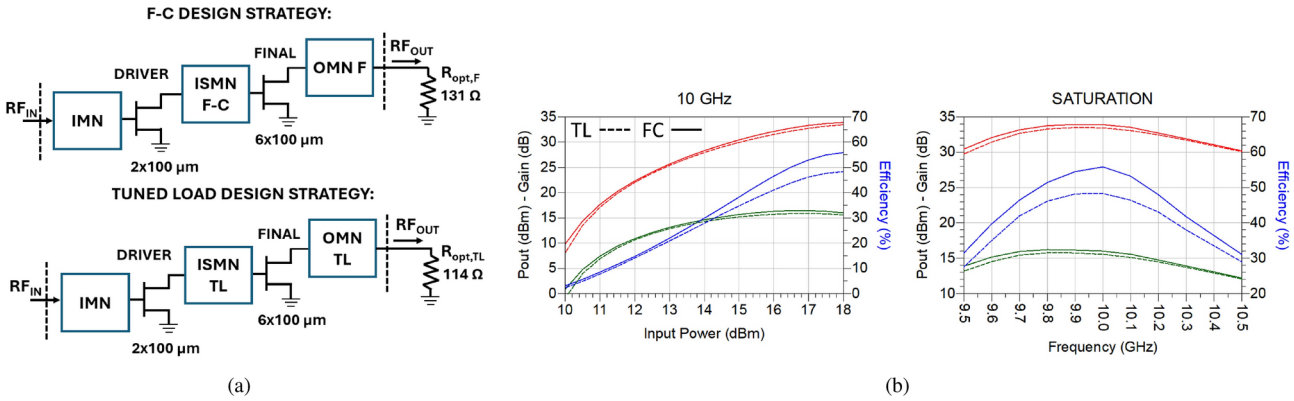


Fig. 14. Class F-C and tuned-load circuit topologies (**a**), and (**b**) performance comparison as a function of the input power at 10 GHz and over frequency at saturation.

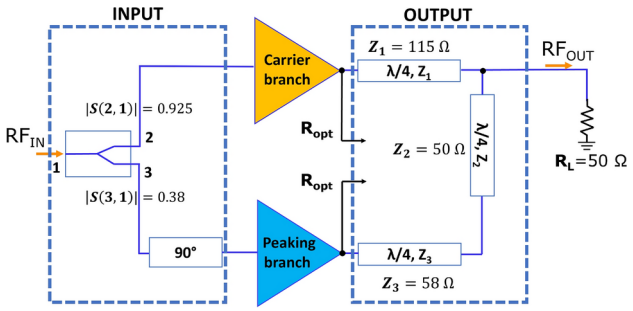


Fig. 15. Simplified scheme of the proposed DPA.

Being the Peaking branch composed of two stages, the uneven input splitter was unbalanced towards the Carrier branch. It was implemented as a branchline coupler to restore the 90° phase shift introduced by the output combiner.

To minimize chip size, the $\lambda/4$ transmission lines in both structures were implemented with lumped elements, using a pi-network composed of one inductor and two shunt capacitors. The value of the components of each Z_i were selected according to:

$$C_i = \frac{1}{2\pi \cdot f_0 \cdot Z_i} \tag{8}$$

$$L_i = \frac{Z_i}{2\pi \cdot f_0} \tag{9}$$

where f_0 is equal to 10 GHz. The final structures of the output combiner and input splitter are shown in Figs. 16a and b, respectively. In the latter case, the characteristic impedances were calculated solving the following system of equations

$$\begin{cases} |S_{21}| = 0.925 = \dfrac{Z_1}{Z_0} \\ |S_{31}| = 0.38 = \dfrac{Z_1}{Z_2} \\ \dfrac{1}{Z_0^2} = \dfrac{1}{Z_1^2} + \dfrac{1}{Z_2^2} \end{cases} \tag{10}$$

resulting in $Z_1 = 46\,\Omega$ and $Z_2 = 122\,\Omega$.

Finally, Fig. 17 shows the microscope photograph of the realized MMIC having a chip area of $3.65 \times 3\ \text{mm}^2$.

Experimental results

The characterization of the fabricated DPA is conducted under nominal bias conditions corresponding to a $V_{\text{DD}} = 28$ V, $V_{\text{GG,DP}} = -3.2$ V, $V_{\text{GG,FP}} = -2.6$ V and $V_{\text{GG,C}} = -1.8$ V.

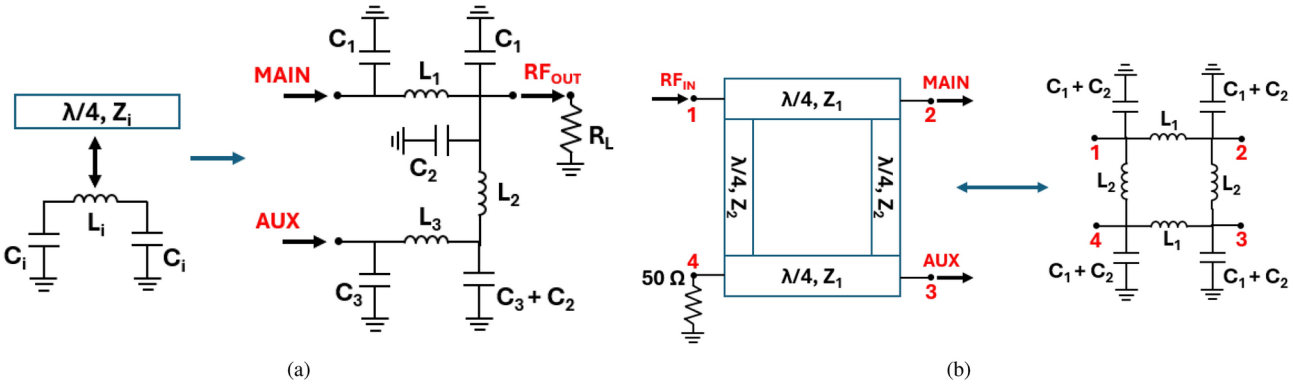


Fig. 16. Schematic of the DPA output combiner (**a**) and scheme of the uneven branch line used as input splitter in the DPA (**b**).

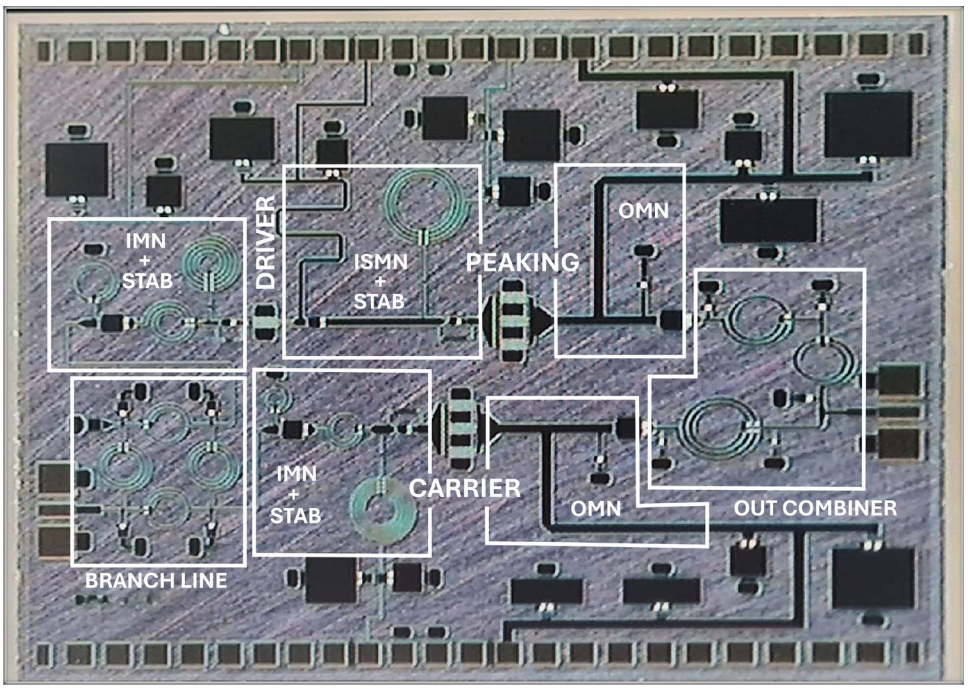


Fig. 17. Photo of the fabricated MMIC DPA (size: 3.65 mm × 3 mm), where each sub-network is highlighted with white boxes.

Small signal performance

Figure 18 shows the comparison between simulated (dashed line) and measured (solid line with symbols) scattering parameters. Notably, there is a good agreement across the frequency range from 0.1 to 20 GHz. The measured small-signal gain is approximately 10 dB at 10 GHz with input and output return losses of about 9.2 dB and 9.3 dB, respectively.

Large signal performance

Figure 19a compares the measured and simulated nonlinear performance of the DPA at the center frequency. The results show good agreement for both output power and gain, though the efficiency is not accurately predicted by the models near saturation. Nonetheless, the measured efficiency is roughly 30% at 6 dB OBO, while at saturation the output power exceeds 36 dBm with an associated gain and efficiency of 9 dB and 40%, respectively. Also, the gain compression is very limited, indicating the proper synchronization of both DPA branches and the correct and complete modulation of the Carrier load. Also, Fig. 19b shows the same features over frequency, both at saturation and 6 dB OBO. At saturation, the output power is slightly below 36 dBm at the upper side of the bandwidth, while efficiency remains above 35%.

A comparison with the actual state-of-art of MMIC DPAs in GaN technology with similar architectures is provided in Fig. 20. The dashed lines represent a linear regression that approximates the performance trend. The

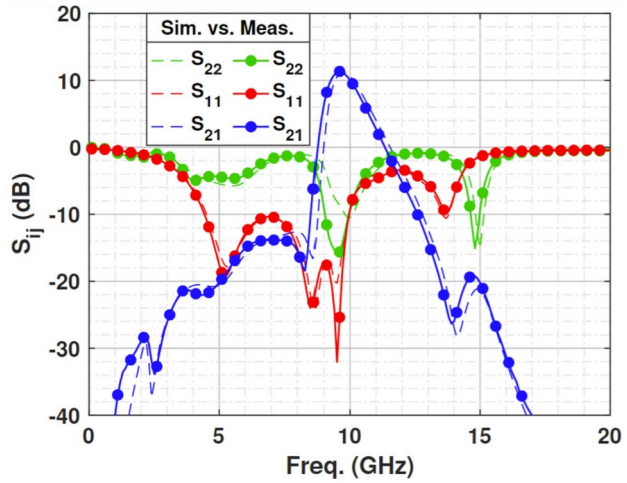


Fig. 18. Comparison between simulated (solid lines) and measured (circle symbols) small signal parameters of the realized DPA from 0.1 to 20 GHz.

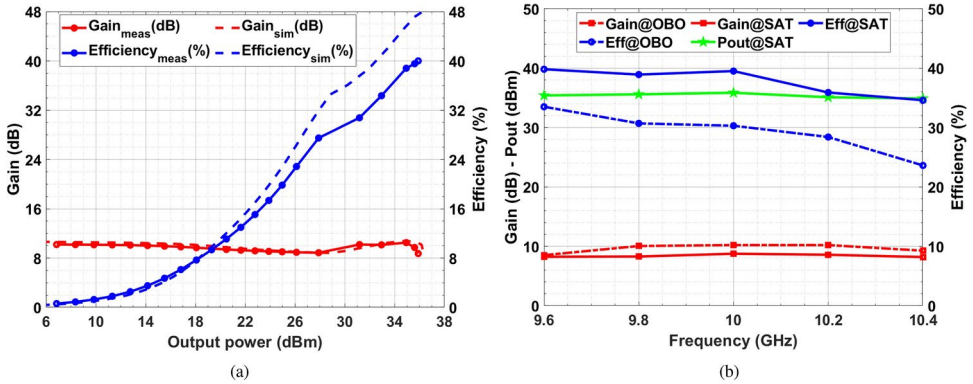


Fig. 19. Measured and simulated efficiency and gain at 10 GHz as a function of the output power (**a**), and measured output power, efficiency and gain over the bandwidth at saturation and 6 dB OBO (**b**).

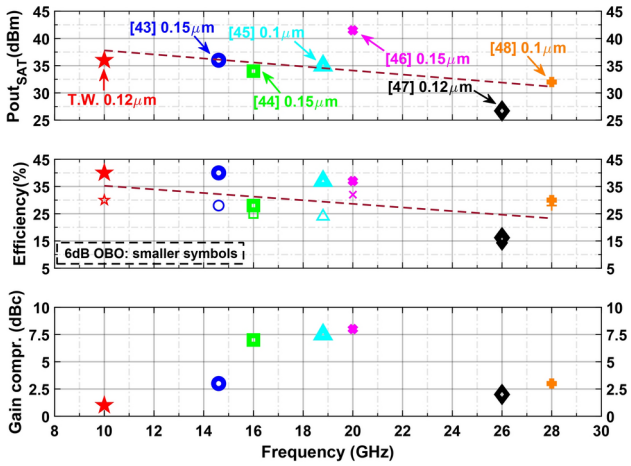


Fig. 20. Comparison with SoA GaN DPAs[43–48].

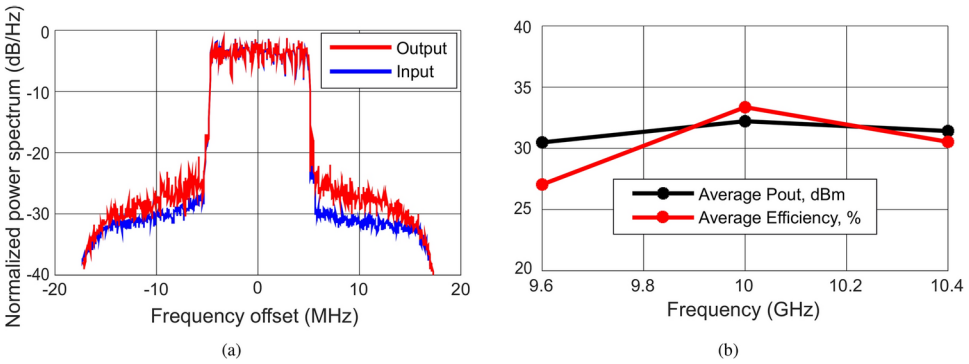


Fig. 21. (**a**) Normalized input (blue) and output (red) power spectra from system level measurements at 10 GHz on the MMIC DPA. Average output power of 31.9 dBm, average efficiency of 32%. Applied baseband signal: 64-QAM, 10-MHz channel, 6-dB PAPR. (**b**) Average output power and efficiency at ACPR of − 30 dBc in the band from 9.6 to 10.4 GHz with a 64 QAM signal with 10-MHz channel bandwidth and approximately 6-dB PAPR.

proposed DPA fits well with both output power and efficiency trends while providing a very limited and not usual gain compression.

System-level characterization

The DPA was tested with a 64 QAM signal with a channel bandwidth of 10 MHz and PAPR of approximately 6 dB. Measurements were performed within the operating bandwidth of 9.6 GHz to 10.4 GHz, without digital pre-distortion. The setup was pre-calibrated using an on-wafer thru to estimate the baseline distortion affecting the measurements, resulting in an ACPR of − 38 dBc.

Figure 21a presents the input (blue) and output (red) normalized power spectra at 10 GHz. The DPA achieved an output ACPR of − 30 dBc, corresponding to an average output power of 31.9 dBm and a remarkable average efficiency of 32%. Similar evaluation across the full DPA bandwidth resulted in an average efficiency always higher than 27% while maintaining ACPR of − 30 dBc, as summarized in Fig. 21b.

Final remarks

The aim of our work was mainly to show the feasibility of the class F-C approach in MMIC GaN DPAs at relatively high frequency. The third-harmonic injection method slightly increases the complexity of the interstage matching network of the Peaking branch, since the third harmonic needs to be controlled in both amplitude and phase at the input of the device of the final stage. Also, the output matching network has to be designed to properly control the third harmonic providing a load near to the open circuit condition at the intrinsic plane of the final stage. Therefore, it could require the use of some additional matching elements that can increase chip area. Nevertheless, the impact on the total chip area with respect to other elements, such as input and output combiner, is not significant since it is relatively simple to merge and arrange components of the matching networks conveniently in the layout. On the other hand, it adds some benefits which easy other critical design issues, such as the need to use a device with larger active periphery in the Peaking final stage with respect to the Carrier one to achieve a correct and full load modulation. Indeed, in this work, two 6×100 µm devices were used as final stage in both Peaking and Carrier branches, achieving the correct and complete load modulation of the Carrier, as demonstrated by measurements. This was possible thanks to the higher output power supplied by the class F-C Peaking branch with respect to the typically adopted tuned-load working mode. In terms of circuit stability, the stability network of the final stage was designed to ensure unconditional stability across all frequencies, with a focus on both the fundamental and third harmonic frequencies. This was achieved paying attention to not compromise the maximum available gain of the device at both fundamental and third harmonic frequencies.

Regarding wide-band scenarios, it is well known that harmonic tuning strategies sometimes can limit the bandwidth of a PA. This limitation arises because resonant matching networks are designed to operate efficiently at specific frequencies, making it challenging to maintain effective harmonic control over a wide bandwidth. However, no specific strategies were implemented to achieve wide-band operation as the individual sub-networks were mainly optimized to operate at center frequency. Thus, probably larger bandwidth can be achieved by slightly sacrificing the performance at center frequency. Anyway, from the comparison between tuned-load and F-C case in Fig. 14, the performance enhancement was achieved throughout the entire frequency range. Concerning multi-band approaches, implementing multi-resonant networks with elements tuned to multiple frequencies can potentially extend harmonic tuning across different bands. However, achieving effective harmonic control across multiple operating frequencies is not easy without compromising performance, and other solutions are maybe preferable, depending on practical implementation constraints.

Conclusion

This paper has presented a design strategy to enhance the performance of the DPA Peaking branch by utilizing the nonlinear interaction between a driver and final stage to create a class F configuration for a class C biased device. The theoretical formulation has been presented together with its experimental verification at both device and circuit level. In particular, the experimental results from the GaN MMIC prototype for X-band applications have shown the potentiality of the proposed approach, achieving a peak of 36 dBm output power, 40% efficiency and 9 dB gain at saturation. With an LTE modulation scheme, the ACPR mark of − 30 dBc was achieved with an average output power around 32 dBm and efficiency greater than 32%, highlighting the intrinsic linearity of the adopted strategy.

Data availability

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

F.M., R.G. and P.C. conceived the idea and designed the DPA prototype, G.B. and V.V. conducted the experimental verification of the theory on the single device, V.C. and A.P. performed the measurements on the fabricated DPA. All authors analyzed the results and contributed to the manuscript.

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Declarations

Competing interests

The authors declare no competing interests.

Additional information

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