Politecnico di Torino

ScuDo
Scuola di Dottorato ~ Doctoral School
WHAT YOU ARE, TAKES YOU FAR

Doctoral Dissertation
Doctoral Program in Computer and Control Engineering (37.th cycle)

Test and diagnosis of memories embedded in Automotive SoCs

Giorgio Insinga

* * * * *

Supervisors
Prof. P.Bernardi, Supervisor
Prof. R. Cantoro Co-supervisor

Politecnico di Torino
March 21, 2025

I hereby declare that, the contents and organisation of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

.....

Giorgio Insinga

Turin, March 21, 2025

Summary

This thesis addresses the critical challenge of ensuring the reliability and testability of embedded memories in Automotive Systems-on-Chips (SoCs), spanning from manufacturing to end-user reliability assessment. With the increasing complexity and safety-critical nature of automotive systems, coupled with shrinking technology nodes, ensuring the robust operation of embedded memories is paramount. This work presents novel methodologies for efficient diagnostic data collection, processing, and retrieval, along with hardware and software solutions for mitigating voltage droop issues and classifying fault shapes.

The starting point of this thesis is the deep characterization of the embedded memories of the Infineon Aurix SoCs produced by Infineon Technologies. In this step, embedded memories are tested under various condition of supply voltage, temperature, read timing etc.

After the characterization step, the challenge of efficiently manage the diagnostic data coming from the test of the embedded memories is tackled. Three on-chip diagnostic data collection methods are proposed and validated on an Infineon Aurix SoC. The first method employs "slices" for lossless failure bitmap encoding, achieving up to 99.8% diagnostic space savings compared to previous list-based methods. The second one further improves the first method by only reporting the differences between one test and the other, further saving 66.99% of diagnostic space. The third one utilizes "pixel slices" for density representation, offering up to 72.6% savings with respect to state-of-the-art lossless approaches, albeit with some loss of information. A novel hardware-software scheme for diagnostic data retrieval reduces test time by 25% and improves fault representation fairness in limited diagnostic memory scenarios. Furthermore, two low-area, low-complexity circuits are presented to mitigate voltage droop during testing, thereby enhancing diagnostic data reliability.

To facilitate advanced fault analysis, a ResNet18-based neural network is implemented to classify eight different fault shapes, outperforming existing approaches and enabling the recognition of novel fault patterns. Finally, this thesis presents software for reconstructing internal memory organization from irradiation test data, allowing end-users to simulate radiation effects and perform accurate reliability assessments. These contributions collectively enhance the testability and reliability of embedded memories in automotive SoCs, paving the way for more robust and dependable automotive systems.