Towards Ultra-Reliable Automotive Systems-on-Chip

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Summary

Nowadays, the automotive industry has witnessed an exponential rise in the number and intricacy of Automotive Systems-on-Chip (SoCs). Proper device testing is crucial to avoiding life-threatening incidents. For this reason, devices must guarantee high reliability, undergoing several testing phases before their sale. However, their increasing complexity poses significant challenges for companies, especially in managing costs and returns from the field.

This thesis has two main research branches: the first focuses on the manufacturing testing phases (pre-sale), while the second focuses on the in-field phase (post-sale) of the device.

For the first research branch, the thesis makes multiple contributions to different phases of manufacturing testing. It first proposes a scan-based test cost model that takes the manufacturing yield and the costs of wafer sort, packaging, and package test as input. The final goal is to address the increasing complexity of devices, which require ever-increasing test costs. Such a model can estimate how many patterns can be cut from the tail of the pattern set during Wafer Sort, thus shifting right some test escapes to the Package Test, while still achieving an overall economic gain. Also, assuming that large devices have non-uniform failure distribution, the proposed methodology analyzes the device layout and a sacrificial lot of devices to extract each fault's layout characteristics and criticality levels. As a further by-product, the thesis shows how generating patterns following the criticalities extracted from the data analysis of sacrificial lots leads to even more significant economic gain.

In addition to scan-based testing, the manufacturing process includes a phase called System-Level Test (SLT), particularly for devices intended for safety-critical

fields. The SLT is introduced just before the Final Test. It aims to cover the faults left uncovered by the structural tests of the previous phases. Precisely, it reproduces the system environment of the device as if it were in its final operation, mainly testing the interconnections between the various modules. The generation of programs for the SLT is done holistically, and evaluating the goodness of these programs is not an easy task, given the extended time of functional fault simulations for very large devices. This thesis proposes a categorization of faults left uncovered by structural testing based on a preliminary analysis of the circuit and the trade-offs made by commercial tools to generate scan-based patterns automatically. This categorization allows for the evaluation and validation of holistically generated SLT programs by verifying their effectiveness in covering those fault categories that are difficult to cover when generating scan-based patterns for the whole circuit. The thesis also explores the application of pseudo-random-generated stress stimuli during the SLT through a low-cost tester architecture.

For the second research branch, the thesis focuses on device life in the field. Considering the problems of returns from the field faced by manufacturing companies, this thesis proposes a logical diagnosis method based on an in-field data collection phase. During its operational life, the device performs key-on and key-off self-tests at different frequencies. The results of these tests are collected within the device's nonvolatile memory. With such collected information, if the device malfunctions and returns to the manufacturing company, it is possible to start from the collected data to more accurately diagnose the failure. The methodology proposed in this thesis is highly adaptable to industrial realities, as it does not involve specific architectures but takes advantage of the self-test modules already present in devices intended for safety-critical fields.

All proposed methodologies are validated using industrial automotive devices produced by STMicroelectronics, as well as production data and failed devices provided by the company.