System-Level Test techniques for Automotive SoCs

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The increasing complexity and heterogeneity of System-on-Chip (SoC) designs, particularly in the automotive domain, pose significant challenges to achieving comprehensive fault coverage during manufacturing testing. While effective at a component level, traditional structural testing methods, such as Scan-Based Testing and Built-In Self-Test (BIST), often fail to fully address faults arising from system-level interactions, particularly in safety-critical applications compliant with ISO 26262 quality standards.

The dissertation explores different key contributions, for the System-Level Test (SLT) phase, at different levels:

- A stress-optimization methodology for SLT that complements structural methods to enhance fault detection in critical non-uniform stressed areas [1];
- Guidelines for developing an SLT suite for testing communication peripherals [2];
- The development of automated SLT workload generation techniques leveraging graph-based SoC abstractions and Device Tree Source (DTS) files, reducing dependency on manual efforts or through genetic frameworks [3], [4];
- Grading methodologies for evaluating SLT effectiveness, using high-level metrics derived from instruction traces [5]–[7] or non functional properties [4], enabling early-stage feedback without requiring exhaustive fault simulation.

The case study is a 40 nm Automotive SoC manufactured by STMicroelectronics, compliant with the ISO 26262 ASIL-D standard. This SoC features approximately 20 million logic gates and around 700,000 flip-flops. It has multiple LBIST partitions (or islands) and Scan Chain Domains. The multicore architecture consists of three 32-bit cores that utilize the PowerPC Variable-Length Encoding (VLE) instruction set. Additionally, it includes 6 MB of Flash memory and 128 KB of general-purpose SRAM, along with several peripheral bridges to access a variety of on-chip and off-chip peripherals. For communication between on-chip components, the SoC is interconnected via two fast crossbar switches, AHB-AMBA version 2.0, operating at 64 bits and functioning up to 200 MHz. These two crossbars are linked by a cross-lake, allowing for the connection of one master from one crossbar to two slaves from the other and vice versa. The SoC also supports various communication peripherals, including CAN, LinFlex, SPI, and FlexRay.

Fault Model	# Faults	Coverage [%]	# Patterns	# Test Escapes
Toggle	ca. 20M	95.89	1k	822,000
Stuck-at	ca. 40M	99.21	69k	316k
Transition Delay	ca. 40M	89.65	82k	4M

TABLE I: Structural tests coverages, number of patterns, and test escapes.

To develop effective SLT workloads and test strategies, information from the RTL, gate-level netlist, and physical layout of the manufactured automotive SoCs are combined. From manufacturing testing, structural tests (including BISTs and scan-based tests) achieve the coverage levels and corresponding number of patterns depicted in Table I [8], [9], and they are the starting point for this PhD thesis.

These contributions collectively advance SLT methodologies, offering scalable, automated, practical, and effective solutions to meet the stringent quality and reliability requirements of modern automotive SoCs, paving the way for broader applications beyond automotive domains, such as high-end processors in data center fleets.

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