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Relaxation Digital-to-Analog Converters Featuring Self-Calibration and Parasitics-Induced Error Suppression in 180-nm CMOS / Rubino, R., Musolino, F., Leite Correia de Toledo, P., Chen, Y., Richelli, A., Crovetti, P.S.. - In: IEEE ACCESS. - ISSN 2169-3536. - ELETTRONICO. - 13:(2025), pp. 6594-6605. [10.1109/ACCESS.2025.3526209]

Availability:
This version is available at: 11583/2997521 since: 2025-02-14T15:30:13Z

Publisher:
Institute of Electrical and Electronics Engineers

Published
DOI:10.1109/ACCESS.2025.3526209

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18 November 2026

IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 22 November 2024, accepted 2 January 2025, date of publication 6 January 2025, date of current version 13 January 2025.

Digital Object Identifier 10.1109/ACCESS.2025.3526209

RESEARCH ARTICLE

Relaxation Digital-to-Analog Converters Featuring Self-Calibration and Parasitics-Induced Error Suppression in 180-nm CMOS

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ABSTRACT The design and the silicon characterization of two mostly digital, low-voltage, energy- and area-efficient Relaxation Digital-to-Analog Converters (ReDACs) in 180 nm featuring digital self-calibration and parasitics-induced error suppression are presented and compared in this paper. The first design is a single-ended ReDAC (SE-ReDAC) and operates at 880 kS/s with a 10-bit resolution, while the second is based on a differential ReDAC (Diff-ReDAC) architecture and operates at 100 kS/s with a 13-bit resolution. The SE-ReDAC testchip in 180nm occupies just 5,030 μ m^2 and operates with a supply voltage ranging from 0.6 V to 1 V. Experimental results at 0.65 V reveal a 72.18 dB-SFDR, a 65.59 dB-THD and a 56.09 dB SINAD, resulting in 9.02 ENOB, with a power dissipation of just 3.3μ W, achieving a competitive energy-efficiency (area-normalized energy efficiency) figure of merit FOM (FOM$_A$) of 166 dB (175 dB). On the other hand, the 180-nm Diff-ReDAC testchip occupies 7,800 μ m^2 and operates in a supply voltage range from 0.45 V to 1 V, while achieving a 77.81 dB-SFDR, a 77.52 dB-THD and a 65.82 dB-SINAD (10.64 ENOB) at 0.6 V supply with a power consumption of just 880 nW, leading to a very competitive FOM (FOM$_A$) of 172 dB (178 dB).

INDEX TERMS D/A converter (DAC), relaxation D/A converter (ReDAC), ultra-low area, digital-based, ultra-low power, ultra-low voltage, Internet of Things (IoT), biosensors.

I. INTRODUCTION

Emerging harvester-powered Internet of Things (IoT) nodes [1], [2] and micrometer-scale biosensors [3] demand extremely compact, low-power, low-cost integrated circuits operating at supply voltages well below 1 V [4].

In this context, Digital-to-Analog (D/A) converters (DACs) with a sub-μ W power budget, an effective resolution in the 10-bit range and a bandwidth from the kHz up to the MHz range are needed in wearable and implantable biosensors for electrochemical impedance spectroscopy (EIS) and cyclic voltammetry [5], [6], [7], [8], [9], [10]. DACs with comparable performance and power budget are required in energy autonomous IoT sensor nodes for on-chip automatic tuning/calibration, audio processing and threshold generation for event detection, among the others [1], [11], [12].

Since these specifications are extremely challenging for traditional analog and mixed-signal (AMS) integrated circuit (IC) design, new digital-based DACs [11], [12], [13], [14], [15], [16], [17], [18], [19] have been proposed in the last years

The associate editor coordinating the review of this manuscript and approving it for publication was Woorham Bae.

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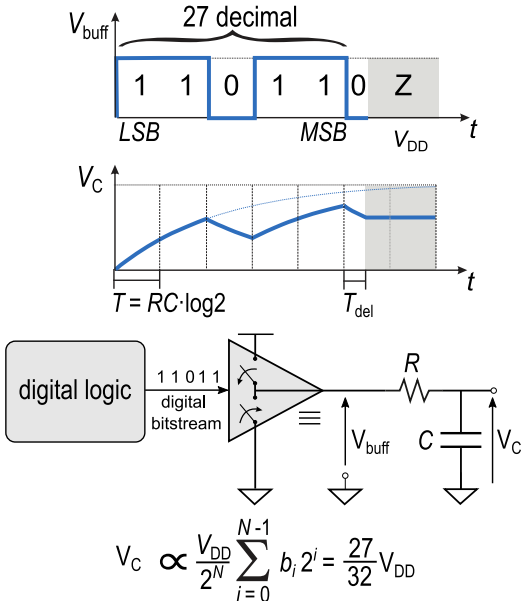


FIGURE 1. ReDAC concept and operating principle.

to address the needs of emerging applications at low cost and design effort.

In this framework, the Relaxation Digital-to-Analog converter (ReDAC) has been introduced in [15] and validated on FPGA and by simulations in 40 nm [20]. From these works, the potential of ReDACs has clearly emerged, even if the early prototypes required impractical manual clock frequency calibration, and their accuracy was severely limited by parasitics. Aiming to address these limitations, a ReDAC self-calibration technique was proposed in [17], but its effectiveness was validated by simulations only, and the ReDAC performance was still limited by parasitics. In [16], a simple parasitics-induced error suppression strategy, which dramatically enhances the ReDAC accuracy, was introduced and demonstrated on an FPGA prototype, which also features automatic clock frequency calibration. Neither the parasitics-induced error suppression nor the automatic calibration, however, have been validated on silicon to date.

In this work, which extends our preliminary conference paper [19], the implementation in 180 nm CMOS of two ReDACs featuring both parasitics-induced error suppression and digital on-chip self-calibration is addressed. The first converter, SE-ReDAC, is based on a single-ended architecture and operates at 880 kS/s with a 10-bit resolution, while the second, Diff-ReDAC, is based on a differential architecture and operates at 100 kS/s targeting a 13-bit resolution.

The rest of the paper is organized as follows: the ReDAC operation is reviewed in Sect. II, while the design of the SE-ReDAC and of the Diff-ReDAC cores are discussed in Sect. III, where the first on-chip implementation of the parasitics-induced error suppression strategy and of the on-chip self-calibration are described in detail. The architecture of the test-chip is introduced in Sect. IV, and the experimental test results are then presented and compared with the state of the art in Sect. V. Some concluding remarks are finally drawn in Sect. VI.

II. THE RELAXATION DAC (REDAC)

The ReDAC operation [15] and the background about ReDAC clock frequency self-calibration and parasitics-induced error suppression [16] are revised in this Section to introduce the silicon implementation presented in this paper.

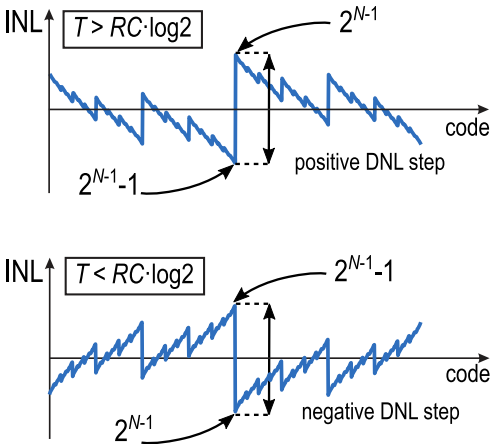


FIGURE 2. ReDAC Integral Non-Linearity (INL) error due to the deviation of the ReDAC clock period T from its nominal value $T^\star = RC \log 2$.

A. REDAC PRINCIPLE

As illustrated in Fig. 1, a ReDAC is made up of a simple three-state digital buffer that drives a first-order low-pass RC network for a period $t \in [0, NT]$ with a stream of N rectangular pulses with equal duration T and amplitude $b_i V_{DD}$, that can be either 0 or V_{DD}, depending on the logical value of the bits $\{b_{N-1} \dots b_0\}$ in the digital input code

$$n = \sum_{i=0}^{N-1} b_i 2^i, \tag{1}$$

streamed out from the LSB, b_0, to the MSB, b_{N-1}.

Assuming a zero initial condition ($v_C(0) = 0\,\text{V}$) and imposing the continuity of v_C at each clock transition, he evolution of the capacitor voltage $v_C(t)$ can be evaluated by first-order transient analysis and its final value $v_C(NT)$ at the end of the conversion can be expressed as [15]

$$v_C(NT) = V_{DD}\left(1 - e^{-\frac{T}{\tau}}\right) \sum_{i=0}^{N-1} b_i e^{-\frac{(N-1-i)T}{\tau}}. \tag{2}$$

If the time constant $\tau = RC$ and the pulse duration T are related to each other so that

$$e^{-\frac{T}{\tau}} = \frac{1}{2} \quad \Longrightarrow \quad T = \tau \log 2 = T^* \tag{3}$$

based on (2), the final capacitor voltage is proportional to the binary value of the digital input code n

$$v_C(NT^*) = \frac{V_{DD}}{2^N}\sum_{i=0}^{N-1} b_i 2^i = \frac{n}{2^N}V_{DD} = V_{DAC}(n), \qquad (4)$$

as expected in a DAC.

B. REDAC CLOCK PERIOD CALIBRATION

When the ReDAC clock period T varies from its nominal value T^*, e.g. because of process, supply voltage and temperature (PVT) variations in the clock source, the ReDAC transfer curve is affected by a nonlinearity error that increases with the clock period deviation $\Delta T = T - T^*$. As a consequence, the condition (3) needs to be enforced by calibration at an accuracy related to the target linearity of the converter.

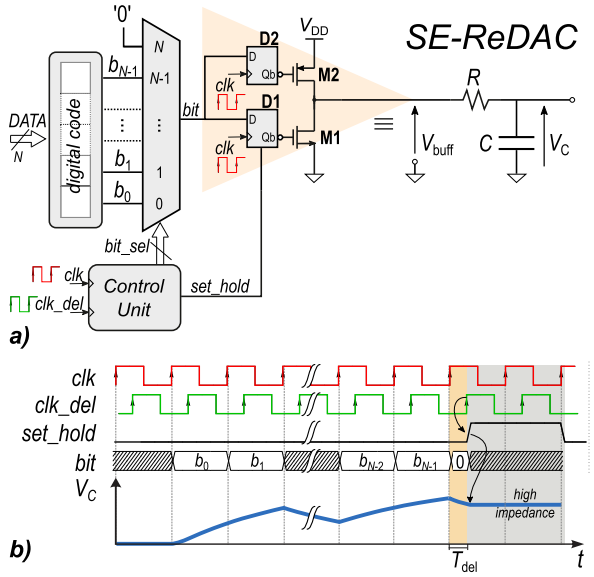


FIGURE 3. Architecture of the proposed SE-ReDAC.

The ReDAC clock period calibration is greatly simplified by the properties of the ΔT-related ReDAC differential nonlinearity (DNL) error highlighted in [16] and illustrated in Fig.2: since the ReDAC DNL is maximum in magnitude at mid-range, it is sufficient to enforce $\Delta V_{DAC} = V_{DAC}(2^{N-1}) - V_{DAC}(2^{N-1}-1) = 0$ at the target resolution to guarantee a DNL below 1 LSB across the whole input range. Moreover, due to the monotonic dependence of the error on ΔT, the condition $\Delta V_{DAC} = 0$ can be enforced tuning the ReDAC clock period based on the sign of ΔV_{DAC} by a binary search algorithm [16], [17], [18].

The calibration approach outlined above has been originally demonstrated in [16] on an FPGA prototype, and its silicon implementation on the SE-ReDAC and Diff-ReDAC prototype will be discussed in Sect.III-D.

C. REDAC NON-IDEALITIES AND PARASITICS ERROR SUPPRESSION

Once the ReDAC clock period is calibrated so as to meet condition (3), the accuracy and performance of a real ReDAC are still limited by parasitics, noise, loading effect in the three-state buffer, finite rise and fall times and leakage currents in the hold phase. Such non-idealities have been shortly analyzed in [16], where it has been highlighted that the errors related to the higher-order time constants introduced by the parasitics of the RC network are by far the more relevant.

The dominant parasitics-induced error, however, can be effectively suppressed driving the three-state buffer low for a short time interval $T_{del} \ll \tau$ before the hold phase, making it possible to achieve a ReDAC effective resolution in the order of 10 bit and more. Such a parasitics-induced error suppression strategy was demonstrated on an FPGA prototype in [16] and its first silicon implementation in the SE-ReDAC and Diff-ReDAC test chips will be introduced in Sect.III-C. The other non-ideal effects will be considered in the design of the same ReDACs in Sect.III, so that to achieve optimal performance.

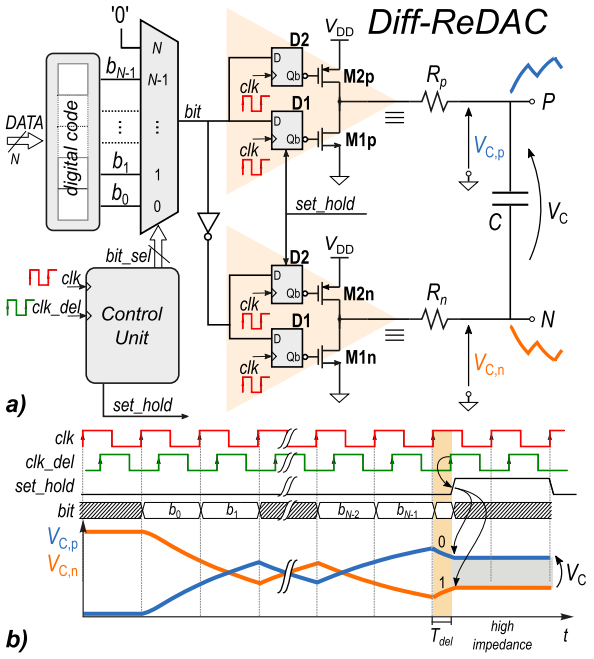


FIGURE 4. Architecture of the proposed Diff-ReDAC.

III. INTEGRATED REDACS DESIGN

The design in 180 nm CMOS of the 10-bit, 880 kS/s SE-ReDAC based on the architecture in Fig. 3 and of the 13-bit, 100 kS/s Diff-ReDAC in Fig. 4 is illustrated in what follows.

A. REDACS ARCHITECTURE

The SE-ReDAC architecture in Fig. 3 closely resembles the block diagram in Fig.1, in which the three-state buffer M1-M2 is driven by two D-flip flops (DFFs). On the other

hand, the Diff-ReDAC is based on the architecture in Fig.4, which entails an output stage made up of two three-state buffers (Buff_p and Buff_n) that drive a floating RC network ($R_\text{p} = R_\text{n} = R/2$ and C). The buffer Buff_p (Buff_n) is driven with the input code bitstream ($b_{N-1} \dots b_0$) (the complemented bitstream ($\bar{b}_{N-1} \dots \bar{b}_0$)) by the DFFs D1_p, D2_p (D1_n, D2_n). After the MSB is processed, the DAC output $V_\text{DAC} = v_{C,\text{p}}(NT^*) - v_{C,\text{n}}(NT^*) = v_C(NT^*)$ is

$$V_\text{DAC} = 2\frac{n}{2^N}V_\text{DD} - V_\text{DD} \tag{5}$$

and its value is hold across the capacitor by operating Buff_p (Buff_n) in high impedance.

B. RC NETWORK AND BUFFER DESIGN

In both ReDACs, the integrated RC network has been designed using high-resistivity polysilicon resistors (RHiPo) in view of their superior linearity, good stability over temperature and high sheet resistance. Similarly, Metal-Insulator-Metal (MIM) capacitors have been chosen in consideration of their linearity, low thermal drift and high specific capacitance.

Since the ReDAC energy per conversion, which can be expressed as a function of the digital code n as:

$$E(n) = CV_\text{DD}^2 \sum_{i=0}^{N-1} b_i \sum_{j=0}^{i} 2^{j-i}(b_j - b_{j-1}) \qquad b_{-1} \triangleq 0. \tag{6}$$

scales linearly with the capacitance C and quadratically with the supply voltage V_DD, the ReDACs have been designed to operate at the lowest supply voltage compatible with the operation of the logic at the target sample rate, i.e.: 0.6 V for the SE-ReDAC, to allow operation at 880 kS/S and 0.4 V for the Diff-ReDAC, to allow operation at 100 kS/s.

Since the ReDAC accuracy is decided by the ratio T/τ and is independent of matching, both area and power are minimized reducing the capacitance C close to the thermal noise limit [15]. In consideration of that, the capacitance C of both the ReDACs has been designed to make the thermal noise power contribution $\kappa T/C$ negligible compared to the quantization noise power $V_\text{DD}^2/(12 \cdot 2^{2N})$ for the target N-bit resolution and at the minimum supply voltage.

Applying this criterium to our design, a capacitance of $C = 900$ fF ($C = 2.6$ pF) is chosen in the SE-ReDAC (Diff-ReDAC) to achieve a 10-bit resolution (a 13 bit resolution).

Once the capacitance C is fixed, the resistance R of the RC network is designed in consideration of the time constant needed to meet the ReDAC condition (3) at the target sample rate $F_\text{conv} = 1/T_\text{conv}$, i.e. imposing

$$T_\text{conv} = (N + K)T^* = (N + K)\tau \log 2 \tag{7}$$

in which N are the clock cycles required for the conversion and $K = 3$ are the extra cycles needed for parasitics-induced error suppression and for the hold phase. In the SE-ReDAC, since $N = 10$, imposing a $880\,\text{kS/s} = T_\text{conv}^{-1}$ sample rate, a time constant $\tau = 126$ ns and hence a resistance $R = 140\,\text{k}\Omega$ are derived from (7). By a similar approach, a resistance $R = 360\,\text{k}\Omega$ is obtained for the Diff-ReDAC imposing a 100 kS/s sample time. Such a resistance has been split into two identical resistors $R_\text{p} = R_\text{n} = R/2 = 180\,\text{k}\Omega$ connected at the non-inverting and inverting outputs for symmetry.

The strength of the output buffer has been optimized based on simulations so that to keep the DNL degradation due to the non-linearity in their ON drain-source resistance below 1 LSB. For the SE-ReDAC, this condition is met with an nMOS (pMOS) aspect ratio of $3.3\,\mu\text{m}/0.18\,\mu\text{m}$ ($6.6\,\mu\text{m}/0.18\,\mu\text{m}$). In the Diff-ReDAC, two output buffers driven by complementary signals are introduced for differential operation and their transistors M1_p M2_p, M1_n M2_n have been designed with an equal aspect ratios of $5\,\mu\text{m}/0.18\,\mu\text{m}$.

C. DIGITAL DESIGN AND PARASITICS-INDUCED ERROR SUPPRESSION

The operations of the SE-ReDAC and Diff-ReDAC are orchestrated by a digital control unit, so as to drive the three-state output buffer(s) with the timing requested for the conversion and for suppressing the parasitics-induced error, as discussed in Sect.II-C. In details, the SE-ReDAC and Diff-ReDAC digital core timing diagrams are shown in Fig. 3b and in Fig. 4b, respectively. The control unit has been synthesized and laid out in a standard-cell digital flow, starting from a behavioral description in Very high speed integrated circuits Hardware Description Language (VHDL).

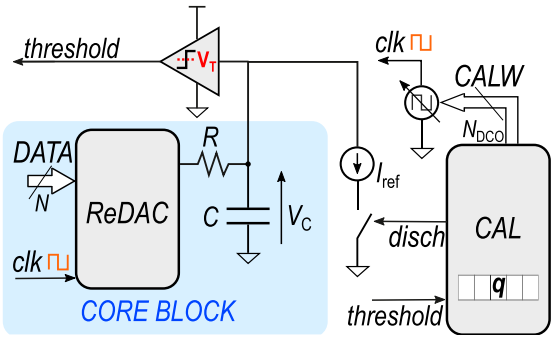


FIGURE 5. Calibration network architecture.

Compared to previous ReDACs [15], [16], [17], [18], in which a shift register was employed to serialize the input bits, in the SE-ReDAC and Diff-ReDAC cells presented in this paper the input code is sampled from the DATA bus and stored in a register, and its bits are streamed out in sequence, LSB-first, by a multiplexer (MUX) driven by the Control Unit. This results in a lower switching activity and hence in a reduced power consumption. For the same purpose, the Control Unit finite state machine is hard-coded as a Gray counter rather than as a binary counter.

To implement the parasitic error suppression technique described in Sect.II-C, the gates of the output buffer are driven by the standard-cell DFFs D1 and D2 operated at $f_\text{clk} = 1/T$, that are synchronously preset at the end of the conversion on

the rising edge of the clock signal, and then asynchronously reset at the rising edge of a delayed clock signal *clk_del*, so as to turn on the pull-down transistor of the output buffer for a time $T_{\rm del} \ll T$ after the end of the conversion, and then set the three-state buffer in high impedance for the hold phase (see timing diagrams in Fig. 3b and Fig. 4b).

D. CALIBRATION

The self-calibration block (CAL) in Fig.5 is designed to tune the frequency of the clock, which is generated by a digitally-controlled oscillator (DCO) based on the sign of the difference $\Delta V_{\rm DAC} = V_{\rm DAC}(2^{N-1}) - V_{\rm DAC}(2^{N-1}-1)$ so as to implement the calibration procedure described in Sect.II-B and to enforce the linear operation condition (3).

In details, the calibration network includes a current sink driven by a pW-power reference [26], that can be enabled by the *disch* control signal to discharge the ReDAC output capacitance during the hold phase, a voltage comparator with threshold $V_{\rm T}$, implemented as a CMOS inverter with power gating, and an up/down counter. All the calibration blocks are driven by the calibration control unit as illustrated in the flow chart in Fig.6 and described below.

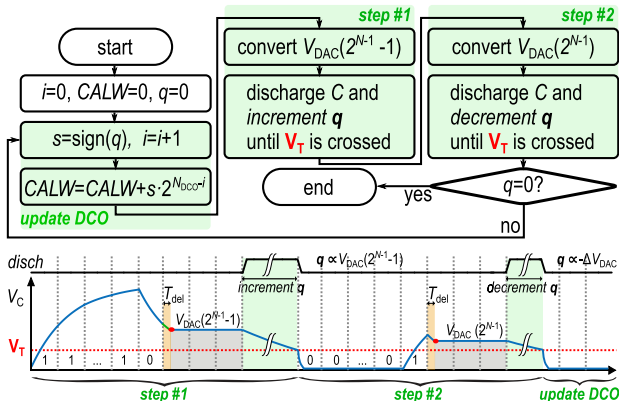


FIGURE 6. Calibration flowchart and timing diagram.

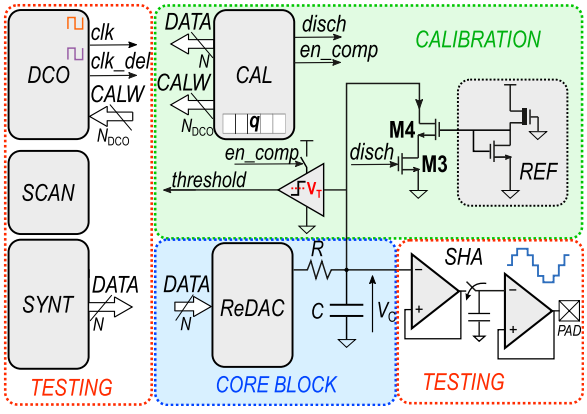


FIGURE 7. ReDAC Test-Chip architecture.

At the system reset, the $N_{\rm DCO} = 11$ bit tentative calibration word *CALW* is set to $2^{N_{\rm DCO}-1}$ to make the DCO oscillate at the center frequency of its tuning range. In the first calibration step, the ReDAC converts $V_{\rm DAC}(2^{N-1}-1)$. Then, during the hold phase the current sink is enabled to discharge the output capacitor at constant current till it crosses the comparator threshold $V_{\rm T}$ (see timing diagram in Fig.6). During the discharge, the counter q is set in up-count mode, and is incremented at each clock active edge so as to digitize the discharge time, as in a time-to-digital converter (TDC). In the second step, $V_{\rm DAC}(2^{N-1})$ is converted and the capacitor is then discharged decrementing the counter q until $V_{\rm T}$ is crossed. The sign of the counter word q at the end of one calibration cycle is therefore equal to the sign of $-\Delta V_{\rm DAC}$ and $-\Delta T$, neglecting the counter quantization and the comparator noise. If $q = 0$, the ReDAC condition (3) is met within 1 LSB and the calibration is terminated. On the other hand, if $q \neq 0$ the calibration word $CALW \propto T$ is dichotomically increased (decreased) by a successive-approximation-register (SAR) logic if $q > 0$ ($q < 0$), and a new calibration cycle begins.

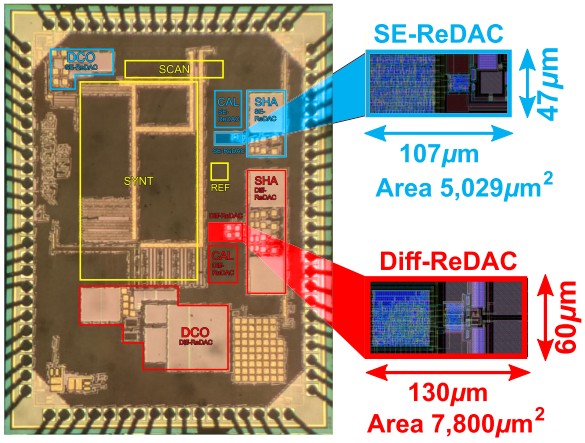


FIGURE 8. Chip micrograph.

TABLE 1. Area of SE-ReDAC and Diff-ReDAC cores and ancillary blocks in the 180 nm test chip in Fig.8.

SE-ReDAC			
Block	Area (μm^2)	Block	Area (μm^2)
Core	5,029	CAL	24,800
DCO	38,800	SHA	46,130
Diff-ReDAC			
Block	Area (μm^2)	Block	Area (μm^2)
Core	7,800	CAL	24,800
DCO	188,600	SHA	92,260
Other blocks			
Block	Area (μm^2)	Block	Area (μm^2)
SYNT	540,000	SCAN	37,600
REF	7,400		

IV. TEST-CHIP ARCHITECTURE

The SE-ReDAC and the Diff-ReDAC presented in this paper have been integrated in a 180 nm ReDAC test-chip whose block diagram is shown in Fig.7 and whose micrograph is

reported in Fig. 8. The SE-ReDAC (Diff-ReDAC) area is only $5,030\,\mu m^2$ ($7,800\,\mu m^2$).

As shown in Fig. 7, the architecture of the test-chip entails the SE-ReDAC and the Diff-ReDAC core blocks along with their digital Calibration (CAL) units described in Sect.III and other ancillary blocks which are needed for testing, namely: a Sample-and-Hold Amplifier (SHA), to provide a low-impedance output suitable to drive external testing instruments, and a Digitally Controlled Oscillator (DCO) to generate the ReDAC clock signal and tune it depending on the digital calibration word from the CAL block, and a Direct Digital Synthesizer (SYNT) [21], to generate the digital input patterns needed for the static and dynamic characterization of the ReDAC. Finally, a Scan-chain (SCAN) interface is introduced to externally control and configure all the blocks. The silicon area occupied by each single block is reported in Tab.1

A. SAMPLE AND HOLD AMPLIFIER (SHA)

The SHAs are based on the standard architecture in Fig.9, which features two operational amplifiers (opamps) in the voltage follower configuration (schematic in Fig.10), a pass gate and a sampling capacitor $C_{SH} = 30\,pF$.

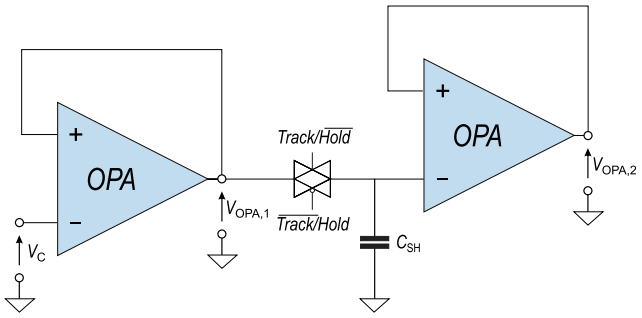


FIGURE 9. Sample-and-Hold Amplifier (SHA).

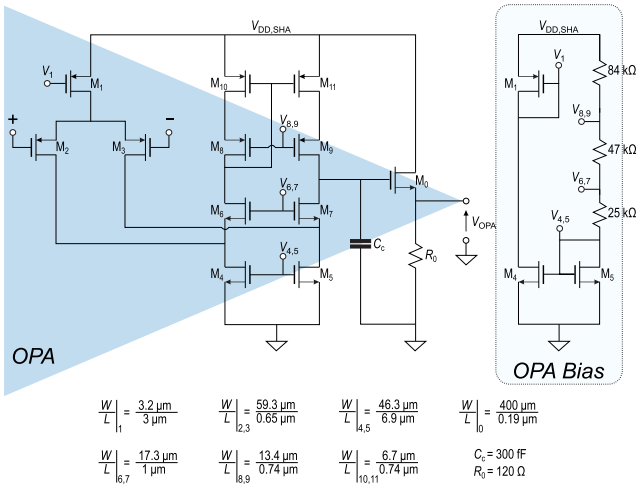


FIGURE 10. Schematic of the Folded Cascode amplifier employed in the Sample-and-Hold Amplifier.

For the SE-ReDAC, the SHA input is connected to the ReDAC capacitor to probe the voltage V_C, while the SHA output $V_{OPA,2}$ is connected to an analog output pad. The SHA is operated by the ReDAC control logic, which provides the $Track/\overline{Hold}$ signal to drive the pass-gate. In the Diff-ReDAC, two identical SHA blocks operated by the same $Track/\overline{Hold}$ signal are adopted for the positive and negative outputs.

The opamps in the SHAs are based on the folded cascode topology and have been designed to drive an output capacitive load up to 50 pF and to achieve a Gain-Bandwidth (GBW) product of 26 MHz, a slew-rate exceeding $18\,V/\mu s$, a 80 dB open-loop DC-gain and a total harmonic distortion (THD) of less than 0.01%, as demanded to settle within the ReDAC clock cycle with a DC accuracy exceeding 13 bit over the whole ReDAC output swing.

The op-amp performance are verified by post-layout simulations under process variations and mismatch, resulting in a 3σ spread of the DC-gain (GBW) of 2.1 dB (4.7 MHz) for process, and 0.2 dB (0.6 MHz) under mismatch.

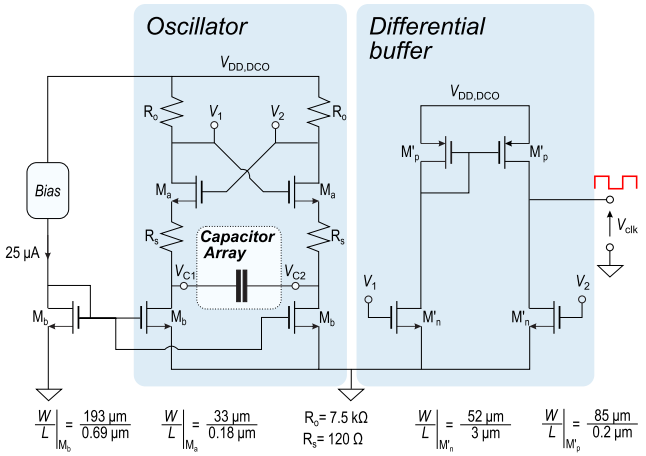


FIGURE 11. Schematic of the digitally controlled oscillator (DCO).

B. DIGITALLY CONTROLLED OSCILLATOR (DCO)

Unlike in [17], a DCO rather than a Voltage Controlled Oscillator (VCO) is adopted in this work. Even if this solution is much more area- and power-consuming compared to the VCOs, it has been chosen in our test chip to inherently avoid clock frequency variations due to leakage currents in the hold capacitor which stores the VCO analog control voltage in [17], and hence to suppress their effects on the ReDACs performance.

The DCOs adopted in the SE-ReDAC and in the Diff-ReDAC are based on the relaxation oscillator topology in Fig.12 with binary weighted capacitors driven by the calibration signals from the CAL blocks as demanded to tune the ReDACs clock frequency to enforce (3) with a resolution finer than the target ReDAC accuracy (11-bit for the SE-ReDAC, 13-bit for Diff-ReDAC). The DCO blocks

also generate the delayed clock *clk_del*, needed to implement the parasitic error suppression as in [16], by means of a digital delay line.

C. DIRECT DIGITAL SYNTHESIZER (SYNT)

A direct digital synthesizer (SYNT) is integrated on the ReDAC test-chip to generate the digital ramps and sine waves to be fed to the ReDACs inputs for static and dynamic testing.

The SYNT block is based on a classical phase-to-amplitude conversion architecture [21], in which the lookup table (LUT), is directly synthesized by combinational logic rather than by a read-only memory (ROM), resulting in a simpler and compact implementation.

The digital code *DATA* provided to the ReDAC can be set via scan-chain to be a ramp (output of the phase accumulator) or a sinewave with configurable offset, amplitude and frequency for static and dynamic testing.

V. TEST SETUP AND EXPERIMENTAL RESULTS

The ReDAC has been tested under static and dynamic conditions by the setup in Fig.12. Here, the ReDAC power supply is provided by a source meter and the on-chip digital blocks are operated via the on-chip scan-chain by an FPGA connected to a PC by a serial data link. The output pad of the SHA is probed and acquired by a 16 bit Picoscope® 4262 oscilloscope connected to the test printed circuit board (PCB).

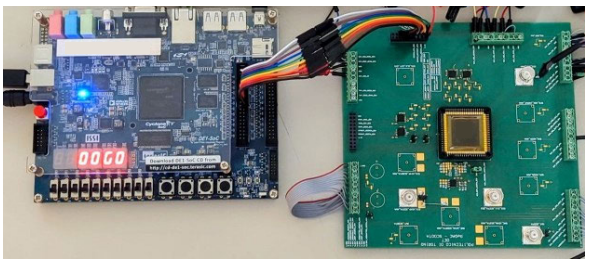


FIGURE 12. Experimental test setup.

The experimental characterization of the SE-ReDAC and of the Diff-ReDAC cells under static and dynamic conditions is presented in the following.

A. SE-REDAC

The results of the characterization of the SE-ReDAC circuit are reported in the following.

1) STATIC CHARACTERIZATION

The SE-ReDAC cell is tested for static characterization under the nominal conditions of 0.65 V supply at ambient temperature. Once the automatic calibration is run and completed, static characterization is performed and its nonlinearity is reported in Fig. 13(a), revealing a maximum (rms) INL of 1.26 LSB (0.42 LSB) and maximum (rms) DNL of 0.34 LSB (0.14 LSB).

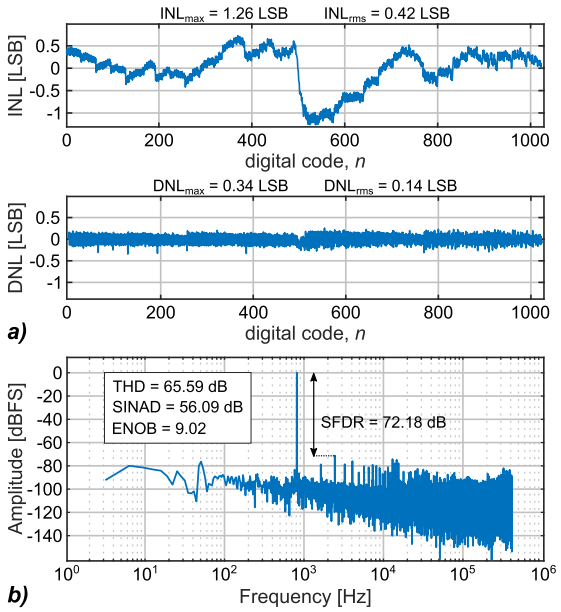


FIGURE 13. SE-ReDAC: static linearity (a) and output spectrum at 0.8 kHz-frequency, 90%-swing amplitude sinewave input (b).

2) DYNAMIC CHARACTERIZATION

The SE-ReDAC is then tested under dynamic conditions with a sinewave input at 0.8 kHz frequency, 90% swing amplitude. The output spectrum measured under these conditions is reported in Fig. 13(b) and reveals a SFDR of 72.18 dB, a THD of 65.59 dB and a SINAD of 56.09 dB, corresponding to 9.02 bit ENOB.

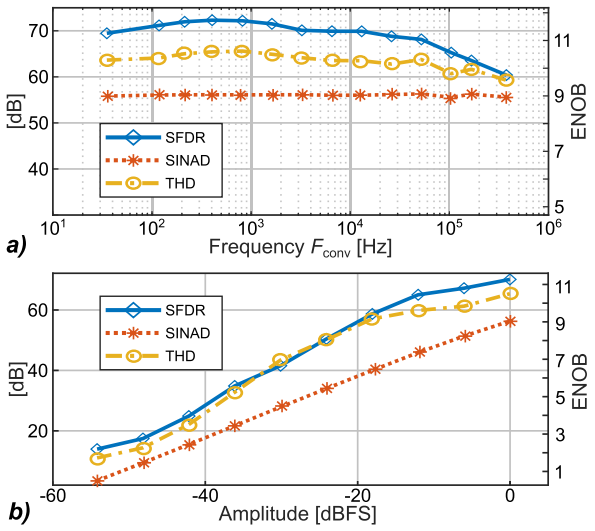


FIGURE 14. SE-ReDAC: dynamic ReDAC characterization versus input frequency at constant 90% swing amplitude (a), and versus input amplitude at 0.8 kHz input frequency (b).

The SE-ReDAC dynamic characterization at constant amplitude (90% full swing up to the Nyquist frequency) and at constant frequency (0.8kHz spanning the whole input

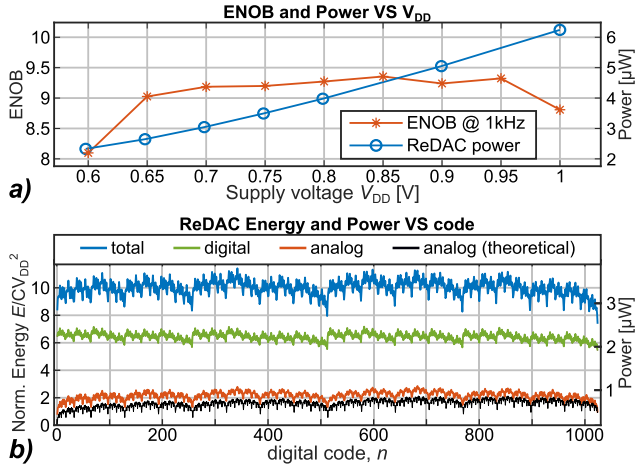


FIGURE 15. SE-ReDAC ENOB and power versus supply voltages (a) and energy per conversion/power versus digital code (b).

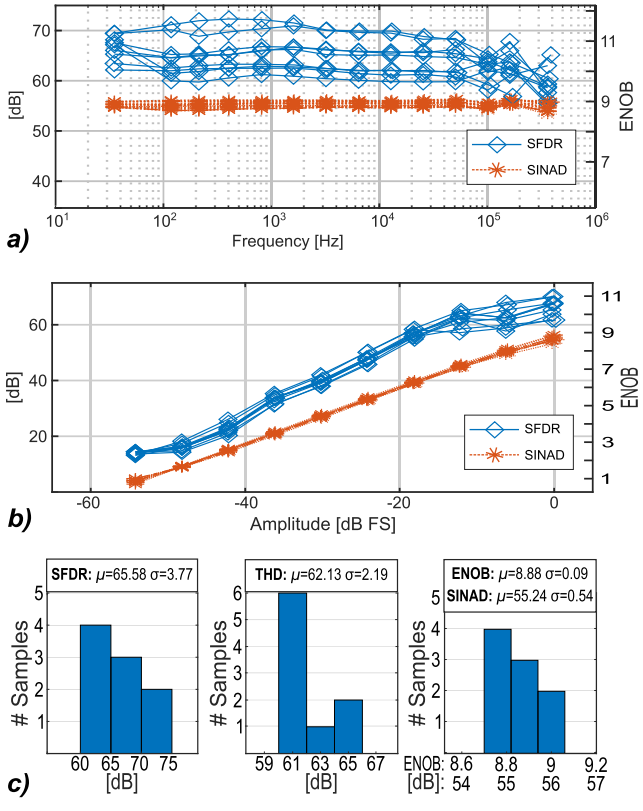


FIGURE 16. Multi-dice dynamic SE-ReDAC characterization over frequency, at 90%-swing amplitude (a), and over amplitude at 0.8 kHz input frequency. Distribution of the SE-ReDAC multi-dice dynamic performance at 0.8 kHz input frequency and 90%-swing amplitude (c).

swing) are reported in Fig. 14(a) and Fig. 14(b) respectively, revealing consistency in the whole frequency and amplitude range. The comparison of the SINAD and of the THD/SFDR plots suggests that the measured dynamic performance is noise-limited, while the SE-ReDAC linearity is very close to the 10-bit design target.

3) POWER CONSUMPTION AND VOLTAGE SCALING

Dynamic characterization of the SE-ReDAC under 1kHz sinewave, 90% swing, for supply voltages ranging in 0.6 V to 1 V reveal an ENOB equal or larger than 9 bit on a wide supply range, as reported in Fig. 15(a).

The SE-ReDAC average power for continuous conversion, under the same supply voltage sweep, is reported in Fig. 15(a) as well, revealing a power dissipation ranging from 2.3 μW to 6.2 μW and an optimum power-performance point between 0.65 V and 0.7 V.

In Fig. 7(b) the SE-ReDAC analog, digital and total power dissipation versus code is reported; the analog normalised energy per conversion nicely follows the predicted theoretical trend in (6), initially reported in [15], resulting in average analog (digital, total) power of 0.8 μW (2.5 μW, 3.3 μW).

4) MULTI-DICE MEASUREMENTS

The results of the SE-ReDAC dynamic characterization across nine dice up to the Nyquist rate (under 90% swing amplitude) is reported in Fig. 16(a).

The single frequency in-band characterization (0.8 kHz, 90% swing) performance distribution in Fig. 16(b) reveals a mean (standard deviation) of 65.58 dB (3.77 dB) for SFDR, 82.13 dB (2.19 dB) for THD and 55.24 dB (0.54 dB) for SINAD, resulting in a highly consistent effective resolution (ENOB) of 8.88 bit across the samples, with a standard deviation of just 0.09 bit.

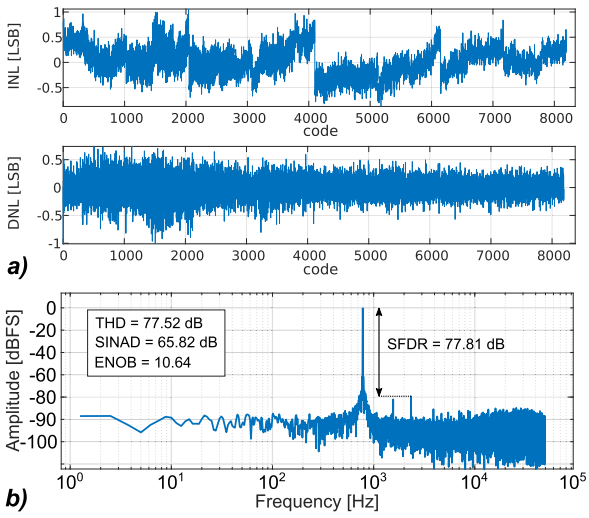


FIGURE 17. Diff-ReDAC: static linearity (a), and 0.8 kHz, 90% swing spectrum (b).

B. DIFF-REDAC

The results of the characterization of the Diff-ReDAC circuit are reported in the following.

1) STATIC CHARACTERIZATION

The results of the Diff-ReDAC static characterization under 0.6 V power supply and at ambient temperature are reported

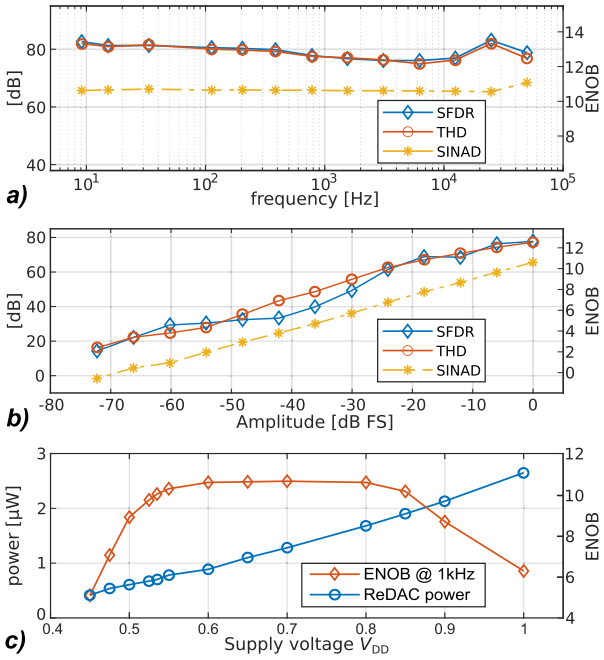


FIGURE 18. Diff-ReDAC: dynamic characterization versus input sinewave frequency at constant 90%-swing amplitude (a), versus input sinewave amplitude at constant 0.8 kHz input frequency (b), ENOB and power consumption at different power supply voltages, for a fixed sinewave input at 800 Hz frequency, 90%-swing amplitude (c).

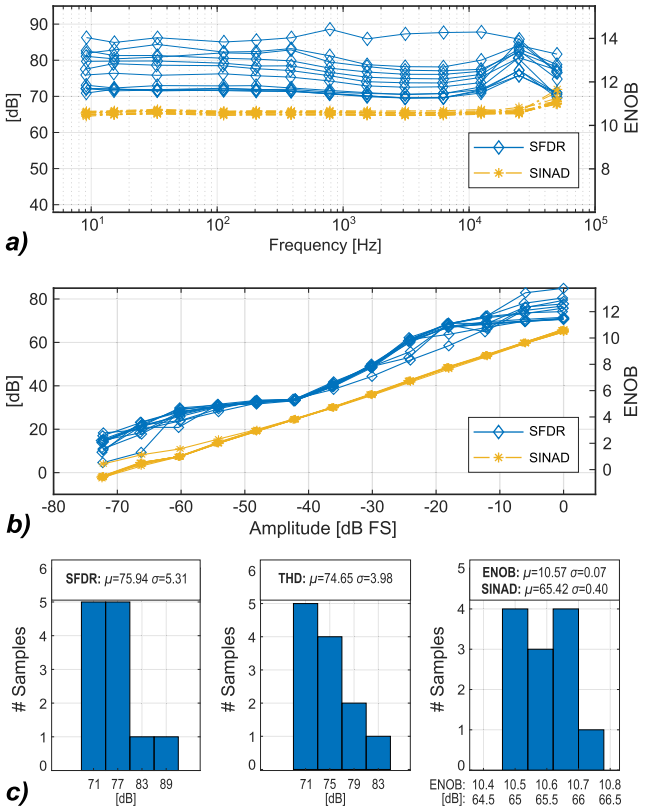


FIGURE 19. Multi-dice dynamic Diff-ReDAC characterization over frequency at 90%-swing amplitude (a), and over amplitude, at 0.8 kHz input frequency (b). Distribution of the Diff-ReDAC multi-dice dynamic performance at 0.8 kHz input frequency, 90% swing amplitude (c).

in Fig. 17(a) and reveal a maximum (rms) INL of 1.07 LSB (0.28 LSB) and a maximum (rms) DNL of 0.96 LSB (0.20 LSB).

2) DYNAMIC CHARACTERIZATION

The spectrum of the Diff-ReDAC output voltage under a 0.8 kHz, 90% swing sine is reported in Fig. 17(b) and reveals a SFDR (THD) of 77.81 dB (77.52 dB) and a 65.82 dB SINAD, resulting in an effective resolution of 10.64 ENOB. Based on Fig. 18(a) and Fig. 18(b), the Diff-ReDAC shows consistent performance up to the Nyquist rate and over the whole input swing. Comparing the SINAD plot with the THD and SFDR plots it can be observed that the measured Diff-ReDAC dynamic performance is noise-limited, while its linearity is close to the 13-bit design target.

3) POWER CONSUMPTION AND VOLTAGE SCALING

The dynamic performance/power tradeoff for the Diff-ReDAC converter has been tested at 800 Hz, 90 % swing sine under different supply voltages (from 0.45 V to 1 V). The results of the test, reported in Fig.18(c) reveal an ENOB larger than 10 bits over most of the supply range and with a power dissipation ranging from 420 nW to 2,650 nW (880 nW under 0.6 V nominal supply).

4) MULTI-DICE MEASUREMENTS

The multi-dice validation across 12 samples is performed under 90 % input sinewave and up to Nyquist (Fig. 19(a)) and at constant 0.8 kHz frequency spanning the whole input range (Fig. 19(b)).

The histograms of the main performance, which are reported in Fig. 19(c), reveal a mean SFDR of 75.94 dB with a standard deviation of 5.31 dB, a mean THD of 74.65 dB with a standard deviation of 3.98 dB and a mean SINAD of 65.42 dB with a standard deviation of only 0.40 dB, resulting in a very consistent Diff-ReDAC effective resolution (ENOB) of 10.57 bit with only 0.07 bit standard deviation.

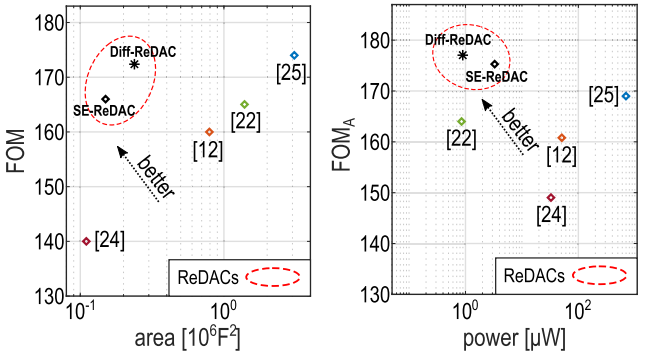


FIGURE 20. Schreirer FOM vs. area and area-normalised FOM_A vs power: comparison with the state of the art.

TABLE 2. DAC performance comparison.

	This Work		[12]	[20]	[18]	[22]	[23]	[24]	[25]
Tech. (nm)	180		40	40	180	180	180	350	180
Type	SE-ReDAC	Diff-ReDAC	DDPM	ReDAC	ReDAC	cap+mos	R-string	curr. steer.	$\Sigma\Delta$
validation	meas.		meas.	sim.	sim.	meas.	meas.	meas.	meas.
Area ($10^6 \mu m^2$)	0.00503	0.00780	0.00127	0.00091	0.01359[a]	0.045[b]	0.15	0.014	0.10[c]
Area ($10^6 F^2$)	0.15	0.24	0.79	0.57	0.42	1.39	4.6	0.11	3.08
Resolution (bit)	10	13	12	10	10	10	12	9	N/A
Sample rate (kS/s)	880	100	110	400	1,450	200	72[d]	111	40[e]
Supply (V)	0.65	0.6	1	0.6	0.7	0.6	1.8	3.3	1.8
Min.supply (V)	0.6	0.45	0.7	N/A	N/A	N/A	1.8	N/A	N/A
INL (LSB)	1.26	1.07	3	0.33	1.01	0.56	0.54	1.6	N/A
DNL (LSB)	0.34	0.96	1	0.2	0.45	0.32	0.26	0.8	N/A
SFDR (dB)	72.18	77.81	85	76.8	59.3	71	N/A	N/A	N/A
THD (dB)	65.59	77.52	85	66.7	59.2	N/A	N/A	N/A	N/A
SINAD (dB) (peak)	56.09	65.82	72	61.0	58.5	56.43	N/A	48[b]	103[f]
ENOB (peak)	9.02	10.64	11.6	9.9	9.4	9.08	N/A	8[b]	16.8
Power (μW)	3.3	0.88	50.8	0.44	9.15	0.85[b]	875[b]	33	700[g]
[†]FOM(dB)	166	172	160	176	166	165	N/A	140	174[f]
[‡]FOM_A (dB)	175	178	161	178	170	164	N/A	149	169

[†]$FOM = 10\log_{10}\left(\frac{2^{2\cdot ENOB_{BW}}}{P}\right)$ [‡]$FOM_A = FOM + 10\log_{10}(1/A_F)$ being A_F the F-normalised area [a]includes part of the calibration [b]based on text and figures [c] not including reconstruction filter [d]from row-line time [e]twice the signal bandwidth [f]A-weighted [g]analog power only.

C. PERFORMANCE COMPARISON

The performance of the ReDACs presented in this paper is discussed and compared with the state of the art in Tab. 2. From the comparison it can be observed that the proposed SE-ReDAC achieves from 2.8× [18] to 3.8× [20] smaller normalized area compared to previously reported ReDACs and the second smallest total normalised area among all (30% larger than the minimum [24], which achieves lower resolution and sample rate).

Compared to DDPM DACs [11], the SE-ReDAC requires a much lower clock frequency to operate at the same bandwidth, while keeping consistent dynamic performance across the whole frequency range (only 0.08 bit ENOB degradation is observed at the Nyquist-rate, compared to the 6.1 bit difference in [11]).

Based on these results, the SE-ReDAC achieves a very competitive energy efficiency figure of merit (FOM) and area-normalized figure of merit (FOM_A) of 166 dB and 175 dB, respectively (see Fig. 20), comparable only with sigma-delta audio DACs [25], which achieves 7.8 more (A-weighted) effective bits with a 20× smaller bandwidth at the cost of 212× more power and 19.9× more area. The proposed ReDAC is also operating at the lowest voltage (same as [20], [22]).

Compared to silicon-proven DACs reported in Tab. 2, the Diff-ReDAC achieves the second smallest absolute area (6.1× more than [11], fabricated in a finer node) and the second smallest normalised area (2.2× the area of [24], which has comparable sample rate and 2.6 less ENOB) and is 19× smaller than [23]. Moreover, our Diff-ReDAC can operate down to the lowest supply voltage (0.45 V) featuring energy-quality scaling.

The Diff-ReDAC achieves the second best energy-efficiency figure of merit FOM of 172 dB (2 dB less than the FOM of the oversampled converter [25], which is based on A-weighted ENOB and has a 795× larger power consumption) and the best area-normalised FOM_A of 178 dB (9 dB more than [25] and 29 dB more than the current-steering DAC [24]).

VI. CONCLUSION

The design and silicon verification of a single-ended and of a differential ReDACs in 180 nm featuring digital self-calibration and parasitics-induced error suppression have been presented. The proposed SE-ReDAC occupies just 5,030 μ m^2 and draws 3.3 μ W from a 0.65 V power supply voltage at 880 kS/s and 9.02 ENOB, achieving competitive energy efficiency, and area-normalized energy efficiency figures of merit of 166 dB and 175 dB, respectively. On the other hand, the Diff-ReDAC design operates down to 0.45 V power supply and with 7,800 μm^2 area and 880 nW power consumption at 100 kS/s and 10.64 ENOB, achieves a FOM of 172 dB and the best reported area normalized energy efficiency FOM_A of 178 dB. Such remarkable results highlight the inherent advantages and the potential of the ReDAC technique in the design of compact, very low power, low design effort, robust integrated DACs for medium resolution and kS/s-to-MS/s sample rate applications, thus meeting the requirements of low-cost analog interfaces for next-generation IoT applications and biosensors.

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