Design of a Multi-Mode Input-Parallel-Output-Series Power Optimizer for Wide-Voltage Range Photovoltaic Applications

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***Abstract*—This paper presents a new hybrid multi-mode Input-Parallel-Output-Series converter to be employed as a Parallel Power Optimizer (PPO) for photovoltaic (PV) applications. The converter combines the high efficiency conversion of an LLC processing the largest fraction of the input power with the possibility to provide a fine gain modulation thanks to a synchronous boost working in the Boundary Conduction Mode. The achievable input voltage range is further extended by a topology-morphing rectifier in the LLC. The proposed optimizer is designed based on the specifications of a target bifacial PV module and preliminary simulation results show that the converter achieves a high efficiency above 94.5% over the wide 15 V–45 V input voltage range, exhibiting a California Energy Commission (CEC) efficiency of 97.0% at the rated 36.5 V voltage.**

***Index Terms*—Power Optimizer, Input-Parallel-Output-Series, Multimode converters, Topology-morphing,**

I. Introduction

Among the various converter architecture solutions to interface photovoltaic (PV) plants to the grid, Parallel Power Optimizers (PPO) ensure the best trade-off bewteen harvesting potential, flexibility and system reliability [1]. Thanks to the parallel connection of the output ports at the same DC rail, a PPO-based system allows to completely eliminate the mismatches between different conversion stages that may arise from unbalanced shading scenarios. In addition, the eventual failure of one optimizer does not compromise the energy harvesting of the entire PV plant, as in Series-Power Optimizers or string solutions. On the other hand, to effectively provide a panel-level Maximum Power Point Tracking (MPPT), PPOs should ensure high voltage gain over a wide voltage and power range to cope with changing temperature, irradiance and shading conditions [2]. Many solutions were proposed in the literature to simultaneously meet the high gain and the wide input voltage range requirements.

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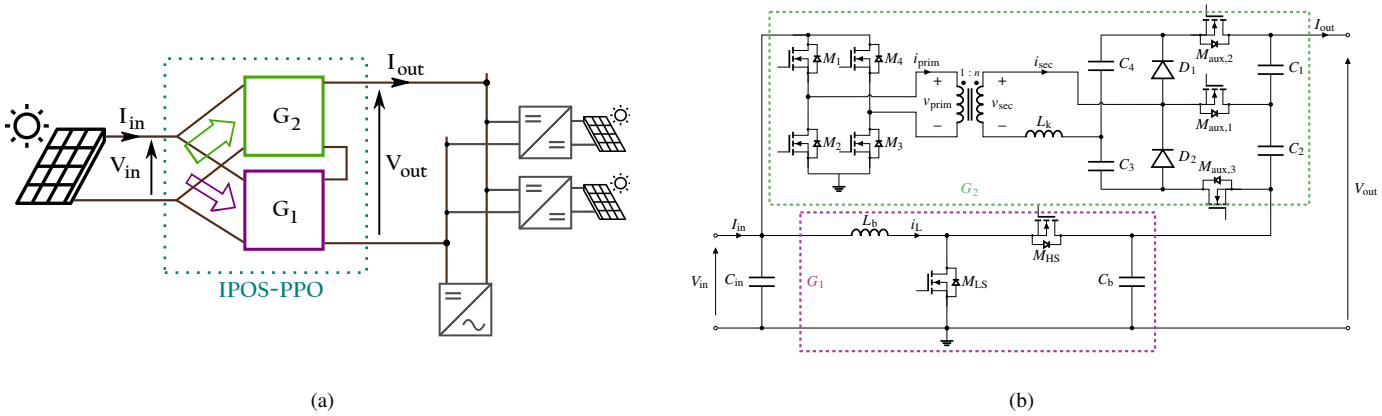
Conventional non-isolated topologies achieve the required high step-up voltage gain employing hybrid and modular structures composed of voltage multipliers and switched capacitors networks [3], [4]. The main limitation of these converters is the large number of passive components to realize the voltage step-up modules, especially diodes and capacitors.

Multi-mode converters such as [5] or [6] overcome this limitation by using a transformer winding ratio as an additional degree of freedom to step up the voltage and, at the same time, to set the maximum efficiency working point at a desired input voltage. These converters are usually based on a resonant LLC equipped with additional conversion stages or an ad-hoc control system to switch between operating modes according to the input voltage to be tracked. The core LLC provides a high efficiency at the rated voltage, but the converters experience gradual and monotonous efficiency decrease moving away from that.

In other solutions, topology-morphing rectifiers are applied to LLC converters to extend the voltage range and achieve very flat efficiency curves characterized by multiple peaks [7], [8], at the expense of a large component count of the rectifier.

A good trade-off between number of components, design flexibility and efficiency is achieved with Input-Parallel-Output-Series (IPOS) converter topologies, in which the input power is split between two conversion stages. This approach allows to reduce the current stresses at the low voltage input ports and the voltage stresses at the output series-connected ports. Minimized current stresses can be obtained by employing identical topologies in the IPOS architecture [9]–[11], whereas a larger flexibility can be achieved when different topologies are adopted [12], [13].



(a) (b)

Figure 1: System-level block diagram and schematic of the proposed IPOS-PPO. (a) Block diagram of the proposed IPOS-PPO. (b) Schematic of the proposed IPOS-PPO.

The converter proposed in this work applies the idea of an unbalanced power splitting of an asymmetric IPOS topology [13] to a PPO, to increase the design flexibility and provide the required high and variable gain, while limiting the electrical stresses. In addition, the proposed converter features a multi-mode operation based on a topology-morphing network to extend the voltage gain. An ad-hoc design methodology is exploited to maximise the conversion efficiency in the neighbourhood of a target PV panel rated voltage, where the module is more likely to work. At the same time, the topology-morphing network allows to limit the efficiency reduction when working far from the rated voltage. The rest of the article is divided as follows: Section II illustrates the main features and the operating principle of the converter, Section III describes the design of its main components, Section IV reports some relevant simulation results to validate the proposed approach, while Section V draws the conclusions and presents the future work.

II. Converter topology and operation

A block diagram of the proposed IPOS-PPO is shown in Fig. 1a, highlighting the parallel connection of multiple DC-DC converters at the high-voltage bus, and the IPOS arrangement of the two conversion stages in the topology. In IPOS architectures, since none of the conversion stages processes the entire input power, the total efficiency becomes:

$$\begin{aligned}\eta_{\mathrm{TOT}} &= \eta_1 \cdot \left(\frac{P_1}{P_{\mathrm{TOT}}}\right) + \eta_2 \cdot \left(\frac{P_2}{P_{\mathrm{TOT}}}\right) \\ &\approx \eta_1 \cdot \left(\frac{G_1 V_{\mathrm{in}} I_{\mathrm{out}}}{V_{\mathrm{out}} I_{\mathrm{out}}}\right) + \eta_2 \cdot \left(\frac{G_2 V_{\mathrm{in}} I_{\mathrm{out}}}{V_{\mathrm{out}} I_{\mathrm{out}}}\right) \\ &= \eta_1 \cdot \left(\frac{G_1}{G_{\mathrm{TOT}}}\right) + \eta_2 \cdot \left(\frac{G_2}{G_{\mathrm{TOT}}}\right), \end{aligned} \tag{1}$$

where η_i, P_i and G_i represent the conversion efficiency, processed power and voltage gain of the i-th stage, respectively. This feature overcomes the intrinsic limitation of cascaded multi-stage architectures, in which all the stages process the total power and then η_{TOT} is the product of the stages efficiencies η_i. Since the DC-link voltage $V_{\mathrm{out}} = 350\,\mathrm{V}$ is fixed by the inverter, the changing irradiance, shading and temperature conditions impose to vary continuously the voltage gain to track the Maximum Power Point of the module.

A. Multi-mode operation

Taking advantage from (1), this work considers two different conversion stages designed to process unbalanced fractions of the total input power: a high-efficiency, fixed-gain G_2 stage processing the largest fraction, and a low and variable gain one (G_1). The combination of the stages in an IPOS architecture ensures lower current stresses at both the input ports and decreases the individual voltage gain requirements. To further extend the achievable voltage range, a topology-morphing approach is exploited in the second gain stage G_2, providing an additional degree of freedom to reduce G_1.

To implement these functionalities, the converter topology shown in Fig. 1b is proposed in this work. A resonant LLC converter with secondary resonance (involving the leakage inductance of the transformer L_{k} and capacitors $C_3 - C_4$) and Voltage Doubler Rectifier (VDR) is selected for G_2. This stage is designed to provide a high efficiency fixed-gain conversion by operating at resonance, which ensures the ZVS turn-ON of the input FETs, and the ZCS turn-OFF of the rectifier diodes.

A synchronous boost working in the Boundary Conduction Mode (BCM) is designed to provide a continuous gain modulation G_1. This topology is selected among other step-up converters to minimize the component count and the control complexity. The variable-frequency BCM is preferred among the other working modes for the possibility to achieve the Zero-Voltage Switching (ZVS) turn-ON of both the high-side and low-side MOSFETs [14]. At the same time, for the same processed power, the BCM results in reduced current stresses on all the components compared to the Discontinuous Conduction Mode (DCM).

Contrarily to symmetrical IPOS or interleaved converters [9]–[11], the boost and LLC stages work asynchronously, due to the variable-frequency modulation: as a consequence,

Table I: Correspondence between rectifier MOSFETs and topology.

$M_{\text{aux},1}$	$M_{\text{aux},2-3}$	Rectifier topology
ON	OFF	VQR
OFF	ON	VDR

Table II: Summary of the main features of the proposed multi-mode operation.

Mode	Voltage boundaries	LLC	Boost	G_{TOT}
LV	$\left[V_{\text{in,min}};\ \frac{V_{\text{out}}}{4n+1}\right]$	Resonance	BCM	$4n + \frac{1}{1-D}$
MV	$\left(\frac{V_{\text{out}}}{4n+1};\ \frac{V_{\text{out}}}{2n+1}\right]$	Resonance	BCM	$2n + \frac{1}{1-D}$
HV	$\left(\frac{V_{\text{out}}}{2n+1};\ V_{\text{in,max}}\right]$	PSM	$D = 0$	$G_2(\Phi) + 1$

a larger ripple current is expected at the input port.

The present analysis focuses on the innovative features of the multi-mode operation and on the most relevant design considerations. At a system level, the transformer turns ratio n of the LLC is the most critical design parameter of the converter because it determines, for a given PV panel working point, the required static voltage gain and the fraction of power processed by each conversion stage. When the LLC operates at resonance with a Voltage Doubler Rectifier (VDR) configuration, its constant voltage gain is $G_2 = 2n$ and the required boost gain becomes:

$$G_1 = G_{\text{TOT}} - G_2 = \frac{V_{\text{out}}}{V_{\text{in}}} - 2n\,. \tag{2}$$

As a consequence, the fraction of power processed by the boost is also function of n and increases when V_{in} decreases:

$$\frac{P_1}{P_{\text{TOT}}} \approx \frac{G_1}{G_{\text{TOT}}} = 1 - 2n\frac{V_{\text{in}}}{V_{\text{out}}}\,. \tag{3}$$

At low input voltages, when the PV module is working under partial shading scenarios, the combination of a high voltage gain and high processed power may lead to significant conduction losses, switching losses and inductor core losses in the boost. To reduce the required boost gain G_1 at low input voltages, the LLC includes a topology-morphing rectifier switching from a VDR to a Voltage Quadrupler Rectifier (VQR). With this approach, $G_2 = 4n$ and the boost gain becomes:

$$G_1 = G_{\text{TOT}} - G_2 = \frac{V_{\text{out}}}{V_{\text{in}}} - 4n\,. \tag{4}$$

The rectifier topology is determined by the conduction state of three auxiliary MOSFETs $M_{\text{aux},1}$, $M_{\text{aux},2}$ and $M_{\text{aux},3}$. Tab. I illustrates the correspondence between their conduction state and the obtained rectifier topology.

One of the main features of the proposed converter is the possibility to use the transformer ratio n as a degree of freedom to set the maximum efficiency at a desired rated voltage. This could be, for instance, the MPP voltage of a target PV module at Standard Test Conditions (STC). More in general, it may be of interest to achieve the highest conversion efficiencies in correspondence of the most frequent and highest power PV voltages. Intuitively, the maximum efficiency is obtained for the minimum boost gain ($G_1 = 1$). As a result, n can be derived from (2) by imposing the minimum G_1 at the desired PV voltage V_{MPP}:

$$G_1(V_{\text{MPP}}) = \frac{V_{\text{out}}}{V_{\text{MPP}}} - 2n \overset{!}{=} 1 \Longrightarrow n = \frac{1}{2}\left(\frac{V_{\text{out}}}{V_{\text{MPP}}} - 1\right). \tag{5}$$

Two observations follow from (5):

- for a given n, there are two working voltages at which it is possible to minimize G_1 (and thus, to obtain local efficiency peaks). In this article, these voltages will be referred to as $V^-_{\text{threshold}}$ and $V^+_{\text{threshold}}$ and are expressed in (6) and (7), respectively:

$$V^-_{\text{threshold}} = \frac{V_{\text{out}}}{4n+1} \tag{6}$$

$$V^+_{\text{threshold}} = V_{\text{MPP}} = \frac{V_{\text{out}}}{2n+1} \tag{7}$$

- for $V_{\text{in}} > V^+_{\text{threshold}}$, the boost cannot provide the required step-down voltage gain. However, at low ambient temperatures, the MPP voltage of a PV panel is likely to increase above the STC voltage. To extend the MPP window above $V^+_{\text{threshold}}$, the proposed converter can operate in a third mode, in which the gain is modulated by Phase-Shift Modulation (PSM) of the LLC [15]. In this mode, only the high-side MOSFET M_{HS} is ON, and the boost provides a constant unity gain.

To summarize, according to the input voltage, the converter can operate in three modes, as reported in Tab. II. . At low input voltages (LV mode, $V_{\text{in}} \leq V^-_{\text{threshold}}$), the LLC operates at resonance with a VQR, and $G_2 = 4n$. The boost duty cycle D variation provides the required gain modulation. At intermediate input voltages (MV mode, $V^-_{\text{threshold}} < V_{\text{in}} \leq V^+_{\text{threshold}}$), the LLC rectifier morphs to a VDR ($G_2 = 2n$), while the boost still operates in BCM. At high input voltages (HV mode, $V_{\text{in}} > V^+_{\text{threshold}}$), the boost provides unity gain and the LLC full-bridge works in PSM. For $n = 4$, the share of gains between boost and LLC is graphically illustrated in Fig. 2. As shown, the topology-morphing approach allows to significantly reduce the boost gain requirements at low voltages.

B. Modified ZVS operation of BCM boost

In the conventional BCM (C-BCM) operation, the high-side MOSFET M_{HS} is controlled to be turned OFF at zero current, as shown in Fig. 3a. The null current is in most cases ineffective to discharge the low-side MOSFET C_{oss} during the dead time $t_{\text{dead,b}}$, causing the remaining capacitance energy

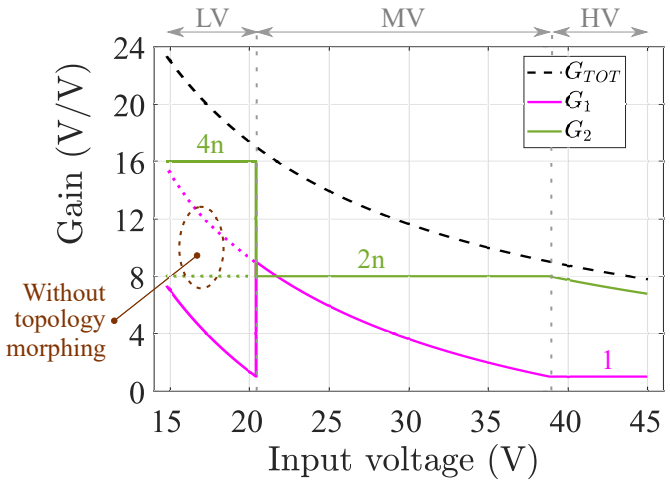


Figure 2: Voltage gains in LV, MV and HV modes.

to be dissipated during the turn ON [14]. This feature, along with the ZVS turn ON and the reduced conduction current of M_{HS} whenever $G_1 > 2$, determines a strong unbalance of losses between the two MOSFETs. To achieve a more uniform distribution of losses, it is possible to extend the conduction time of M_{HS} until the inductor current reaches a sufficiently negative value $I_R \leq 0$ to assist the ZVS turn ON of M_{LS}. This modified approach is here called ZVS-BCM and, as shown in Fig. 3a, determines an increased period T'_{sw} and in increased RMS current for the same average current $\bar{I}_L$ and input-output voltages.

The minimum required I_R for achieving the ZVS can be analytically derived by solving the equivalent boost circuit during the dead time (shown in Fig. 3b), with $C_{oss,LS} = C_{oss,HS} = C_{oss,b}$ and initial conditions $i_L(0) = I_R$ and $v_{sw}(0) = G_1 V_{in}$. The minimum I_R to completely discharge $C_{oss,LS}$ before the end of the dead time $t_{dead,b}$ is expressed in (8):

$$I_R < -\frac{V_{in}}{Z_0} \cdot \frac{1 + (G_1 - 1)\cos(\omega_0 t_{dead,b})}{\sin(\omega_0 t_{dead,b})}, \tag{8}$$

where $Z_0 = \sqrt{L_b/2C_{oss,b}}$ and $\omega_0 = 1/2\pi\sqrt{2C_{oss,b}L_b}$. Notice that (8) represents a more general expression of the current constraint derived in [14] extended to the case in which the boost gain is higher than 2. Since both G_1 and $C_{oss,b}$ depend on V_{in}, the minimum I_R is overall a function of V_{in} for a specific selection of MOSFETs. Clearly, the minimum I_R is recommended to minimize the conduction losses.

III. Converter design

A specific bifacial PV panel was considered for the design of the converter, 3SUN-B60 [16]. The design approach presented here, however, can be easily generalized according to the PV module voltage range at which it is desired to maximise the efficiency. After defining the turns ratio from (5), all the components voltage and current stresses can be derived as a consequence.

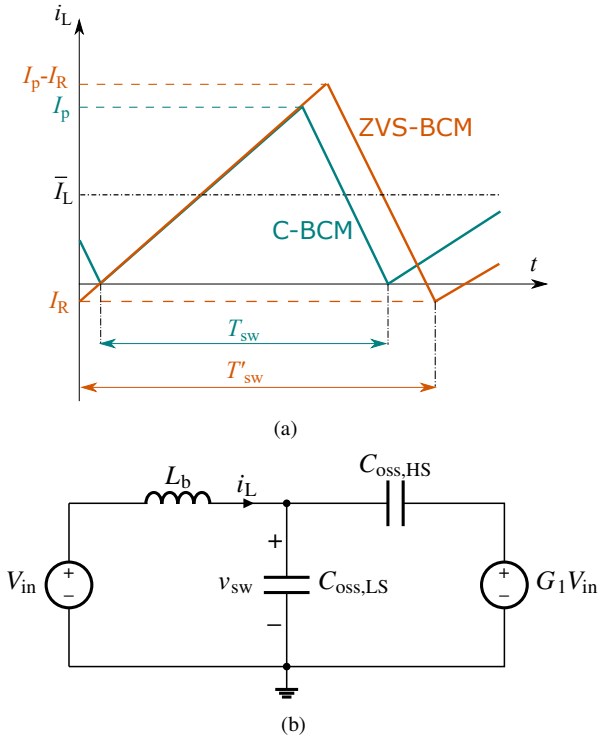


Figure 3: Modelling of the BCM boost to achieve the ZVS turn ON of the low-side MOSFET. (a) Qualitative waveforms of the boost inductor current in the C-BCM and the modified ZVS-BCM. (b) Equivalent circuit of the boost during the dead time between M_{HS} turn OFF and M_{LS} turn ON.

A. LLC design

The following discussion presents the electrical stresses highlighting the main differences between the LV and MV mode, which can be analytically described. A more detailed derivation of the electrical stresses of a PSM-LLC can be found in [17]. Beside the turns ratio, the main design parameters of the transformer are the magnetizing inductance L_m and the leakage inductance L_k. L_m is referred to the primary side and its value can be determined according to the output capacitances of the full bridge MOSFETs M_{1-4}, in order to achieve their ZVS turn-ON [18]:

$$L_m < \frac{t_{dead}}{8C_{oss}f_{sw}}, \tag{9}$$

where t_{dead} is the dead time duration and C_{oss} is the energy-equivalent output capacitance of the FETs. L_k is referred to the secondary side, as shown in Fig. 1b, and is employed to resonate with C_3 and C_4 (with $C_3 = C_4 = C_r$). Its value can be designed according to the desired resonance frequency $f_{res} = 1/2\pi\sqrt{2C_rL_k}$ and regulation capability when the LLC is controlled in the PSM. For the same load and desired voltage gain, indeed, a larger L_k decreases the required phase shift. In this specific case, however, since the converter is expected to work mainly in the MV mode (at resonance), a lower L_k is preferred, resulting in a better magnetic coupling between primary and secondary sides. The primary and secondary

current stresses of the transformer can be expressed as in (10) and (11), respectively:

$$I_{\text{prim,RMS}} = \left[\left(\frac{\pi}{2\sqrt{2}} G_2 I_{\text{out}} \right)^2 + \left(\frac{V_{\text{in}}}{4\sqrt{3} f_{\text{sw}} L_{\text{m}}} \right)^2 \right]^{\frac{1}{2}} \tag{10}$$

$$I_{\text{sec,RMS}} = \frac{\pi G_2}{2\sqrt{2} n} I_{\text{out}} , \tag{11}$$

where G_2 depends on the operating mode, according to Tab. II. An optimized approach for the selection of the resonance frequency will be investigated in a future work.

The full-bridge FETs voltage stress is limited by the maximum V_{in}. When operating at resonance (in both LV and MV modes), their current stresses are equally distribute:

$$I_{\text{M}_{1-4},\text{RMS}} = \frac{\pi}{4} G_2 I_{\text{out}} . \tag{12}$$

Since the turn-ON losses are minimized, low $R_{\text{DS,ON}}$ FETs are preferred to minimize the conduction losses as well. However, low $R_{\text{DS,ON}}$ devices usually exhibit worse switching performances, which would result in a larger magnetizing current to satisfy the ZVS constraint, and increased turn-OFF losses. An optimal trade-off between conduction and switching losses should be investigated.

The rectifier diodes D_1 and D_2, thanks to the resonant operation, turn OFF at zero current. Their current stress is a half sinusoid with average value I_{out}, in both the LV and MV modes. Their maximum voltage stress $V_{\text{D}_{1-2},\text{max}}$ is experienced in the HV mode, when the boost gain is unitary:

$$V_{\text{D}_{1-2},\text{max}} \approx V_{\text{out}} - V^{+}_{\text{threshold}} . \tag{13}$$

In the MV mode, the auxiliary MOSFETs $M_{\text{aux},2-3}$ are kept ON and their current stress is a rectified sinusoid with RMS value $\frac{\pi}{2\sqrt{2}} I_{\text{out}}$, whereas $M_{\text{aux},1}$ is OFF. In the LV mode, instead, $M_{\text{aux},1}$ conducts a sinusoidal current whose RMS value is $\frac{\pi}{\sqrt{2}} I_{\text{out}}$. In this mode, the body diodes of $M_{\text{aux},2}$ and $M_{\text{aux},3}$ are exploited to implement the VQR, while the MOSFETs are kept OFF. This approach allows to avoid additional external diodes, while improving the conduction performances in the MV mode thanks to the MOSFETs conduction. In addition, since it is not required to turn ON and OFF these MOSFET at the switching frequency f_{sw}, slower and cheaper opto-couplers can be adopted instead of more expensive gate drivers. The operating principle of a VQR is better detailed in [19].

B. Boost design

Once the transformer ratio n is selected from (5), the boost voltage gain G_1 is determined for the LV and MV modes according to (4) and (2), respectively. The required duty cycle derives consequently:

$$D = 1 - \frac{1}{G_1} . \tag{14}$$

In this work, the variable-frequency BCM is preferred compared to the fixed-frequency one for the possibility to reduce the conduction losses at reduced load [14]. From (3)

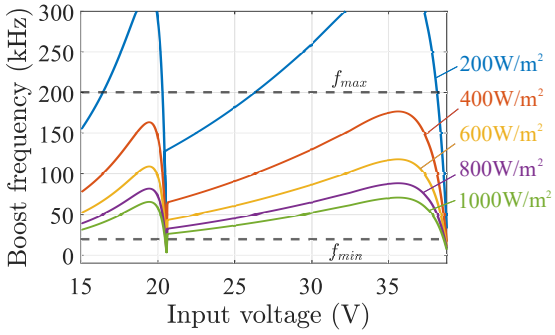


Figure 4: Boost frequency as function of input voltage at various irradiance conditions.

and from the analysis of the static voltage gain in a BCM boost, it is possible to prove that the operating frequency $f_{\text{sw,BCM}}$ can be expressed as:

$$f_{\text{sw,BCM}} = \frac{G_1 - 1}{G_1^2} \frac{V_{\text{in}} V_{\text{out}}}{2 L_{\text{b}} P_{\text{out}}} , \tag{15}$$

where L_{b} is the boost inductance. Since G_1 and P_{out} depends on the PV panel working point, L_{b} is the only design choice to set $f_{\text{sw,BCM}}$ in a desired frequency range. Additional criteria such as power density, inductor losses and MOSFETs switching losses could be taken into account. Fig. 4 illustrates the behaviour of $f_{\text{sw,BCM}}$ as function of V_{in}, for different uniform irradiance scenarios. The plots refer to $L_{\text{b}} = 30\,\mu\text{H}$ and for the selected $n = 4$, which sets the threshold voltages at around 20.5 V and 38.9 V, respectively. In this case, $L_{\text{b}} = 30\,\mu\text{H}$ was selected so as to ensure that $f_{\text{sw,BCM}}$ is bounded between 20 kHz and 200 kHz for most of the uniform irradiance scenarios, as shown in Fig. 4. At lower irradiances (reduced power), the controller can be designed to clamp $f_{\text{sw,BCM}}$ at 200 kHz, so as to limit the turn-OFF switching losses of the boost FETs. In this operating mode, the boost switches to DCM.

The maximum voltage stress across the boost switches is experienced at the maximum gain operation, immediately above $V^{-}_{\text{threshold}}$ (as shown in Fig. 2), and can be derived from (2) and (6):

$$V_{\text{DS}_{\text{HS,LS}},\text{max}} = V^{-}_{\text{threshold}} \cdot G_1(V^{-}_{\text{threshold}}) = \frac{2n+1}{4n+1} V_{\text{out}} . \tag{16}$$

From Fig. 3a, it is intuitive to observe that the current stresses of the boost components increase compared to the C-BCM according to the value of I_{R}. By defining, for compactness of notation, $\gamma = \sqrt{\frac{3}{4} + \left(\frac{\bar{I}_{\text{L}} - I_{\text{R}}}{2\bar{I}_{\text{L}}} \right)^2}$ ($\gamma \geq 1$), it is possible to express the inductor, low-side MOSFET and high-side MOSFET current stresses as in (17), (18) and (19), respectively.

$$I_{\text{L,RMS}} = \frac{2}{\sqrt{3}} \gamma G_1 I_{\text{out}} \tag{17}$$

$$I_{\text{LS,RMS}} = 2\sqrt{\frac{D}{3}} \gamma G_1 I_{\text{out}} \tag{18}$$

Table III: Main design specifications and circuit parameters adopted for the simulations.

Design specification / parameter	Symbol	Value
Input voltage	V_{in}	15 V – 45 V
Output voltage	V_{out}	350 V
Rated input voltage	$V_{\text{in,rated}}$	36.5 V
Rated power	P_{rated}	750 W
LLC resonance frequency	f_{res}	100 kHz
Transformer turns ratio	n	4
Transformer magnetising inductance	L_{m}	50 µH
Transformer leakage inductance	L_{k}	15 µH
Boost inductance	L_{b}	33 µH

$$I_{\text{HS,RMS}} = 2\sqrt{\frac{1-D}{3}}\gamma G_1 I_{\text{out}} \tag{19}$$

Assuming a constant I_{out}, the triangular current stress of the boost capacitor C_{b} can be expressed in (20):

$$I_{\text{C}_\text{b},\text{RMS}} = I_{\text{out}}\sqrt{\frac{4}{3}G_1\gamma^2 - 1}\,. \tag{20}$$

The minimum required capacitance can be computed by imposing a maximum voltage ripple across C_{b} in the worst-case stress scenario (in correspondence of the maximum G_1), which results in the following approximated expression:

$$C_{\text{b}} > \frac{L I_{\text{out}}^2}{2V_{\text{in}}\Delta V_{\text{C}_\text{b}}}\frac{(2G_1-1)^2}{G_1-1}\,, \tag{21}$$

where $\Delta V_{\text{C}_\text{b}}$ is the maximum tolerated peak-to-peak voltage ripple.

Once both the input current stresses of the LLC and boost are known, the input capacitor stresses follow accordingly. Assuming a constant input current I_{in}, the current flowing through C_{in} is the superposition of a rectified sinusoid from the LLC (with fundamental frequency $2f_{\text{sw}}$) and a triangular current from the boost (with fundamental frequency $f_{\text{sw,BCM}}$). In the LV and MV modes, assuming that the spectra of the LLC and boost currents are perfectly decoupled, the expression of the resulting RMS current can be derived analytically:

$$I_{\text{C}_\text{in},\text{RMS}} = I_{\text{out}}\sqrt{\left(\frac{\pi^2}{8}-1\right)G_2^2 + \left(\frac{4}{3}\gamma^2 - 1\right)G_1^2}\,. \tag{22}$$

From the analysis of (22), it can be proved that, for a constant V_{in} and P_{out}, the lowest current stresses are obtained when G_1 is minimized. This is an additional advantage of setting the minimum G_1 in correspondence of the maximum power point. Due to the complex current waveform, an analytical design equation for the minimum C_{in} is not easy to derive. This work relied on simulations to extract empirically the minimum required capacitance to limit the voltage ripple across the PV module below 8.5% of the rated input voltage [20].

Table IV: Main components of the designed converter used in simulations.

Component	Part number
MOSFETs M_{1-4}	STL120N10F8
Rectifier diodes D_{1-4}	STPSC10065
Rectifier MOSFETs $M_{\text{aux},1-3}$	STB47N50DM6AG
Transformer	ETD 54/28/19 N87, 7:28 turns ratio
Boost MOSFETs $M_{\text{LS-HS}}$	STB41N40DM6AG
Boost inductor L_{b}	AGP4233-333ME

IV. Simulation results

Tab. III lists the main specifications and design parameters following from the proposed design presented in Section III. The selected voltage range sweeps from 15 V (minimum voltage to limit $G_1 < 10$) and 45 V (open circuit voltage of the PV panel at low temperatures). The rated input voltage and power refer to the module Bifacial Standard Test Conditions (BSTC). Tab. IV reports the list of the main components used in simulations, which are compliant with the worst-case electrical stresses derived in Section III. The transformer model adopted for the simulations refers to an equivalent ETD-54/28/19 core in N87 material, with $\frac{N_2}{N_1} = \frac{28}{7}$, and considers both core and winding losses. The simulations were performed in SIMetrix [21] for the possibility to test SPICE models including components non-idealities and temperature-dependent performances.

Fig. 5 shows the power budget of the converter at three representative working conditions, at 15 V in the LV mode (left), at the rated working conditions (center) and at 43 V in the HV mode (right). The selection of $n = 4$ in the current design allows to minimize the boost losses in the neighbourhood of the rated input voltage. At $V_{\text{in}} = 15$ V, instead, the boost contributes to more than 50% of the total losses while processing only approximately 30% of the total power. It is relevant to observe that, despite more than twice the output power, the converter exhibits similar total losses at the rated condition and in the LV operation ($\approx$ 17 W and $\approx$ 14.5 W, respectively), thanks to the strongly unbalanced power splitting that is beneficial at the rated input voltage. In the HV mode, instead, the always-ON HS MOSFET represents the only relevant contribution to the boost losses.

To test the wide-range efficiency of the proposed solution, the IPOS converter was characterized at multiple working points. The input voltage range and operating power range at which the converter was simulated are illustrated qualitatively in Fig. 6a, in which the power-voltage curve refers to the target panel characteristic at BSTC. Fig. 6b shows the behaviour of converter efficiency as function of V_{in} at two representative working powers (300 W and 500 W). At 300 W, the simulated efficiency is always above 94.5% and, as expected, exhibits two local efficiency peaks where the boost gain is minimized, immediately below $V_{\text{threshold}}^{-} = 20.5$ V and $V_{\text{threshold}}^{+} = 38.9$ V.

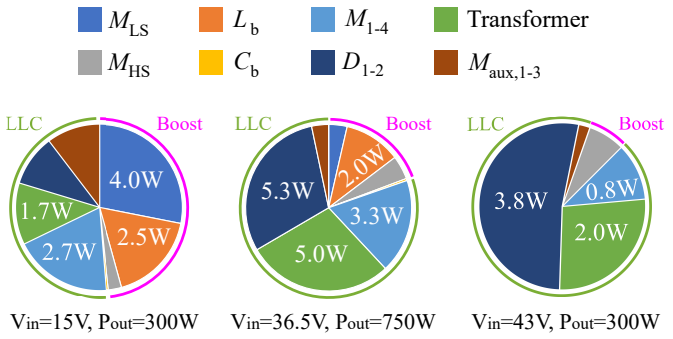


Figure 5: Simulated power budget of the proposed converter at three representative working points: V_{in} = 15 V – P_{out} = 300 W, V_{in} = 36.5 V – P_{out} = 750 W and V_{in} = 43 V – P_{out} = 300 W.

For the same operating power and the same share of power processed by the two stages, however, the converter exhibits slightly improved efficiency at $V^{+}_{threshold}$ (97.10%) compared to $V^{-}_{threshold}$ (96.9%) mainly due to the increased conduction losses of M_{1-4} and the transformer in the LV mode, according to (10), (11) and (12). The highest efficiencies are correctly measured in the neighbourhood of the rated input voltage, both at 300 W and 500 W, validating the effectiveness of the proposed design. The converter efficiency decreases for an increasing boost power (G_1) mainly because of the larger conduction losses, as predicted in (17), (18) and (19). Finally, Fig. 6c reports three efficiency plots as function of the working power, at V_{in} = 15 V, 36.5 V and 43 V. These results are relevant to predict the converter performances in a realistic outdoor scenario with changing irradiance. For operating powers below 300 W, the HV mode ensures improved performances compared to the rated voltage, mainly due to the minimized boost losses and to the easier achievement of the ZVS of the LLC MOSFETs. At V_{in} = 36.5 V, the converter exhibits a flat efficiency above 96.5% on the wide 200 W – 750 W range, with a 97.8% peak at 560 W and 97.0% California Energy Commission (CEC) efficiency. Tab. V compares the proposed IPOS converter with other state of the art solutions of PPOs employing different step-up techniques. The proposed converter shares with multi-mode and topology-morphing converters the relatively high numbers of active switches, three of which are, however, supposed to be always ON or OFF. The use of a transformer allows to significantly reduce the number of diodes and DC capacitors compared to converters based on voltage multipliers. Notice that, despite the transformer in the LLC, the converter does not provide an overall galvanic isolation between PV panel and high-voltage DC rail. From the presented simulation results, the proposed converter exhibits promising performances on a wide range of operating conditions. The effectiveness of the approach will be experimentally verified in future work.

V. Conclusion

The proposed multi-mode power optimizer integrates a topology-morphing network to an Input-Parallel-Output-Series

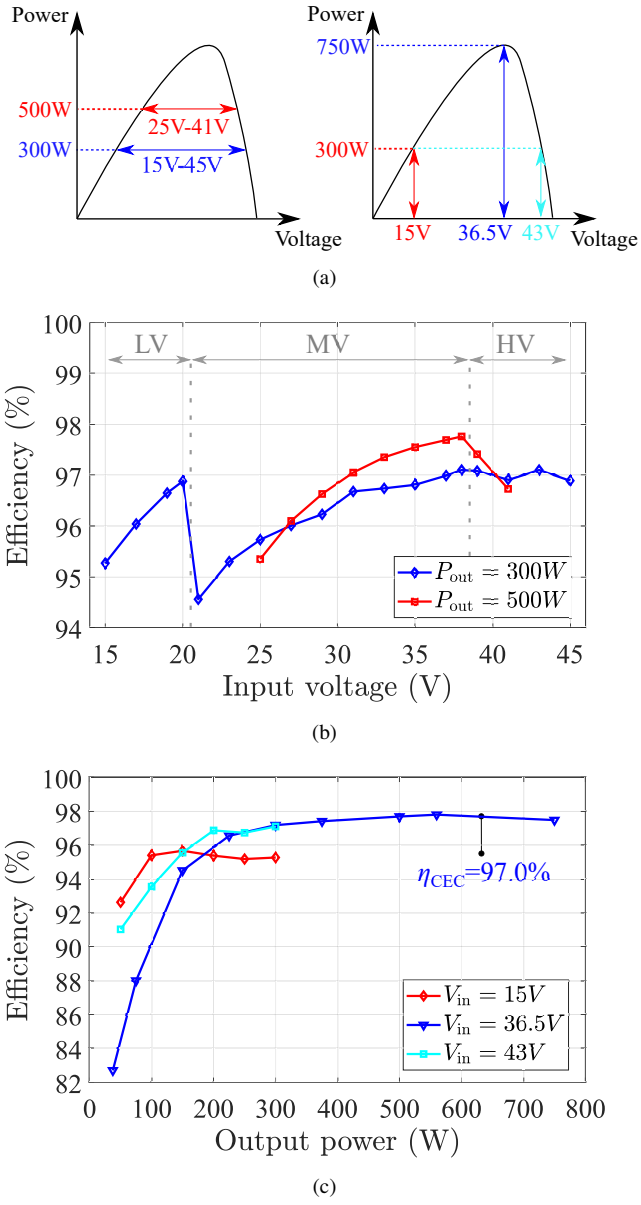


Figure 6: Main simulation results of the proposed converter efficiency as function of the operating power and input voltage. (a) Efficiency as function of the input voltage, at two representative working powers (300 W and 500 W) (b) Efficiency as function of the operating power, at three representative input voltages (15 V, 36.5 V and 43 V).

architecture that exploits an unbalanced power splitting between a resonant LLC and a boost operating in BCM. The analysis of converter stresses and the main design equations are presented in this work. Preliminary simulations results prove that the proposed converter achieves a high conversion efficiency over a wide input voltage range (always > 94.5% at 300 W in the 15 V – 45 V range), with an efficiency peak in the neighbourhood of the desired rated voltage. One of the main potential limitations is the relatively high number of active devices in the converter, which may deteriorate the

Table V: Comparison of the proposed power optimizer with other state of the art solutions.

Reference	[3]	[4]	[5]	[6]	[8]	[9]	[10]	[11]	Proposed
Step-up technique	Voltage Multipliers	Voltage multipliers, switched capacitors	Multi-mode LLC	Multi-mode LLC	Topology-morphed LLC	Symmetric IPOS	Symmetric IPOS	Symmetric IPOS, Voltage Multipliers	Multi-mode asymmetric IPOS
Isolation	No	No	Yes	Yes	Yes	No	Yes	No	No
Number of switches	4	1	5	5	6	2	4	2	9
Number of diodes	7	8	2	2	7	7	12	5	2
Number of magnetic components	6 (ind.)	1 (coupled ind.)	1 (transf.)	1 (transf.), 1 (coupled ind.)	1 (transf.)	2 (ind.)	4 (transf.), 4 (ind.)	2 (coupled ind.)	1 (transf.), 1 (ind.)
Number of capacitors	9	8	4	5	8	7	5	6	6
Rated power	1 kW	200 W	300 W	300 W	300 W	250 W	1 kW	400 W	750 W
Input voltage range	25 V – 40 V	25 V – 40 V	22 V – 36 V	10 V – 60 V	20 V – 50 V	10 V	30 V	20 V – 30 V	15 V – 45 V
Min / max efficiency in the voltage range	97.2% – 97.9% (1 kW)	92.7%–95% (200 W)	95.5% – 97.6% (300 W)	79%–97.4% (custom power profile)	94.5% – 95.5% (300 W)	91% (250 W, sim.)	N/A	95.8% (200 W)	94.6% – 97.1% (300 W, sim.)

reliability of the converter and increase its cost compared to other solutions. For these reasons, the future steps of this work include the design optimization of the converter based on the minimization of the Levelized Cost of Energy (LCOE) and constrained by reliability criteria. The performances of the proposed PPO will be measured on an experimental prototype.

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