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Modelling of a Multi-Period Damped Resonant DC-DC Converter with Capacitive Isolation

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***Abstract*—A new step-down Multi-Period Damped Resonant (MPDR) DC-DC converter for Capacitive Power Transfer (CPT) is proposed in this article for a grid adapter. The proposed solution is based on a Series Resonant Converter that exploits multiple resonant periods for the power transfer. In this way, it is possible to reduce the size of the resonant passive components while operating at lower switching frequencies, to reduce the impact of the switching losses of the active devices. Compared to other CPT solutions, the converter exploits a unique inductor as compensation network, improving the power density and reducing the design complexity. The converter operation and its analytical modelling based on a first-harmonic approximation modified with time-domain corrections are illustrated. The article includes a generalized design procedure to size the resonant inductance and select the switching frequency in order to produce the desired output voltage, and simultaneously achieve the ZVS turn-ON of the input FETs. The proposed model is validated in simulation and experimentally, showing high accuracy in both the operating modes of the converter.**

***Index Terms*—Capacitive Power Transfer, DC-DC conversion, Laptop charger, Power Converter Modelling, Series Resonant Converters.**

I. Introduction

In the last few years, power converters based on Capacitive Power Transfer (CPT) have become a popular alternative to Inductive Power Transfer (IPT) to provide the galvanic isolation in applications requiring high power density and conversion efficiency, such as portable devices chargers [1].

The state of the art solutions for power grid adapters exploit multiple techniques to meet the required high step-down voltage gain from the rectified grid with a low component count. Some of them are based on buck-derived single-switch topologies such as the Single-Stage-Single-Switch (S4) converter [2] or the Integrated-Buck-Buck-Boost (IBuBuBo) [3]. Despite the high peak efficiencies above 88 %, the active switch is subjected to a high voltage stress and operates in hard-switching. Another transformerless solution is the Semi-Quadratic Buck converter in [4], which is proved to exhibit improved step-down voltage gain and Total Harmonic Distortion (THD) compared to the conventional Buck converter. The hard-switching operation, which bounds the switching frequency below 100 kHz, and the presence of multiple inductors and filter capacitors limit the power density of these Pulse-Width-Modulated (PWM) solutions.

To simultaneously increase conversion efficiency and power density, resonant converters based on high-frequency transformers and Wide-Bandgap devices (WBG) have recently become popular in many applications [5], [6], thanks to the superior performances compared to Silicon devices [7]. Solutions relying on Inductive Power Transfer (IPT) exploit the transformer turns ratio as a degree of freedom to provide the required voltage gain and the parasitic magnetizing inductance to achieve the zero-voltage switching of the input power devices. In this cases, the transformer typically represents the bottleneck for the conversion efficiency [6], [7]. In contactless chargers, moreover, IPT converters suffer of high sensitivity to misalignment between primary and secondary coil [8].

Capacitive Power Transfer (CPT) converters, on the other hand, exploit two isolating capacitors to transfer power through a high-frequency electrical field, and are typically lighter and more tolerant to misalignments [9]. CPT-based converters are gaining attention in a variety of applications, from low power [10] to high power charging systems [11]. One of the main limitations of conventional CPT converters is the adoption of complex compensation networks at both primary and secondary sides, and the dependence of the resonant frequency on the passive components tolerances [12].

In this work, to overcome some of the above-mentioned limitations of the state of the art power grid adapters, a frequency-modulated Series Resonant Converter (SRC) based on a Multi-Period Damped Resonance (MPDR) is proposed, allowing to simplify the compensation network to a single inductor and to limit the negative impact of components tolerances. Compared to a conventional SRC, the active devices of the converter (GaNFETs) operate at a lower switching frequency than the resonance frequency. This approach allows at the same time to reduce the size of the passive components, designed to resonate at a higher frequency, without increasing the switching losses of the active devices: as a result, it provides a potential solution to increase both the conversion efficiency and power density.

The rest of the article is divided as follows: Section II describes the operating principle and the mathematical modelling of the proposed MPDR-SRC, Section III presents a generalized

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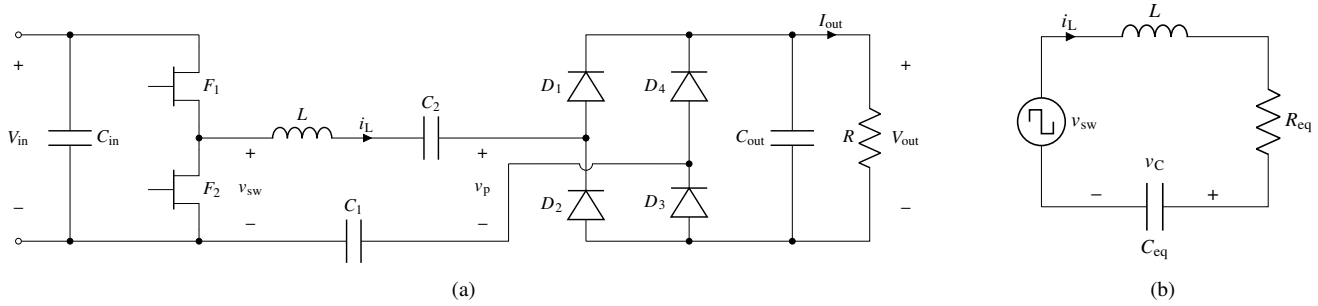


Figure 1: (a) Full schematic of the proposed converter; (b) Schematic of the equivalent SRC.

approach to design the resonant tank and select the switching range so as to achieve the desired output voltage and the ZVS turn-ON of the input power devices, while Section IV presents the experimental validation of the modelling at a reduced voltage operation.

II. Converter operation and modelling

The proposed MPDR-SRC topology is shown in Fig. 1a. It includes a half-bridge inverter (F_1 and F_2), the resonant tank (composed by the two isolating capacitors $C_1 = C_2 = C$ and the resonant inductor L, which resonate at f_{res}) and a diode-bridge rectifier (D_{1-4}). Filter capacitors C_{in} and C_{out} are added to stabilize the input and output voltages, respectively. For the description of the converter steady-state operation, the following assumptions are considered:

- V_{in} and V_{out} are assumed to be constant during a switching cycle;
- the half-bridge FETs are ideal;
- the dead time is assumed to be negligible compared to the duration of a switching period;
- the rectifier diodes are ideal, except for their forward conduction voltage V_γ.
- the passive components of the resonant tank, namely L and the isolating capacitors C, are ideal.

The FETs F_1 and F_2 switch at frequency f_{sw} (with $f_{sw} \ll f_{res}$), 50 % duty cycle and 180° phase shift, so that v_{sw} assumes a square wave behaviour and the converter operation is symmetric in the two halves of the period. For modelling purposes, the First-Harmonic Approximation (FHA) is applied to the simplified SRC shown in Fig. 1b, in which the isolating capacitances are replaced by an equivalent capacitor $C_{eq} = \frac{C}{2}$ and the rectifier input behaves as an equivalent resistive load R_{eq}. Instead of the conventional $R_{eq} = \frac{8}{\pi^2}R$ [14], the rectifier efficiency $\alpha_\gamma = \frac{1}{1+\frac{2V_\gamma}{V_{out}}}$ is included to provide a more accurate expression of R_{eq}:

$$R_{eq} = \frac{\frac{4}{\pi}\left(RI_{out} + 2V_\gamma\right)}{\frac{\pi}{2}I_{out}} = \frac{8}{\pi^2}\frac{R}{\alpha_\gamma}. \tag{1}$$

Notice that, with the made assumptions, the other contributions of resistive losses in the SRC loop are considered to be negligible compared to R_{eq}. Once R_{eq} is defined, the converter operation is fully described by the second-order differential equation in (2), characterized by $\omega_{res} = \frac{1}{\sqrt{LC_{eq}}}$ undamped resonance frequency and $\gamma = \frac{R_{eq}}{2L}$ damping coefficient:

$$\begin{cases} \frac{d^2v_C}{dt^2} + \frac{R_{eq}}{L}\frac{dv_C}{dt} + \omega_{res}^2 v_C = \omega_{res}^2 V_{in} \\ v_C(0) = V_0 \\ \frac{dv_C}{dt}(0) = \frac{i_L(0)}{C_{eq}} = \frac{I_0}{C_{eq}} \end{cases}. \tag{2}$$

Assuming an underdamped resonance operation ($L\omega_{res} > R_{eq}$), the solutions $i_L(t)$ and $v_C(t)$, parametrized by the unknown initial conditions V_0 and I_0, are expressed in (3) and (4), respectively.

$$i_L(t) = e^{-\gamma t}\left[\left(\frac{V_{in}-V_0}{\omega_{res}L} - \frac{\gamma}{\omega_{res}}I_0\right)\sin(\omega_{res}t) + I_0\cos(\omega_{res}t)\right] \tag{3}$$

$$\begin{aligned} v_C(t) = V_{in} + e^{-\gamma t}\Bigg[&\left(\frac{\gamma}{\omega_{res}}(V_{in}-V_0) + \omega_{res}LI_0\right)\sin(\omega_{res}t) \\ &- (V_{in}-V_0)\cos(\omega_{res}t)\Bigg] \end{aligned} \tag{4}$$

The time-domain expressions of $i_L(t)$ and $v_C(t)$ show that the sinusoidal waveforms, in each half period, are damped by the exponential term $e^{-\gamma t}$. For sufficiently high quality factors, the oscillations do not get extinguished by the end of the half period, and this condition is referred to as Partially Damped Oscillations (PDO) mode. The main SRC waveforms in this operating mode are qualitatively shown in Fig. 2a. For very high quality factors ($L\omega_{res} \gg R_{eq}$), the waveforms collapse to sinusoids (undamped resonant operation).

On the other hand, for low quality factors (but still larger than 1) the oscillations are likely to be completely damped within the end of the half period, as shown in Fig. 2b. This condition occurs when the rectifier primary voltage $v_p(t)$ (shown in Fig. 1a) is not sufficient to forward-bias the rectifier diodes $D_1 - D_3$ (or $D_2 - D_4$) through the complete half switching cycle: as a result, the resonant oscillations get completely damped. In this article, this operating mode will be referred to as Completely Damped Oscillations (CDO) mode.

Notice that, contrarily to conventional SRC operated at resonance, in this converter the switching frequency f_{sw} is a degree of freedom and is selected to be $\ll f_{res}$, resulting in multiple resonant oscillations inside a switching period.

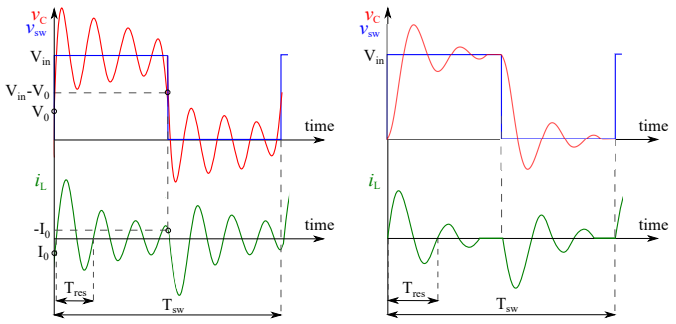


Figure 2: Qualitative waveforms of switching node voltage v_{sw}, capacitor voltage v_C and inductor current i_L of the equivalent SRC: (a) PDO mode; (b) CDO mode.

With this approach, it is possible to reduce the size of passive components in the circuit operating at high resonance frequencies (thus increasing the power density), while at the same time limiting the switching losses of the high-voltage FETs, which work at a lower f_{sw}.

Generalized analytical expressions of $V_0(f_{sw}, R)$ and $I_0(f_{sw}, R)$ (for both the PDO and CDO mode) can be derived exploiting the symmetric operation of the converter, as shown qualitatively in Fig. 2a:

$$\begin{cases} i_L\left(\frac{T_{sw}}{2}\right) = -i_L(0) = -I_0 \\ v_C\left(\frac{T_{sw}}{2}\right) = V_{in} - v_C(0) = V_{in} - V_0 \end{cases} . \tag{5}$$

The combination of (3)–(4) and (5) leads to closed-form expressions of I_0 and V_0:

$$\begin{cases} I_0 = -\frac{V_{in}}{\omega_{res} L} \frac{B_{fR}}{A_{fR}^2 + B_{fR}^2} \\ V_0 = V_{in}\left(1 - \frac{A_{fR}}{A_{fR}^2 + B_{fR}^2}\right) \end{cases} , \tag{6}$$

where, for compactness of notation:

$$A_{fR} = 1 + e^{-\frac{\gamma}{2f_{sw}}}\left[-\frac{\gamma}{\omega_{res}}\sin\left(\pi\frac{f_{res}}{f_{sw}}\right) + \cos\left(\pi\frac{f_{res}}{f_{sw}}\right)\right] \tag{7}$$

$$B_{fR} = e^{-\frac{\gamma}{2f_{sw}}}\sin\left(\pi\frac{f_{res}}{f_{sw}}\right) \tag{8}$$

The ideal static characteristic is the result of the integral of the instantaneous power transferred at the switching port:

$$\begin{aligned} P_{in}(f_{sw}, R) &= \frac{1}{T_{sw}}\int_0^{T_{sw}} v_{sw}(t)\cdot i_L(t)dt \\ &= C_{eq} f_{sw} V_{in}\left(V_{in} - 2V_0(f_{sw}, R)\right) . \end{aligned} \tag{9}$$

In the CDO mode, it is easily proved from (7) and (8) that $I_0 \to 0$ (thus the FETs turn ON at zero current) and $V_0 \to 0$. This result provides a mathematical proof of the completely damped oscillations operation. A relevant consequence is that (9) collapses to a linear function of f_{sw} that is independent of the load:

$$P_{in}(f_{sw}) = C_{eq} f_{sw} V_{in}^2 . \tag{10}$$

It is possible to prove from (9) that, in the PDO mode, the static characteristic exhibits local power peaks at the odd sub-harmonics of f_{res} ($\frac{f_{res}}{2n+1}$, $n \in \mathbb{N}$), and local power minima at the even sub-harmonics ($\frac{f_{res}}{2n}$, $n \in \mathbb{N}$). At increasing load resistances, however, the increased damping eliminates the effect of the resonant oscillations and the power-frequency characteristic tends to become linear, as correctly predicted by (10). Independently on the working mode, the output voltage can be derived from the input power as:

$$V_{out} = \sqrt{R P_{in}(f_{sw}, R)} . \tag{11}$$

Table I: Rated design specifications of the converter.

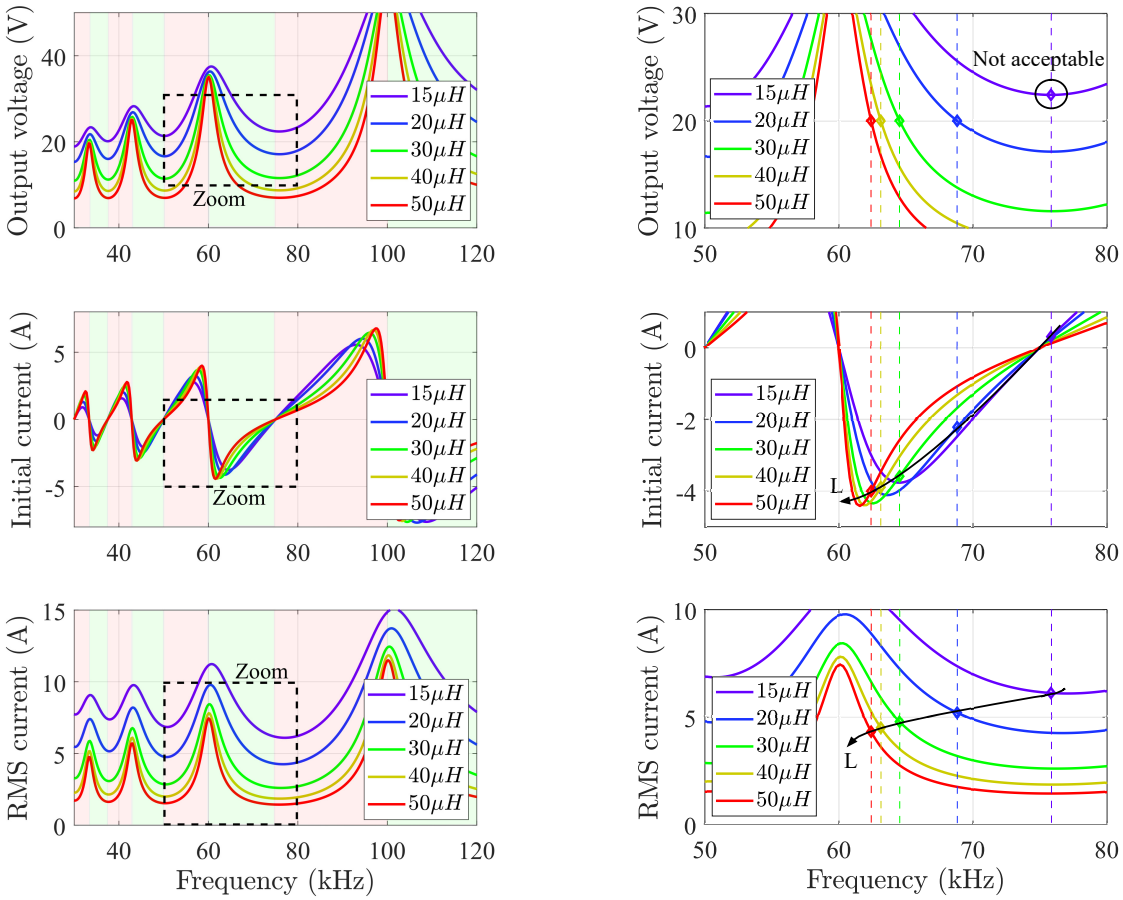
Specification	Value
V_{in}	330 V
V_{out}	20 V
P_{out}	60 W

III. Design

The complete analytical modelling of the converter operation allows to derive a detailed design procedure for the resonant tank and the switching frequency range for a given set of specifications. The goal of the design is the optimization of efficiency and power density for the given rated specifications. In the present case, a grid adapter is designed for the specifications reported in Tab. I, which are typical of a laptop charger. Although the CDO mode allows a load-independent power transfer, higher conversion efficiencies can be achieved when the converter operates in the PDO mode: with a proper design, as explained in this section, it is possible to achieve the ZVS commutation of the input FETs at rated operation, to reduce the switching losses. For this reason, the following design steps are based on the analytical equations referred to the PDO case, namely (3), (6) and (9). The proposed design procedure is here illustrated step by step:

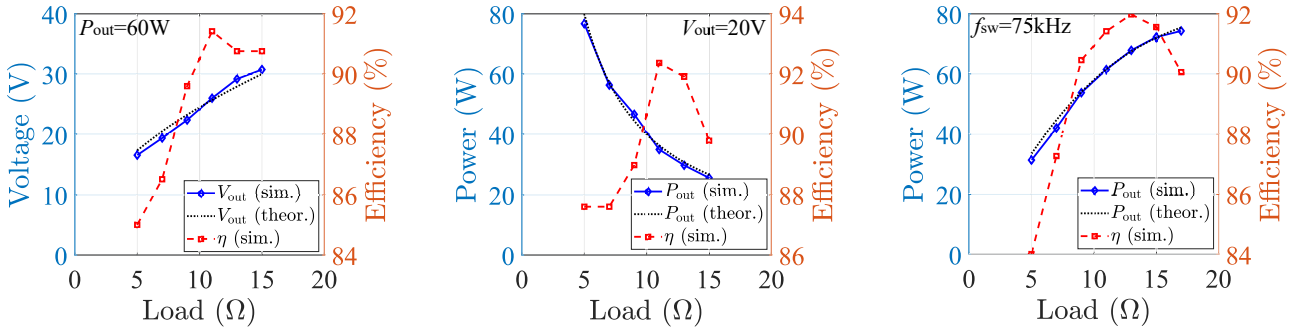
1) identify the rated design specifications: V_{in}, V_{out}, $R = \frac{V_{out}^2}{P_{out}}$;
2) make some preliminary design choices on the resonance frequency and capacitance range. In the present case, $f_{res} = 300\,\text{kHz}$ and C is selected in the $10\,\text{nF} - 50\,\text{nF}$ range. The resulting inductances to satisfy the resonance frequency range approximately between $10\,\mu\text{H}$ and $50\,\mu\text{H}$. This choice may be corrected in the following steps if no solution meets the ZVS and output voltage requirements simultaneously;
3) select the FETs and identify their equivalent output capacitance $C_{oss,eq}$. In order to achieve the ZVS turn-ON of the high-side FET, the energy stored in the inductor at the beginning of the switching period must satisfy (12):

$$I_0 < -V_{in}\sqrt{\frac{2C_{oss,eq}}{L}} \tag{12}$$



(a) (b)

Figure 3: Output voltage V_{out}, inductor initial current I_0 and inductor RMS current I_{RMS} as function of frequency, for different values of inductance L and fixed resonance frequency 300 kHz. (a) Identification of the frequency intervals for which $I_0 < 0$ A (highlighted in green) and $I_0 > 0$ A (highlighted in red). (b) Zoom on the 50 kHz – 80 kHz range and identification of the I_0 and I_{RMS} occurring at $V_{out} = 20$ V. Notice that a larger L increases the absolute value of I_0 (higher turn-OFF losses) and at the same time reduces the RMS current (lower conduction losses). Inductances below 20 µH do not allow to achieve $V_{out} = 20$ V in the selected frequency range.



(a) (b) (c)

Figure 4: Simulated output voltage or power and converter efficiency as function of the load resistance at: (a) Fixed output power ($P = 60$ W); (b) Fixed output voltage ($V_{in} = 20$ V); (c) Fixed frequency ($f_{sw} = 75$ kHz).

4) evaluate $I_0(f_{sw})$ at the rated load and for various inductance values and identify the frequency ranges for which $I_0 < 0$ (green bands in Fig. 3a). These frequency ranges are good candidates for the achievement of the ZVS. From (6), it's possible to prove that:

$$I_0(f_{sw}) < 0 \iff \frac{f_{res}}{2k+1} < f_{sw} < \frac{f_{res}}{2k}, k \in \mathbb{N}. \quad (13)$$

Among the available options, an intermediate frequency range should be selected, which ensures a good trade-off between turn-OFF losses of the input FETs and ZVS margin at lighter load conditions. In the present case, the 60 kHz – 75 kHz range is considered;

5) evaluate $V_{out}(f_{sw})$ from (11) and determine the inductances which allow to achieve $V_{out} = 20\,V$ within the selected frequency range (as shown in Fig. 3b, top pane). In the present case, there is no solution for $L < 20\,\mu H$. At the same time, the inductance should be sufficiently large to meet (12) at the 20 V frequency.

6) further considerations can be done on the selection of the inductance once the minimum bound is determined. A larger L (higher quality factor) increases the initial current I_0 and thus increases the turn-OFF losses of the half-bridge FETs. On the other hand, a lower L (lower quality factor) increases the RMS current of the tank but, in general, allows to decrease the inductor losses. An approximated expression for the RMS current of the inductor can be derived from (3) assuming an undamped sinusoidal waveform:

$$I_{L,RMS} \approx \frac{1}{\sqrt{2}}\sqrt{\left(\frac{V_{in}-V_0}{\omega_{res}L} - \frac{\gamma}{\omega_{res}}I_0\right)^2 + I_0^2} \quad (14)$$

The behaviours of I_0 and $I_{L,RMS}$ for various inductor values are represented in Fig. 3b (middle and bottom panes, respectively).

In the present case, it is possible to prove that the minimum L achieving the voltage and ZVS requirements at the rated load is 18 µH. From the analysis performed in Section II, a lighter load results in lower I_0, making it more difficult to achieve the ZVS turn-ON for the same selected inductance. As a result, for a more conservative design, the presented procedure could be repeated for a reduced output power. Clearly, the final design should be adjusted on the basis of the available commercial capacitors. The proposed modelling and design were validated by an experimental prototype employing the components listed in Tab. II.

The input FETs should be selected according to the maximum voltage stress ($V_{in} = 330\,V$). The designed prototype employs 650 V GaNFETs to reduce the switching losses, thanks to the reduced gate capacitance compared to Silicon MOSFETs for the same rated voltage. 630 V, 22 nF Multi-Layer Ceramic Capacitors (MLCC) were selected for the isolating capacitors. Their minimum voltage rating can be derived from (4). A custom inductor was realized with a toroidal core and 25 turns, resulting in $L = 28.5\,\mu H$.

Table II: Main components of the prototype.

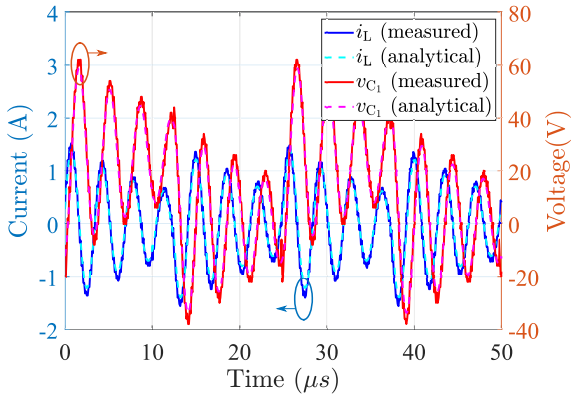
Prototype component	Part number
FETs $F_{1,2}$	SGT120R65AL
Capacitors C (22 nF)	C3225C0G2J223K230AA
Inductor L (28.5 µH)	Custom (Kool Mµ core, 25 turns)
Rectifier diodes D_{1-4}	STPS5L60
Input capacitor (680 µF)	B43642



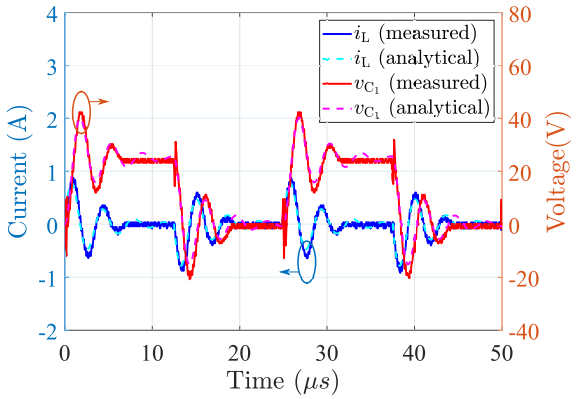
Figure 5: Picture of the prototype.

The core material and shape were selected so as to keep the temperature increase of the inductor below 40 °C in the worst-case operation. The adopted L and C resonate at $f_{res} \approx 284$ kHz. The present design is proved to satisfy the ZVS requirement for $P_{out} \geq 40$ W. 60 V, 5 A Schottky diodes were employed for the output rectifier. Finally, a 680 µF electrolytic capacitors was selected to stabilize the DC rail voltage.

Fig. 4 shows some simulations results extracted on LTSpice [13] performed with the Spice models of the same components of the prototype. The primary goal of the simulations was to validate the mathematical modelling and refining the design so as to optimize the conversion efficiency at the rated power condition. All the simulations refer to the nominal input voltage condition, $V_{in} = 330\,V$, and were performed at multiple load conditions, to analyze the converter performances in a realistic charging scenarios. Fig. 4a shows the output voltage (analytical from (11) and simulated) and the conversion efficiency at rated power operation ($P = 60$ W). At each load condition, f_{sw} was manually adjusted to maintain a constant output power. Intuitively, for the same power, an increasing load resistance results in a higher efficiency, thanks to the lower conduction losses in all the components. Fig. 4b shows output power and efficiency variations at fixed output voltage, $V_{out} = 20\,V$. The efficiency curve is affected by two concurrent effects of the load variation: an increasing load resistance reduces the conduction losses, but also decreases the possibility to achieve the ZVS of the GaNFETs. Fig. 4c shows output power and efficiency at fixed frequency operation, $f_{sw} = 75$ kHz. In this case, an increasing load resistance modifies both output voltage and power simultaneously. The simulated output power

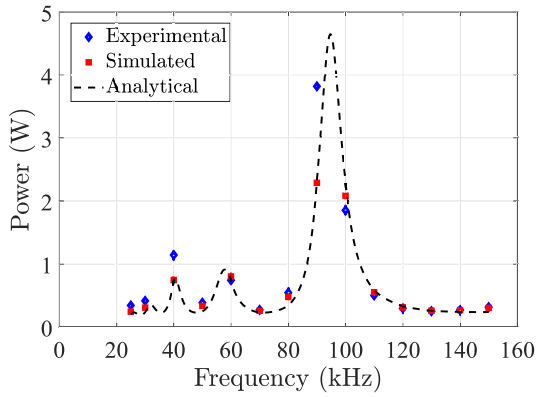


(a)

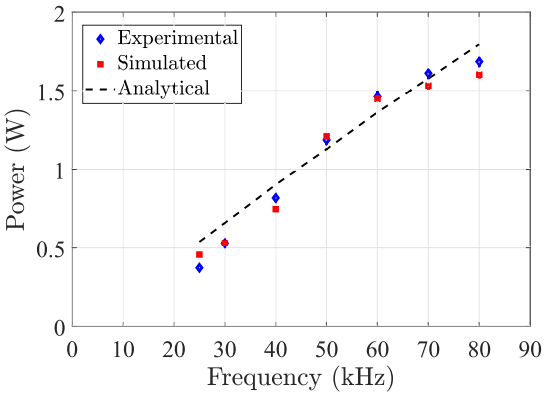


(b)

Figure 6: Comparison of analytical, simulated and experimental inductor current and C_1 capacitor voltage waveforms at f_{sw} = 40 kHz, at reduced voltage operation: (a) PDO mode (V_{in} = 50 V, R = 3 Ω); (b) CDO mode (V_{in} = 50 V, R = 30 Ω).



(a)



(b)

Figure 7: Comparison of analytical, simulated and experimental static characteristics $P(f_{sw})$ at reduced voltage operation: (a) PDO mode (V_{in} = 50 V, R = 3 Ω); (b) CDO mode (V_{in} = 50 V, R = 30 Ω).

is compared with the analytical model expressed in (9), which shows high fitting accuracy.

IV. Experimental Validation

A prototype was built according to the proposed design approach and for the specifications in Tab. I. The top-layer view of the PCB prototype is shown in Fig. 5. The DC-link electrolytic capacitor C_{in} and the toroidal core resonant inductor represent the most critical components to the converter power density and could be objects of further improvements. The inductor design, for instance, significantly affects both power density and conversion efficiency. The adoption of an air-core inductor would eliminate the core losses associated to the high frequency magnetic field. At the same time, however, the large number of turns required for the minimum inductance to meet the output voltage and ZVS requirements would result in a bulky inductor [9].

Fig. 6 shows the preliminary experimental validation of the modelling at scaled-down operation (V_{in} = 50 V). Figs. 6a and 6b compare the experimental and analytical waveforms of i_L and v_{C_1}, in a PDO and CDO mode condition, respectively. In the CDO mode case, a time-domain correction is applied to take into account the discontinuity of current in the definition of R'_{eq}, similar to the approach adopted in [15] for LLC converters:

$$R'_{eq} = 2n_{periods}\frac{f_{sw}}{f_{res}}R_{eq}\,, \tag{15}$$

where $n_{periods}$ is the number of resonant periods inside a half switching cycle, during which there is an effective power transfer. The modified FHA model corrected with (1) and (15) provides a very accurate description of the circuit waveforms.

Figs. 7a and 7b compare the experimental and simulated static characteristics in the CDO and PDO modes with the analytical results provided by (10) and (9), respectively. The results refer to a scaled-down voltage operation, as in Fig. 6. The time-domain corrections (1) and (15) are still taken into account to improve the fitting. As explained in Section II, the static characteristic exhibits power peaks and valleys in the PDO mode, and a linear behaviour in the CDO mode. The measurements prove that the proposed analytical modelling

Table III: Comparison of the proposed DC-DC converter with the state of the art solutions for grid adapter.

Reference	Converter type	Active switches	Diodes	Magnetic components	Capacitors	Switching technique	Output power / voltage
[2]	Buck-derived	1	3	3 inductors	3	Hard switching	100 W/19 V
[3]	Buck-derived	1	3	3 inductors	3	Hard switching	100 W/19 V
[4]	Buck-derived	2	3	2 inductors	3	Hard switching	65 W/24 V
[6]	IPT	4	0	1 transformer - 1 inductor	3	Soft switching	170 W/28 V – 42 V
[7]	IPT	3	0	1 transformer	3	Soft switching	90 W/19.5 V
[8]	IPT	4	4	1 transformer	3	Soft switching	100 W/20 V
[9]	CPT	2	4	1 inductor	4	Soft switching	90 W/19.5 V
Proposed	CPT	2	4	1 inductor	4	Soft switching	60 W/20 V

well-fits the experimental converter operation and may serve the purpose of a closed-loop controller design.

Tab. III compares the proposed MPDR-SRC with some of the most recent step-down grid adapters, in terms of number of components, rated specifications and switching technique. Compared to buck-derived topologies, the proposed converter exhibits a lower number of inductors and filter capacitors, resulting in an improved power density. In addition, the soft-switching operation should result in an improved conversion efficiency. The IPT-based topologies and the CPT charger in [9] are all based on a high-frequency resonant operation of the converters FETs. For the same rated power and FET selection, the proposed converter is expected to exhibit reduced FET losses thanks to the exploitation of the multi-period resonant power transfer. A thorough experimental validation at rated voltage operation will be part of the future development of this work.

V. Conclusions

The analytical modelling and preliminary experimental validation of a capacitively isolated DC-DC converter for grid adapter applications has been presented. The converter operates as a series resonant converter that exploits multiple resonant periods to transfer power. With this approach, it is possible to achieve a high power density by employing a high frequency resonance tank, at the same time reducing the switching losses of the active switches, which operate at lower frequency. The FHA-based analytical modelling exploits time-domain corrections to improve the mathematical description on a wide range of load resistances and switching frequencies, and is suited for the design of a closed-loop controller. Simulations and preliminary experimental tests on a prototype at scaled-down voltage conditions validate the accuracy of the modelling in both the operating modes of the converter.

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