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Engineering Discrete Simulated Bifurcation for an FPGA Digital Ising Machine

Fabrizio Orlando*, Deborah Volpe*, Giacomo Orlandi*,
Fabrizio Riente*, Marco Vacca* and Mariagrazia Graziano†

*Department of Electronics and Telecommunications, Politecnico di Torino Italy

†Department of Applied Science and Technology, Politecnico di Torino Italy

fabrizio.orlando@studenti.polito.it, deborah.volpe@polito.it, giacomo.orlandi@polito.it,

fabrizio.riente@polito.it, marco.vacca@polito.it and mariagrazia.graziano@polito.it

Abstract—Simulated Adiabatic Bifurcation (aSB) is a quantum-inspired algorithm that provides approximate solutions for large-scale optimization problems using the Ising model. It emulates the quantum adiabatic evolution of a network of non-linear Kerr oscillators on classical platforms. These oscillators undergo bifurcation, where each branch corresponds to a spin state, with the network creating an energy imbalance to determine the optimal solution.

This approach is highly parallelizable, making it suitable for implementation on GPUs and FPGAs. However, classical emulation introduces analog errors, potentially compromising performance. To address this, alternative methods like ballistic (bSB) and discrete (dSB) evolutions were developed, with the ballistic approach further enhanced by thermal fluctuations (HbSB).

Our comprehensive analysis of bSB, dSB, and HbSB using benchmark Max-Cut and knapsack problems aimed to identify the best balance of speed, area, and accuracy. We found that fixed-point number representation allows more algorithm iterations within the same timeframe as floating-point representation. The proposed FPGA architecture implements dSB and its heated version, leveraging high parallelizability and efficient memory organization. This design supports larger coefficients and improves problem-solving efficiency without multipliers for matrix-vector evaluation.

Challenges include mitigating data dependency between matrix-vector multiplication and time evolution, and developing a preconditioning method for adapting problem coefficients, making the architecture suitable for real-world applications and potential ASIC release.

Index Terms—Ising Machines, Simulated Bifurcation, Quadratic Unconstrained Binary Optimization, quantum-inspired optimization, Ising

I. INTRODUCTION

Simulated Adiabatic Bifurcation (aSB), a quantum-inspired algorithm introduced in [1], offers approximate solutions of large-size optimization problems written according to Ising formulation, which is equivalent to Quadratic Unconstrained Binary Optimization (QUBO) model. It emulates on classical platforms the quantum adiabatic evolution of a non-linear-Kerr-oscillators network. These oscillators exhibit a bifurcation during their evolution, and each branch can be associated with a spin state. The problem is encoded by associating an oscillator with each spin variable, and the spin interactions are expressed through the network, whose role is to create an imbalance in the energy of the systems such that the optimum

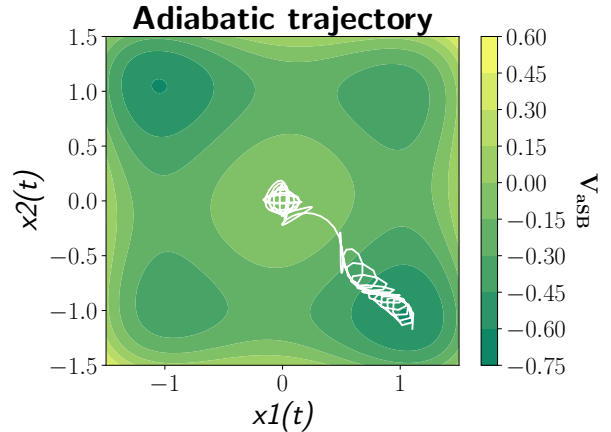


Fig. 1: Simulated Adiabatic Bifurcation (aSB) evolution for a 2-spin max-cut problem starting from the origin. The trajectories of the two oscillators' network over time are illustrated by the white lines. The potential energies at the final time are also depicted (V_{aSB} , V_{bSB} and V_{dSB}).

of the problem corresponds to the final ground state, forcing each oscillator to choose the branch representing the spins state of the problem solution (Figure 1). A key advantage of this approach is the high level of parallelizability in simulating the system evolution, which promotes its hardware implementations such as on Graphics Processing Unit (GPU) and Field Programmable Gate Array (FPGA).

However, the mathematical model employed for emulating the adiabatic evolution of the system classically generates some analogue errors, potentially compromising performance. In response, alternative approaches like the ballistic (bSB) and discrete (dSB) evolution of the network were introduced in [2]. The bSB can be further enhanced by introducing a thermal fluctuation term (HbSB) for escaping from local minima [3].

II. METHODOLOGY AND PROPOSED IMPLEMENTATION

We conducted a comprehensive analysis of bSB, dSB, and HbSB through proper software models, focusing on benchmark maxcut and knapsack problems. The analysis aimed to identify the algorithm guaranteeing the best compromise among speed, area and results accuracy for proposing a new digital architecture for FPGA and to achieve the best number

