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Oscillatory Circuits With a Real Non-Volatile Stanford Memristor Model

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ABSTRACT Stanford memristor model is a widely used model that accurately characterizes real non-volatile metal-oxide resistive random access memory (RRAM) devices with bipolar switching characteristics. The paper studies for the first time the dynamics and bifurcations in a class of nonlinear oscillators with *real non-volatile memristor devices* obeying Stanford model. This is in contrast with papers in the literature considering oscillators with ideal, abstract, or artificial memristor models, that are unable to describe physical memristors implemented in nanotechnology. One main new idea in the paper is to use the memristor as a *programmable nonlinear resistor*. Namely, two principal modes of operation are considered. 1) Analogue transient phase: the oscillator is designed so that in the transient oscillations the voltage on the memristor is below threshold, hence the main memristor state variable, i.e., the gap of the insulating material, is almost constant and the memristor behaves as a static nonlinear resistor. 2) Programming phase: the nonlinear characteristic of the memristor, which depends on the gap, can be changed via the application of voltages above threshold. The paper studies nonlinear oscillations in the transient phase for a fixed gap as well as the bifurcations phenomena displayed when the gap is varied. The paper also discusses the differences between the approach in the paper and those to design other memristor oscillators with non-volatile memristors.

INDEX TERMS Bifurcations, Chua's circuit, complex dynamics, memristor, Stanford model.

I. INTRODUCTION

Oscillatory circuits with memristors have attracted a widespread interest in recent years [1]–[12]. Due to the rich dynamics guaranteed by the presence of memristors, such circuits are considered more effective candidates than traditional nonlinear *RLC* circuits to implement the core dynamics of reservoir computing systems [13] or to obtain sources of controllable chaotic behavior to incorporate into neural-inspired future computational systems [8]. More generally, memristor circuits lend themselves as a promising tool to overcome some limitations of Von Neumann computing systems via the implementation of new in-memory, analogue and parallel (neuromorphic) computing paradigms [14], [15].

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When considering memristor oscillatory circuits, it is of importance to distinguish between *ideal memristors*, as those introduced in the original paper by Chua [16], and *generic or extended memristors* introduced by Chua and Kang in the seminal paper [17]. In the latter case, an additional fundamental dichotomy to take into account is between *volatile* and *non-volatile* memristor models [18]. Ideal memristors are mainly of theoretic interest. On the other hand, the importance of generic and extended memristors cannot be overemphasized, since they are used to model *real physical memristor* devices implemented in nanotechnology [16], [19]–[24].

Oscillatory circuits with *ideal memristors* have been investigated in several works (see, e.g., [1]–[4], [25]–[30], and references therein). The theory underlying the dynamic behavior in the ideal case is nowadays quite well understood. In fact, it has been shown in [9], [24], [31] that the state

space of circuits with ideal memristors is foliated in a continuum of invariant manifolds. On each manifold the dynamics is equivalent to that of an oscillator where the ideal memristor is replaced by a nonlinear resistor with the same shape of the nonlinear characteristic and there is also a constant forcing term depending on the manifold. As an example, Chua's circuit with an ideal memristor [31], [32] is seen to embed infinitely many different forced Chua's circuits where an additional parameter depending on the manifold can yield bifurcations even when the circuit parameters are held fixed (bifurcations without parameters).

The analysis of oscillatory circuits with *real memristors* modeled by generic or extended memristors is instead still in its infancy and it constitutes one of the major challenges in the current research. In the *volatile* case, to obtain oscillations, a passive memristor with an *S*-type locally active quasi-static $i - v$ characteristic is used. As in a typical Pearson-Anson oscillator, the memristor is biased via a suitable network in the locally-active region, i.e., in a branch of the characteristic with a negative differential resistance (NDR) [5], [6], [11], [12], [33]. It is worth to remark that NDR is observed in thermistors and other specific types of passive nanoscale devices, as NbO_x, VO_2, and TaO_x devices [34]. An interesting source of NDR is attributed to electro-physical processes such as Mott transition dynamics, see [8], [35], where it is used to obtain periodic oscillations, beating oscillations, action potentials (burst and bursting phenomena) and even chaos in a class of third-order memristor circuits.

Let us now consider the class of oscillators with real *non-volatile* memristors. It is known that in this case it is no longer possible to consider the memristor quasi-static characteristic and hence to rely on the concept of NDR for designing an oscillator (see, e.g., [36]). To the authors knowledge, only very few contributions on oscillatory circuits with real non-volatile memristors are available in the literature. As an example, [37] describes a jerk circuit, which is able to display complex dynamics, using a non-volatile Knowm memristor [7]. Similarly, [38] investigated the nonlinear dynamics and bifurcations in a modified Shinriki oscillatory circuit also using a Knowm memristor. We also mention the article [39] that reports on the design and experimental realization of a memristive frequency generator with digital logic gates, a single-supply voltage and a threshold-type non-volatile memristive device.

A variety of real memristor models has been put forward in the literature, depending on the realization, material and level of accuracy which is needed in the applications [19], [22], [23], [40]. One of the most popular models of real memristor devices is described by the *Stanford model* [19], [41]–[43]. This is a physics-based compact model of non-volatile metal-oxide resistive random access memory (RRAM) devices with bipolar switching characteristics. Stanford model, which corresponds to an extended memristor, is able to explain the

dynamic resistive switching phenomena observed in a broad range of devices and especially it can accurately capture dynamic effects as the apparent threshold effect, the voltage dependence of the switching time and the possibility to set multi-level conductances. The model concerns filamentary-type devices characterized by two state variables, i.e., the length g of the gap of the insulating material, and the temperature T of the filament tip. One main feature is the existence of a voltage *threshold* such that g and the memductance have almost negligible variations below the threshold, while the same quantities display very sharp variations above threshold.

In this paper, we study for the first time a class of memristor oscillators, obtained by a modification of Chua's circuit [44], where the memristor is a *real non-volatile extended memristor obeying Stanford model.* The oscillators are named Stanford memristor Chua's circuits (SMCCs). One main new idea in the paper is to design SMCC so that the memristor behaves as a *programmable nonlinear resistor*. Namely, we consider the behavior of SMCC under two main operation modes.

1) *Transient phase (sub-threshold behavior):* We ensure that during the transient oscillations the voltage on the memristor stays below threshold and hence the *gap g remains almost constant* and the memristor behaves as a *static nonlinear resistor* with a hyperbolic sine characteristic (see Section IV for the details).
2) *Programming phase (supra-threshold behavior):* The nonlinear memristor characteristic depends upon g, that can be suitably programmed using for instance voltage pulses above threshold.

Goal of the paper is to study via analytic and numerical means the nonlinear dynamics of SMCC during the transient phase for fixed g and also the bifurcation scenario of SMCC when g is varied due to programming.

The paper differs from existing papers in the literature where the memristor oscillators use ideal, abstract, or artificial memristor models, that cannot accurately describe the behavior of real memristor devices implemented in nanotechnology [24]. The approach in the manuscript to implement an oscillator is also basically different from the quoted papers in the literature [7], [37], [39] where the oscillations are built upon the hysteresis loops displayed by the memristor in the $v - i$ plane. In that case, the memristor is not a programmable nonlinear resistor, rather the state variable undergoes wide variations during the transient oscillations. Then, the same state variable cannot be used as a bifurcation parameter and bifurcations are instead obtained via variations of circuit parameters. It is also worth to remark that, while in Chua's circuit the bifurcations are due to variations of a linear conductance [44], in SMCC we instead consider bifurcations due to variations of the nonlinear memristor characteristic.

II. STANFORD MEMRISTOR MODEL

The equations describing Stanford model of RRAM devices are given as follows [19], [41]–[43]

$$i = I_0 \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{v}{V_0}\right) \qquad (1)$$

$$\frac{dg}{dt} = -v_0 \left[\exp\left(-\frac{qE_{ag}}{kT}\right) \exp\left(\frac{qa_0\gamma}{\ell kT}v\right) \right.$$
$$\left. - \exp\left(-\frac{qE_{ar}}{kT}\right) \exp\left(-\frac{qa_0\gamma}{\ell kT}v\right) \right] \qquad (2)$$

$$\frac{dT}{dt} = \frac{vi}{C_{th}} - \frac{T - T_0}{\tau_{th}} \qquad (3)$$

where i and v are the current and voltage in the memristor device.

TABLE 1. Universal constants.

Symbol	Unit	Value	Description
k	J/K	1.38×10^{-23}	Boltzmann constant
q	C	1.6×10^{-19}	Elementary unit charge

A detailed discussion on the physical quantities and parameters involved in the model is available in [43] (see also Tables 1, 2). Here, we only remark that the considered devices have a typical structure with an oxide layer sandwiched between the top electrode and the bottom electrode. The switching mechanism is attributed to the formation/rupture of conductive filaments which may consist of oxygen vacancies. The SET process, i.e., the switching from the high-resistance state (HRS) to the low-resistance state (LRS) when a positive voltage is applied, is due to the dielectric soft breakdown and creation of conductive filaments in the oxide, while the RESET process during the application of a negative voltage, i.e., the switching from LRS to HRS, is due to the annihilation of the conductive filaments by Joule heating dissolution or electrochemical reactions involving oxygen ions or vacancies.

For simplicity, in the model, it is supposed that there is a single dominant 1D conductive filament, so that the internal state variable is the gap distance, g, defined as the average distance between the top electrode and the tip of the conductive filament. Actually, g has a lower and a upper limit g_{min} and g_{max}, respectively, i.e.,

$$g \in [g_{min}, g_{max}]$$

where g_{min} is reached when the tip of the conductive filament is nearly in contact with the top electrode during the SET, while g_{max} is the residual conductive filament during the RESET.

The current in the device is modeled using an electron tunneling conduction and it has an exponential relationship with respect to the tunneling distance, determined by g, and field strength, resulting in the quasi-static Ohm's law (1).

Quantity dg/dt is the gap growth/dissolution velocity depending on the applied voltage v and the net difference between the oxygen vacancy generation and recombination

rates. It is stressed that the role of temperature (T) is accounted for in the switching dynamics (cf. (2)). Again, to simplify the model, a lumped model of heat conduction based on Newton's law of cooling is adopted (cf. (3)), where τ_{th} denotes the effective thermal time constant and C_{th} the effective thermal capacitance. Finally, γ is a g-dependent local field enhancement factor, given by

$$\gamma = \gamma_0 - \beta \left(\frac{g}{g_\beta}\right)^3.$$

The first group of parameters a_0, E_{ar}, E_{ag}, ℓ, T_0, R_{th} and C_{th} are the so called 'process parameters' since they are dictated by the fabrication aspects, as device structure and material properties, and measurement setup. The second group I_0, g_0, V_0, v_0, g_β, γ_0, β and α are named 'switching parameters' since they describe the filament evolution. Especially, I_0, V_0 and g_0 dominate the nonlinear resistor $v - i$ curves, whereas v_0, γ_0, g_β, β and α describe the process of gap growth or dissolution, i.e., when the resistance starts to change. A general procedure to extract these parameters in order that the model behavior fits the experimentally observed $v - i$ curves and hysteresis loops is discussed in [43], [45].

Actually, RRAMs are naturally subject to a certain amount of variability which are due to the stochastic nature of formation and rupture of the conductive filament and gap size of multiple filaments. A feature of the Stanford model is the possibility to account for the intrinsic variability observed in resistive-switching devices (cycle-to-cycle and device-to-device) via the addition of suitable terms in the model. A technique to introduce and fit with the experiments an amount of variability in Stanford model is presented in [46].

For simplicity, in this first study, unless stated otherwise, we will not take into account parameter variations. In particular, we will refer to the numerical values of parameters in Table 2, that were obtained from experimental data of a set of HfO$_x$-based RRAM devices [43]. The treatment can of course be extended to other devices with similar characteristics but with a different set of parameters.

It is worth remarking that from a circuit theory viewpoint the Stanford model is developed in the framework of memristor devices. In particular, it corresponds to a *second-order extended memristor* [18] where the first equation is the quasi-static Ohm's conduction law and the two additional dynamic equations involve the internal state variables g and T. Henceforth, we will refer to the devices as memristors instead of using the name RRAMs.

A. HYSTERESIS LOOP AND APPARENT THRESHOLD

A standard configuration with a 1 transistor and 1 resistor (1T1R) can be used for the SET and RESET operation of the memristor [43]. The transistor is used to enforce a suitable value of the current compliance for electrical stress protection of the memristor. As discussed next, the compliance can also be used for continuous programming purposes.

TABLE 2. Model parameters.

| Symbol	Unit	Value	Description
a_0	m	0.25×10^{-9}	Atomic hopping distance
E_{ag}	eV	1.501	Activation energy for vacancy generation
E_{ar}	eV	1.5	Activation energy for vacancy recombination
ℓ	m	5.0×10^{-9}	Oxide thickness
g_{min}	m	0.1×10^{-9}	Minimum gap distance
g_{max}	m	1.7×10^{-9}	Maximum gap distance
I_0	A	6.14×10^{-5}	$i - v$ fitting parameter
g_0	m	2.75×10^{-10}	=
V_0	V	0.43	=
v_0	m/s	150	Gap dynamics fitting parameter
γ_0	–	16.5	=
g_β	m	1.0×10^{-9}	=
β	–	1.25	=
T_0	K	298	Ambient temperature
C_{th}	J/K	3.18×10^{-16}	Effective thermal capacitance
τ_{th}	s	2.3×10^{-10}	Effective thermal time constant
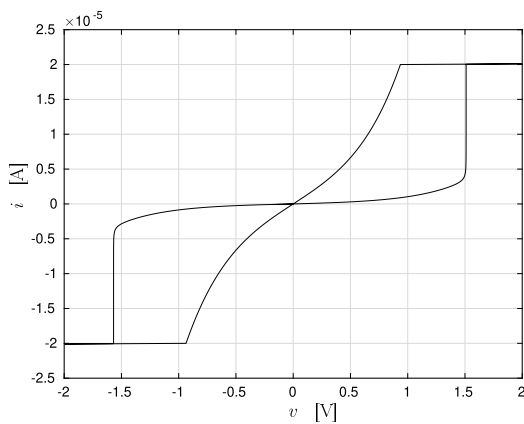
FIGURE 1. Hysteresis loop displayed by a 1T1R structure subject to a zero-mean triangular waveform with rate 4 V/s and peak voltage 2 V. The compliance current is ±20 μA.

Figure 1 illustrates a typical hysteresis loop when the 1T1R structure is subject to a zero-mean triangular waveform with rate 4 V/s and peak voltage 2 V and the compliance is set to ±20 μA. It is seen that there is an *apparent threshold voltage* related to the resistance switching. Below threshold, which in this case amounts to about 1.5 V, smooth changes in resistance are observed and the gap g is seen to remain almost constant, whereas when the voltage threshold is reached, very sharp gap and resistance changes occur. The threshold is related to the exponential dependence of the growth rate of g on applied voltage (cf. (2)) and the nonlinear tunneling effect.

B. MULTILEVEL CAPABILITY AND CONTINUOUS PROGRAMMING

The article [47] thoroughly explores the potential use of the memristor modeled as in (1)-(3) as an analogue memory which has *multiple resistance states* in between HRS and LRS. Intermediate values of the resistance can be programmed using a dc sweep and a 1T1R structure. In this case, the continuous SET is obtained with the application of a fixed positive voltage over the threshold and

a consecutive increase of the compliance. A continuous reset can be instead achieved with a consecutive increase of the magnitude of the reset stop voltage without using a negative compliance. Continuous programming can be also obtained via the application of short positive (or negative) pulses with duration of some tens of nanoseconds. In that case, due to the low energies of the pulses, the compliance is not necessarily needed for memristor protection.

C. MEMRISTOR AS A PROGRAMMABLE NONLINEAR RESISTOR

The existence of a voltage threshold and the possibility to set intermediate values of resistances allow to use a memristor as a *programmable nonlinear resistor* in a given range of the electric quantities involved. We discuss this possibility with the next experiment.

Example 1: Consider a memristor obeying model (1)-(3) and having the same parameters as in Table 1 and Table 2. Recall that $g \in [g_{min}, g_{max}]$, where $g_{min} = 0.1 \times 10^{-9}$ m and $g_{max} = 1.7 \times 10^{-9}$ m. Let $g_{min} < g_a = 0.8 \times 10^{-9} < g_b = 1.2 \times 10^{-9} < g_{max}$ and choose three different initial gaps at $t = 0$, namely, $g_1 = g_a$, $g_2 = 1.0 \times 10^{-9}$ nm and $g_3 = g_b$, and apply in each case a triangular voltage waveform with zero mean, rate 20 V/s and peak voltage equal to 1 V, which is below the threshold voltage. Figures 2(a), (b), respectively, report the gap g and the relative variations of the gap $\Delta g = 100 \times (g(t) - g_i)/g_i$ %, $i = 1, 2, 3$, as a function of time obtained via simulation of (1)-(3). It is seen that in each case the gap remains almost constant in the time interval $[0, 3]$ s. The maximum relative error, which occurs for g_1, is lower than 0.2 %. Figure 2(c) depicts the corresponding $v - i$ curves obtained in the simulations. Since the gap is almost constant, as expected, the memristor behaves with very good approximation as a static nonlinear resistor with voltage-current characteristic

$$i = \hat{i}_j(v; g_j) \doteq I_0 \exp\left(-\frac{g_j}{g_0}\right) \sinh\left(\frac{v}{V_0}\right), \quad j = 1, 2, 3.$$
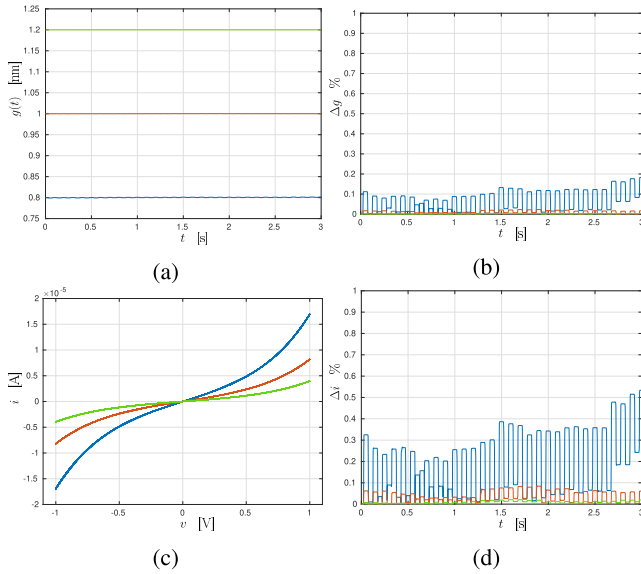
(4)

(a)

(b)

(c)

(d)

FIGURE 2. (a) Gap as a function of time when a zero-mean triangular waveform with peak voltage 1 V and rate 20 V/s is applied; (b) relative error in the gap; (c) curves in the $v - i$ plane and (d) relative error in the memristor current. Green: case $g = 1.2$ nm; red: case $g = 1$ nm and blue: case $g = 0.8$ nm.

(a)

(b)

FIGURE 3. (a) Curves in the $v - i$ plane and (b) relative error in the gap when a zero-mean triangular waveform with peak voltage 1.1 V and rate 22 V/s is applied. Green: case $g = 1.2$ nm; red: case $g = 1$ nm and blue: case $g = 0.8$ nm.

(a)

(b)

FIGURE 4. (a) Curves in the $v - i$ plane and (b) relative error in the gap when a zero-mean triangular waveform with peak voltage 1 V and rate 1 V/s is applied. Green: case $g = 1.2$ nm; red: case $g = 1$ nm and blue: case $g = 0.8$ nm.

To further confirm these results, in Fig. 2(d) we report the relative error in the memristor current $\Delta i = 100 \times (i(t) - \hat{i}_j(v(t); g_j))/\hat{i}_j(v(t); g_j)$ %, $j = 1, 2, 3$. Note that the maximum error, occurring for g_1, is lower than 0.55 %.

Similar results are obtained if we repeat the experiment for any other value of the initial gap in the interval $[g_1, g_3]$ and for any voltage sweep with a larger rate and/or a peak voltage less than or equal to 1 V (the simulations are not reported here for the sake of brevity).

These properties may no longer hold if we apply a waveform with a larger peak voltage approaching the threshold. As an example, Figs. 3(a), (b), report the results of an experiment analogous to that in Fig. 2(b), (c), respectively, the only difference being that a larger peak voltage of 1.1 V is now applied and the rate is 22 V/s. In this case, we have a more pronounced variation of the gap g_1, that in turn implies that in the $v - i$ plane we no longer see a single-valued curve but rather a multiple-valued hysteretic curve. An analogous situation is observed if we consider extremely low rates, see as an example Figs. 4(a), (b) in the case where the peak voltage is 1 V and the rate is 1 V/s. ∎

Remarks:

1) In the paper we will use the memristor within an analogue circuit, namely, a modified memristor Chua's circuit (SMCC), with the goal to obtain oscillations and complex dynamics. In particular, we will choose suitable initial gaps, and we will guarantee that SMCC operates in a range of voltages below threshold such that, for the frequencies of the analogue transient, and in the considered time intervals, the memristor behaves with a good approximation as a programmable nonlinear resistor.
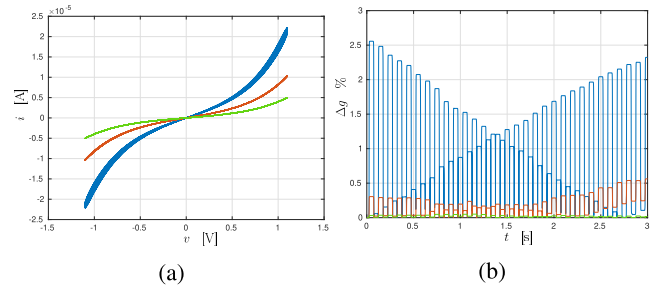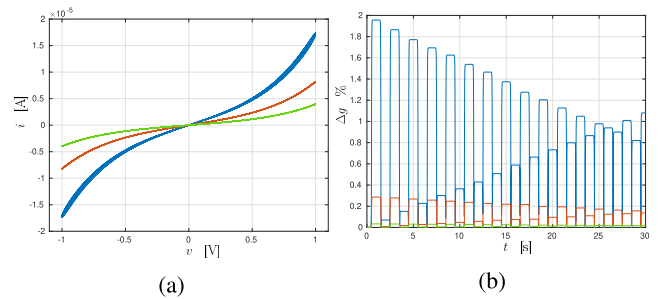
2) We have seen in the simulations that in the voltage range $[-1, 1]$ V the variations of g are negligible. Yet, in the same range the memristor characteristics (4) deviate significantly from linear functions. This is an important aspect, since in the SMCC the memristor is the only nonlinear element that we will use for generating oscillations.

3) We have performed simulations of memristor behavior when considering variations of parameters with respect to those in Table 2. In particular, we considered $\pm 10\%$ variations of γ_0 (cf. [43, Sect. IIb]), a parameter that mainly influences the value of memristor threshold [45], while the other parameters are kept fixed. By repeating an experiment as in Fig. 2, we found that there are not appreciable changes in the $v - i$ curves for the initial gaps $\{0.8, 1, 1.2\}$ nm due to the varied γ_0. We will further investigate on the aspects related to parameter variations in subsequent work.

III. MEMRISTOR CHUA CIRCUIT

Let us consider the circuit in Fig. 5, which is obtained by replacing the active nonlinearity in Chua's circuit (Chua's diode) [44] with a memristor M in parallel to a negative linear conductance $-G_a < 0$. We suppose the memristor is passive and obeys Stanford model (1)-(3). As usual, the negative conductance may be implemented using a negative impedance converter (NIC) [48, p. 192].
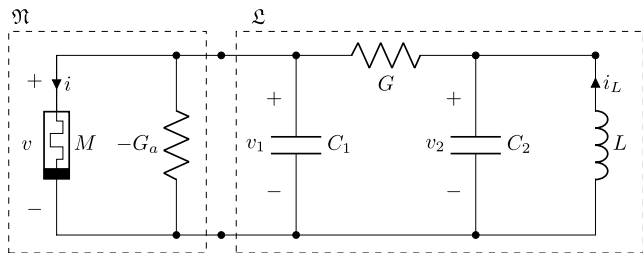
FIGURE 5. Memristor Chua's circuit given by the connection of a two-terminal linear element $\mathfrak{L}$ and a nonlinear element $\mathfrak{N}$ with a memristor and a linear conductance.

It can be readily verified that the Stanford memristor Chua circuit (SMCC) satisfies the fifth-order system of differential equations in the state variables v_1, v_2, i_L, g and T

$$C_1 \frac{dv_1}{dt} = G_a v_1 - G(v_1 - v_2) - I_0 \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{v_1}{V_0}\right)$$

$$C_2 \frac{dv_2}{dt} = -G(v_2 - v_1) + i_L$$

$$L \frac{di_L}{dt} = -v_2$$

$$\frac{dg}{dt} = -v_0 \left[\exp\left(-\frac{qE_{ag}}{kT}\right) \exp\left(\frac{qa_0\gamma}{\ell kT}v_1\right) \right.$$
$$\left. - \exp\left(-\frac{qE_{ar}}{kT}\right) \exp\left(-\frac{qa_0\gamma}{\ell kT}v_1\right) \right]$$

$$\frac{dT}{dt} = \frac{v_1 I_0}{C_{th}} \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{v_1}{V_0}\right) - \frac{T - T_0}{\tau_{th}} \quad (5)$$

where $\gamma = \gamma_0 - \beta(\frac{g}{g_\beta})^3$ and $g \in [g_{min}, g_{max}]$.

The remaining part of the paper is devoted to study the dynamics and bifurcations of (5). To this end we find it convenient to preliminarily analyze a reduced-order system associated with (5). More precisely, in Section IV we assume that g is constant during the transient and the memristor behaves as a programmable nonlinear resistor. In such a case SMCC satisfies a reduced third-order system in the state variables v_1, v_2 and i_L. We show in the same section that we can design the reduced-order system in a way that there is a wide range of gaps g such that, on the attractors, which are studied in detail in Section V, the voltage on the memristor stays below the memristor threshold. Then, according to the discussion in Sect. II-C, we expect that g is almost constant also on the attractors of the fifth-order system (5). In Section VI, we verify that there is indeed a wide range of initial gaps for which the reduced-order model and (5) display a similar dynamic behavior for the state variables v_1, v_2 and i_L.

IV. REDUCED-ORDER MODEL
Let us choose $g \in [g_a, g_b]$, where $g_{min} < g_a < g_b < g_{max}$. We assume in this section that the gap g is constant, hence the memristor behaves as a nonlinear resistor

$$i = \hat{i}(v; g) \doteq I_0 \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{v}{V_0}\right). \quad (6)$$

Under this assumption, SMCC satisfies the third-order system of differential equations in the state variables v_1, v_2 and i_L

$$C_1 \frac{dv_1}{dt} = G_a v_1 - G(v_1 - v_2) - I_0 \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{v_1}{V_0}\right)$$

$$C_2 \frac{dv_2}{dt} = -G(v_2 - v_1) + i_L$$

$$L \frac{di_L}{dt} = -v_2. \quad (7)$$

This is analogous to Chua's circuit, the main difference being that in (7) there is a hyperbolic sine nonlinearity (6), while in Chua's circuit we have a piecewise linear [44] or a cubic nonlinearity [49]. Moreover, nonlinearity (6) depends on the value g of the programmable gap distance. In Section V we will study the bifurcations of (7) obtained by varying g and hence the memristor nonlinearity. Again, this is different from Chua's circuit where bifurcations are obtained by varying the linear conductance G.

The equilibrium points (EPs) of (7) are obtained by letting $dv_1/dt = 0$, $dv_2/dt = 0$ and $di_L/dt = 0$. These yield the set of three static relations $v_2 = 0$, $i_L = -Gv_1$ and

$$(G_a - G)v_1 = I_0 \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{v_1}{V_0}\right). \quad (8)$$

The origin $(v_1, v_2, i_L) = (0, 0, 0)$ is always an EP. Moreover, it can be easily checked that there are two additional EPs $P^+ \neq 0$ and $P^- = -P^+$, symmetric with respect to the origin, when the following condition is satisfied

$$G_a > G + \frac{I_0}{V_0} \exp\left(-\frac{g}{g_0}\right). \quad (9)$$

If (9) is not met, then the origin is the only EP of (7).

Under the assumption of a constant g, SMCC is the interconnection of a linear two-terminal element $\mathfrak{L}$ containing C_1, C_2, L and G and a static nonlinearity $\mathfrak{N}$ given by the parallel of the passive memristor nonlinearity (6) and the negative linear conductance $-G_a$ (Fig. 5). In the following, we first select suitable circuit values for $\mathfrak{L}$. Then, we address the design of $\mathfrak{N}$. Note that once the memristor parameters in Table 2 are considered, and the gap g is constant, the memristor has a fixed nonlinearity (6). Thus, the design of $\mathfrak{N}$ only amounts to select a suitable value for G_a.

A. LINEAR TWO-TERMINAL ELEMENT $\mathfrak{L}$
Henceforth, we refer to a typical set of circuit parameters for $\mathfrak{L}$ as in Chua's circuit introduced in [50]. Namely, we choose $\mathcal{C}_1 = 4.7$ nF, $\mathcal{C}_2 = 47$ nF, $\mathcal{L} = 18$ mH and $\mathcal{R} = 1600$ Ohm. We then use an impedance scaling technique and let $C = \mathcal{C}/\eta$, $L = \mathcal{L}\eta$, $G = 1/R = 1/(\mathcal{R}\eta)$, where $\eta > 0$ is a suitable parameter to be chosen at a later point (cf. Sect. IV-C).

B. NONLINEARITY $\mathfrak{N}$
In order to select a value for G_a, we find it convenient to first choose a gap quantity, denoted by $\tilde{g}$, which is in a one-to-one correspondence with G_a. Starting with the choice of $\tilde{g}$ is

advantageous since we know *a priori* the gap interval where $\tilde{g}$ should belong.

To proceed, fix a gap $\tilde{g} \in (g_a, g_b)$. The value of G_a is chosen in a way that when $g = \tilde{g}$ the Jacobian $J(0; \tilde{g})$ of the vector field defining (7) at the EP in the origin has a null trace. We have

$$J(0; \tilde{g})$$
$$= \begin{pmatrix} \frac{1}{C_1}\left(G_a - G - \frac{I_0}{V_0}\exp\left(-\frac{\tilde{g}}{g_0}\right)\right) & \frac{G}{C_1} & 0 \\ \frac{G}{C_2} & -\frac{G}{C_2} & \frac{1}{C_2} \\ 0 & -\frac{1}{L} & 0 \end{pmatrix}$$

and

$$tr(J(0; \tilde{g})) = \frac{1}{C_1}\left(G_a - G - \frac{I_0}{V_0}\exp\left(-\frac{\tilde{g}}{g_0}\right)\right) - \frac{G}{C_2}.$$

Hence, $tr(J(0; \tilde{g})) = 0$ yields the condition

$$G_a = \frac{I_0}{V_0}\exp\left(-\frac{\tilde{g}}{g_0}\right) + \left(1 + \frac{C_1}{C_2}\right)G. \qquad (10)$$

Clearly, the EP at the origin is unstable when $g = \tilde{g}$. Moreover, since (10) implies (9), it turns out that SMCC has three EPs. Indeed, by substituting in (9) the expression of G_a in (10), it follows that (7) has three EPs for all g such that

$$g > \hat{g} \doteq g_0 \ln \frac{1}{\exp\left(-\frac{\tilde{g}}{g_0}\right) + \frac{V_0}{I_0}\frac{C_1}{C_2}G}. \qquad (11)$$

Moreover, it can be shown that for all g satisfying (11) the EP at the origin has a unique unstable eigenvalue (see Appendix). This implies that for each fixed gap $\tilde{g} \in (g_a, g_b)$, and hence for the value of G_a given by (10), there exists a range of g defined by condition (11) where SMCC possesses three EPs and the EP at the origin has a unique unstable eigenvalue. It is worth to remark that this scenario is quite similar to that displayed by the double-scroll family [44].

C. IMPEDANCE SCALING
To guarantee that v_1 does not exceed the memristor threshold during the transient we need that (7) has attractors with amplitude smaller than the memristor threshold. In general, it is difficult to precisely estimate such an amplitude for a chaotic circuit. In the paper we rely on an approximate yet effective technique where the attractors amplitude is kept small by reducing the magnitude of coordinates $\pm\bar{v}_1$ of EPs P^+ and P^-.

First of all, we find an approximate expression for the EPs. Suppose to replace the hyperbolic sine $\sinh(v_1/V_0)$ with its third-order Taylor expansion $v_1/V_0 + v_1^3/(6V_0^3)$. Then, when (9) holds, (8) has two non-zero solutions $\pm\bar{v}_1$ where

$$\bar{v}_1 = \sqrt{6G\frac{C_1}{C_2}\frac{V_0^3}{I_0}\exp\left(\frac{g}{g_0}\right)} = \sqrt{6\frac{G}{\eta}\frac{C_1}{C_2}\frac{V_0^3}{I_0}\exp\left(\frac{g}{g_0}\right)}.$$

Then, $|\bar{v}_1|$ decreases when g decreases or if we increase the scaling factor η. Another possibility is to increase the ratio C_2/C_1.

It is worth to remark that parameters $\alpha = C_2/C_1$ and $\beta = R^2/(C_2 L)$, used when writing Chua's circuit equations in adimensional form [50], are not affected by the impedance scaling.

Example 2: Let $g_a = 0.8$ nm, $g_b = 1.2$ nm and fix $\tilde{g} = 1$ nm. From (10) we have $G_a = 3.8137 \times 10^{-5}$ Ohm^{-1}. The EP of (7) for $g = \tilde{g}$ and $\eta = 5$ nm are $\{0, P^+ = (1.45, 0, -0.00018), -P^+\}$. Note that $\bar{v}_1 = 1.45$ is quite close to the memristor threshold. If instead we choose a higher value $\eta = 20$, the EPs for $g = \tilde{g}$ are $\{0, P^+ = (0.87, 0, -0.000027)), -P^+\}$. Now $\bar{v}_1 = 0.87$ is quite below the memristor threshold. ∎

Example 3: Consider once more the case $\tilde{g} = 1$ nm and $\eta = 20$. Table 3 reports the number of asymptotically stable and unstable EPs of (7) and the eigenvalues of the Jacobian at the EPs for some values of the gap $g \in [0.8, 1.2]$ nm. From (11) we have $\hat{g} = 0.83$ nm, hence (7) has three EPs when $g > 0.83$ nm and only one EP when $g \leq 0.83$ nm. We remark that when $g = 1$ nm and $g = 0.925$ nm there are three unstable EPs $\{0, P^+, P^-\}$ and their structure is analogous to that of Chua's circuit [51, Sect. II]. Namely, $J(0; 0.925)$ has a real positive eigenvalue and two complex conjugate eigenvalues with negative real part, while $J(P^+; 0.925)$ and $J(P^-; 0.925)$ have a real eigenvalue and two complex conjugate eigenvalues with positive real part. Instead, when $g = 0.85$ nm there three EPs but two of them are asymptotically stable. When $g = 0.8$ nm the origin is the only asymptotically stable EP. ∎

V. REDUCED-ORDER MODEL: COMPLEX DYNAMICS AND BIFURCATIONS
In this section we report on numerical simulations using MATLAB of SMCC assuming g is constant during the transient, hence SMCC satisfies the reduced third-order system (7).

We refer to the memristor parameters in Table 2 and circuit parameters as in Section III. Let $g_a = 0.8$ nm and $g_b = 1.2$ nm. In the first set of simulations we have chosen $\tilde{g} = 1$ nm, so that from (10) we obtain $G_a = 3.8137 \times 10^{-5}$ Ohm^{-1}. Moreover, for the impedance scaling we let $\eta = 20$.

Figure 6 reports the bifurcation diagram of (7) using g as a parameter that is varied in $[0.8, 1.2]$ nm. The vertical axis shows the voltage v_1 on the memristor. Note that for $g \geq 0.92$ nm (7) displays either complex dynamics or periodic windows. Especially, we can observe quite a wide periodic window with a period-5 cycle for $g \in [0.951, 0.962]$ nm. When g is decreased below 0.92 nm there is a sequence of inverse period-doubling bifurcations causing the death of the complex attractor. In particular, we find that there in an inverse period-doubling bifurcation at $g = 0.905$ nm, an inverse Hopf bifurcation at $g = 0.864$ nm and an

TABLE 3. Number of asymptotically stable and unstable EPs of (7) and eigenvalues of the Jacobian at the EPs for various values of g. We have $\tilde{g} = 1$ nm and $\eta = 20$.

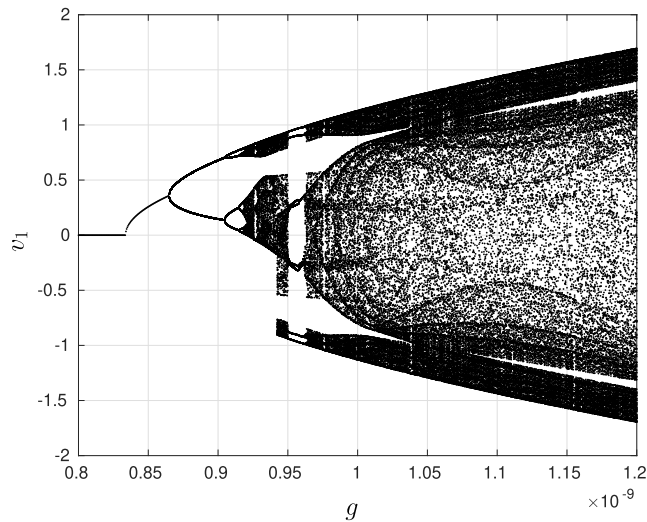| g [nm]	Asymptotically stable EPs	Unstable EPs	Eigenvalues of Jacobian [rad/sec]
1	–	$\{0, P^+ = (1.45, 0, -0.000027)), P^-\}$	$J(0; g): \{26459, -13229 \pm j32909\}$ $J(P^+; g), J(P^-; g): \{-61132, 3310 \pm j40946\}$
0.925	–	$\{0, P^+ = (0.63, 0, -0.000019)), P^-\}$	$J(0): \{19095, -12057 \pm j30656\}$ $J(P^+; g), J(P^-; g): \{-37805, 3097 \pm j34683\}$
0.85	$\{P^+ = (0.27, 0, -0.0000083)), P^-\}$	$\{0\}$	$J(0): \{5263, -8438 \pm j27019\}$ $J(P^+; g), J(P^-; g): \{-12982, -2056 \pm j26975\}$
0.8	$\{0\}$	–	$J(0; g): \{-13063, -2029 \pm j26991\}$

FIGURE 6. Bifurcation diagram of (7) for $\tilde{g} = 1$ nm and $\eta = 20$.

inverse Pitchfork bifurcation at $g = \hat{g} = 0.83$ nm (cf. Example 3) [52]. It is worth to observe that, in accordance with the considerations in Section IV-C, higher values of g correspond to higher values of the positive peak of voltage v_1 on the attractors.

Figure 7 shows the projection onto the $v_1 - v_2$ plane of the attractors of (7) for specific values of the bifurcation parameter g. It is seen that for $g = 1$ nm (7) displays a double-scroll attractor that is remarkably similar to that displayed by Chua's circuit with a piecewise nonlinearity [50]. This behavior is consistent with the fact that for $g = 1$ nm (7) has a structure of EPs similar to that of Chua's circuit (cf. Example 3). The peak positive amplitude on the double-scroll attractor is $v_1 = 1.1$ V, which is below the memristor threshold of about 1.5 V observed in Section II. From simulations we observe a double-scroll attractor also when $g = 1.04$ nm and $g = 1.18$ nm. In particular, we note once more that the positive peak amplitude v_1 increases when g increases. For instance, when $g = 1.04$ nm the peak amplitude is about 1.26 V and it approaches the threshold, while when $g = 1.18$ nm the peak amplitude is about 1.9 V and is beyond the memristor threshold. Finally, when $g = 0.85$ nm we have convergence to a stable EP at $P^+ = (0.76, 0, 0.0000083)$ (simulation not shown in the figure). See also Example 3.
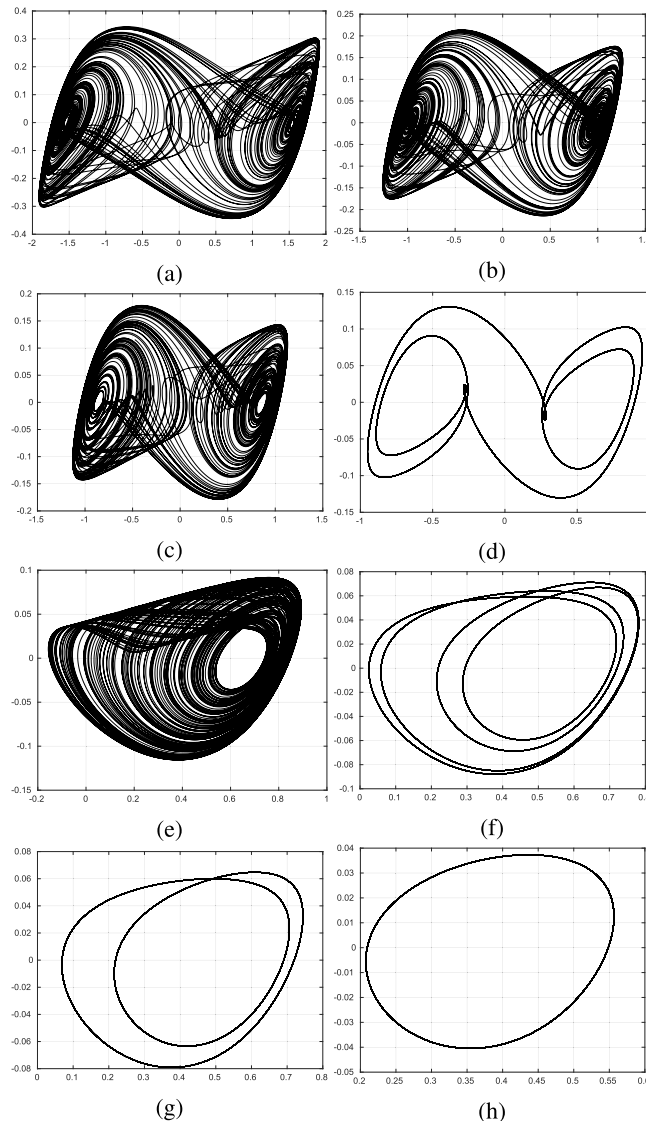

FIGURE 7. Attractors of (7) (projection onto the $v_1 - v_2$ plane) for specific values of the bifurcation parameter g. Horizontal axis: v_1 [V]; vertical axis: v_2 [V]. We have $\tilde{g} = 1$ nm and $\eta = 20$. (a), (b), (c) Double-scroll attractor for $g = 1.18$ nm, $g = 1.04$ nm and $g = 1$ nm, respectively; (d) period-5 cycle ($g = 0.953$ nm); (e) single-scroll attractor ($g = 0.94$ nm); (f) period-4 cycle ($g = 0.917$ nm); (g) period-2 cycle ($g = 0.91$ nm); (h) limit cycle ($g = 0.88$ nm).

We have done simulations analogous to those presented before also for $\tilde{g} \in \{1.1, 1.05, 1., 0.95, 0.9\}$. These simulations, not reported here, have led to a scenario quite similar
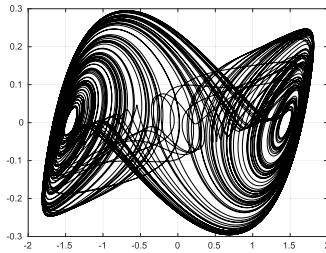
FIGURE 8. Attractor of (7) (projection onto the $v_1 - v_2$ plane) when $g = \tilde{g} = 1$ nm and $\eta = 5$. Horizontal axis: v_1 [V]; vertical axis: v_2 [V].
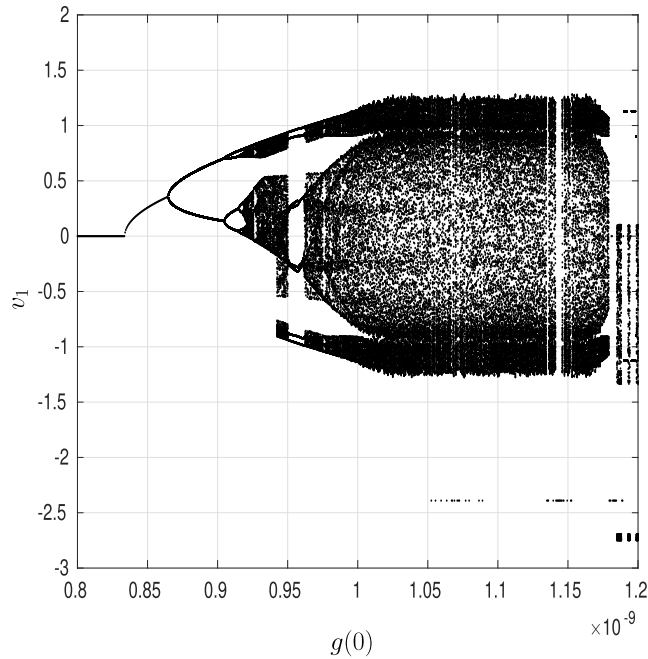

FIGURE 9. Bifurcation diagram of (5) for $\tilde{g} = 1$ nm and $\eta = 20$.

to that in Figs. 6, 7. On the contrary, by changing η we obtain significant variations in the amplitude of attractors. As an example, Fig. 8 depicts the double-scroll attractor for $\eta = 5$ and $g = \tilde{g} = 1$ nm. The maximum amplitude is about 1.8 V and exceeds the memristor threshold. We recall that in the case $\eta = 20$ and $g = \tilde{g} = 1$ nm such an amplitude was about 1.1 V.

VI. COMPLETE MODEL: COMPLEX DYNAMICS AND BIFURCATIONS

In this section we consider for SMCC the complete fifth-order model (5). Our goal is to verify via simulations that there is quite a wide range of initial conditions $g(0)$ for the gap such that we have $g(t) \simeq g(0)$ during the transient evolution of (5). In turn, due to such negligible variations of g, the dynamic behavior of (5) is almost coincident with that of the reduced-order system (7) as long as the state variables v_1, v_2 and i_L are concerned.

Let $\tilde{g} = 1$ nm and $\eta = 20$ and also assume the memristor and circuit parameters are as in Section V. Figure 9 reports the bifurcation diagram of (5) with respect to parameter $g(0)$ varying in [0.8, 1.2] nm. Such diagram is seen to be
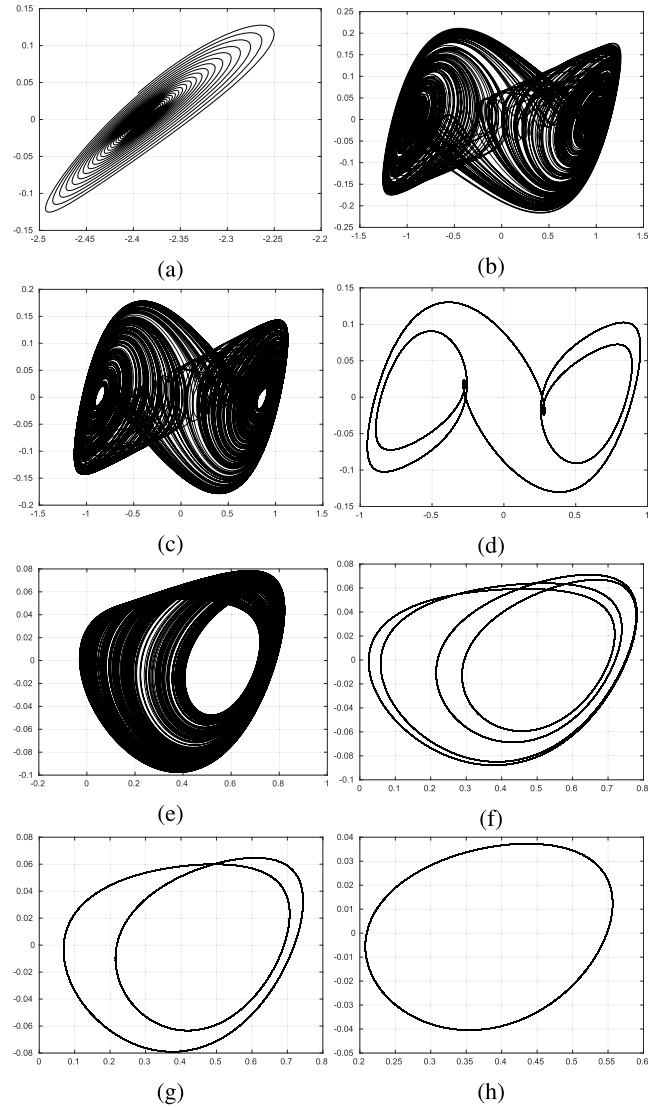

FIGURE 10. Attractors of (5) (projection onto the $v_1 - v_2$ plane) for specific values of the bifurcation parameter $g(0)$. Horizontal axis: v_1 [V]; vertical axis: v_2 [V]. We have $\tilde{g} = 1$ nm and $\eta = 20$. (a) Asymptotically stable EP with ($g(0) = 1.18$); a trajectory converging toward the EP is also shown; (b), (c) double-scroll attractor for $g(0) = 1.04$ nm and $g(0) = 1$ nm, respectively; (d) period-5 cycle ($g(0) = 0.953$ nm); (e) single-scroll attractor ($g(0) = 0.925$ nm); (f) period-4 cycle ($g(0) = 0.917$ nm); (g) period-2 cycle ($g(0) = 0.91$ nm); (h) limit cycle ($g(0) = 0.88$ nm).

qualitatively similar to that of the reduced-system (7), given in Fig. 6, except for large values of $g(0)$, namely $g(0) > 1.05$ nm. In particular, it is worth to stress that for $g \in [0.8, 0.92]$ nm system (5) closely reproduces the sequence of period-doubling, Hopf and Pitchfork bifurcations displayed by (7). When $g(0) > 1.05$ nm, the behavior of (5) is quite different from that of (7). In fact, there are values of $g(0)$ such that (5) displays complex attractors with reduced amplitude with respect to those of (7) for $g = g(0)$. Moreover, there are values of $g(0)$ such that (5) is convergent to some stable EP while, for $g = g(0)$, (7) is not convergent.

These differences are further discussed with the aid of Fig. 10, that depicts the attractors of (5) (projections onto
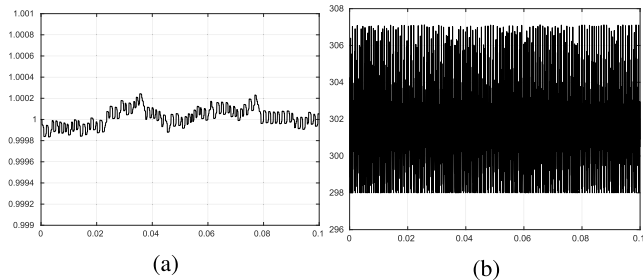
FIGURE 11. (a) Time-domain behavior of the gap. Horizontal axis: time t [s]; vertical axis: $g(t)$ [nm]. (b) Behavior of temperature. Horizontal axis: time t [s]; vertical axis: $T(t)$ [K]. Case $g(0) = 1$ nm.

FIGURE 13. (a) Time-domain behavior of the gap. Horizontal axis: time t [s]; vertical axis: $g(t)$ [nm]. (b) Behavior of temperature. Horizontal axis: time t [s]; vertical axis: $T(t)$ [K]. Case $g(0) = 1.04$ nm.

FIGURE 12. (a) Time-domain behavior of the gap. Horizontal axis: time t [s]; vertical axis: $g(t)$ [nm]. (b) Behavior of temperature. Horizontal axis: time t [s]; vertical axis: $T(t)$ [K]. Case $g(0) = 0.925$ nm.
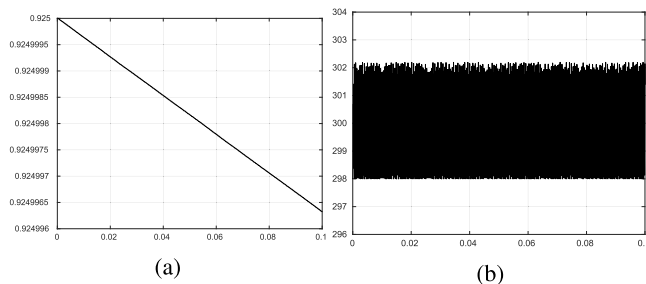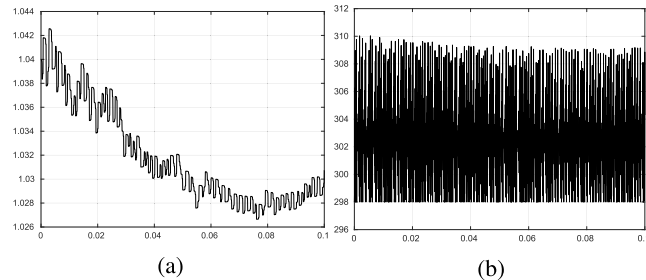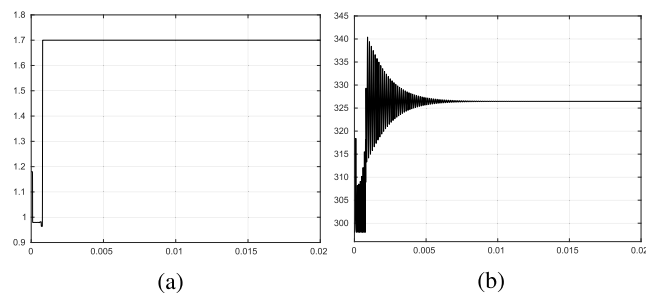

FIGURE 14. (a) Time-domain behavior of the gap. Horizontal axis: time t [s]; vertical axis: $g(t)$ [nm]. (b) Behavior of temperature. Horizontal axis: time t [s]; vertical axis: $T(t)$ [K]. Case $g(0) = 1.18$ nm.

the $v_1 - v_2$-plane) for some specific values of $g(0)$. When $g(0) = 1$ nm we observe for (5) a double-scroll attractor very similar to that of (7). We can easily justify this behavior by noting that the amplitude v_1 stays quite below the memristor threshold. As depicted in Fig. 11, g has almost negligible random variations around $g(0)$ during the transient. In the same figure we also report for completeness the behavior of T, that undergoes as expected only small variations above the ambient temperature.

In the case $g(0) = 0.925$ nm, we again observe for (5) a single scroll attractor similar to that of (7). Actually, also in this case v_1 stays below the memristor threshold during the transient. One difference is that now v_1 oscillates around the value 0.63 of the second coordinate of the EP P^+ (cf. Table 3) and then it has non-zero mean. As a consequence, g shows a small unidirectional drift (Fig. 12). Variations of g are however extremely small and g remains almost constant in a practical time interval up to 1 s. The behavior of (5) in the cases $g(0) \in \{0.925, 0.918, 0.917, 0.91, 0.88\}$ can be explained in a similar way.

Consider the case $g(0) = 1.04$ nm. The behaviors of g and T are reported in Fig. 13. Now, v_1 approaches the memristor threshold during the initial part of the transient and g has some significant variations. However, the double-scroll attractor is quite robust and is again similar to that displayed by (7) when $g = 1.04$ nm.

Finally, consider the case $g(0) = 1.18$ nm. The behaviors of g and T are depicted in Fig. 14. Now, v_1 exceeds the memristor threshold during the transient. Note that g displays
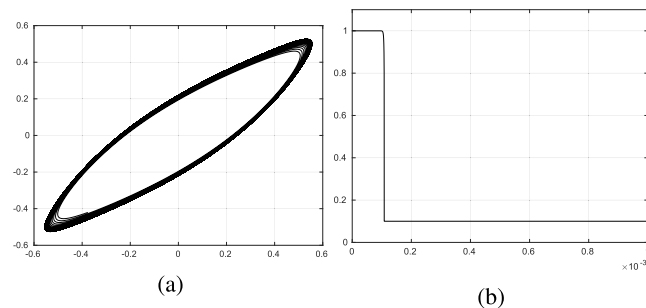

FIGURE 15. (a) Trajectory of (5) (projection onto the $v_1 - v_2$ plane) converging to a cycle when $g(0) = \tilde{g} = 1$ nm and $\eta = 5$. Horizontal axis: v_1 [V]; vertical axis: v_2 [V]. (b) Time-domain behavior of the gap. Horizontal axis: time t [s]; vertical axis: gap $g(t)$ [nm].

rapid and big variations and eventually achieves the limiting value $g = g_{\max} = 1.7$ nm (cf. Section II). Meanwhile, after an oscillatory transient, T reaches a steady-state value of 326 K. Once g has reached $g_{\max}$, we observe convergence of the trajectory to the EP P^- with $v_1 = -2.39$ V, a behavior that is drastically different from (7), that instead displays a double-scroll attractor when $g = 1.18$ nm.

We simulated the behavior of (5) for several other values of $\tilde{g}$, $g(0)$ and η. As an example, Fig. 15(a) depicts the time-domain behavior of (5) when $g(0) = \tilde{g} = 1$ nm and $\eta = 5$. Note that we have convergence to a limit cycle, which is different from the double-scroll attractor displayed by (7) for the same values of $g = g(0)$, $\tilde{g}$ and η (Fig. 8). Figure 15(b) depicts the corresponding behavior of the gap. This different

behavior can be explained with analogous considerations as in the case $\tilde{g} = 1$ nm, $g(0) = 1.2$ nm and $\eta = 20$.

VII. DISCUSSION AND CONCLUSION

The paper has studied the nonlinear dynamics and bifurcations in a class of Chua's circuits with a real non-volatile memristor obeying Stanford model. The key feature is that the memristor is used as a programmable nonlinear resistor. Namely, the memristor Chua's circuit (SMCC) is designed in order that during the transient oscillations the memristor voltage stays below threshold, its main state variable (i.e., the gap g) is almost constant, and the memristor behaves as a static nonlinear resistor. We stress that the memristor nonlinearity is the only one used in SMCC to generate oscillations and complex dynamics. This is possible since there is a voltage range below memristor threshold where the memristor characteristic deviates significantly from a linear function while dg/dt turns out to be negligible. On the other hand, g and the nonlinear memristor characteristic can be varied during the programming phase, using for instance voltage pulses above threshold, thus causing bifurcation phenomena.

The approach in the paper differs from previous ones on oscillators with real non-volatile memristors where the oscillations are due to wide changes that the memristor state variable undergoes along the hysteresis loops, while bifurcations are generated via variations in the circuit parameters. It is also remarked that using a memristor as a programmable nonlinear element is different from its use as a synapse [53], [54], since in the latter case the nonlinearity of the memristor is an undesirable feature. We refer the reader to [54, Sect. V-A] where a bridge configuration is employed to compensate for memristor nonlinearities in the implementation of programmable synapses. Analogous considerations hold if we compare the approach in this paper with that in [55], where again the memristor is used as a programmable linear conductance in some analogue circuits applications.

In the paper we have been mainly interested in cases where the behavior of SMCC is analogous to that of a reduced third-order system obtained by assuming g is constant during the transient. Instead, if we allow the memristor voltage to reach or exceed the memristor threshold, then g can undergo to large changes. In such cases we have observed a very rich dynamic scenario for the fifth-order system describing SMCC. We believe this is an interesting aspect to be further explored in future research of SMCC.

Nowadays, real memristor devices obeying Stanford model, as those considered in [43], begin to be commercially available, as for instance at foundries Taiwan Semiconductor Manufacturing Company Limited (TSMC) or United Microelectronics Corp (UMC). The ultimate goal of this research shall be to verify the phenomena observed through simulations via the implementation of actual circuit prototypes of SMCC when real devices will be at our disposal.

APPENDIX

We want to show that for all g satisfying (11) the EP at the origin of (7) has a unique unstable eigenvalue. First, we recall that g satisfies (11) if and only (9) holds and, hence, if and only if we have

$$1 - \frac{G_a}{G} + \frac{I_0}{GV_0} \exp\left(-\frac{g}{g_0}\right) < 0$$

where G_a is given by (10). Now, we observe that the Jacobian $J(0; g)$ of the vector field defining (7) at the origin can be written as

$$\begin{pmatrix} -\dfrac{G}{C_1}\rho & \dfrac{G}{C_1} & 0 \\ \dfrac{G}{C_2} & -\dfrac{G}{C_2} & \dfrac{1}{C_2} \\ 0 & -\dfrac{1}{L} & 0 \end{pmatrix} \doteq J_\rho$$

where the scalar quantity ρ is defined as

$$\rho \doteq 1 - \frac{G_a}{G} + \frac{I_0}{GV_0} \exp\left(-\frac{g}{g_0}\right).$$

Hence, we have to show that J_ρ has a unique positive real eigenvalue for all $\rho < 0$. To proceed, we compute the characteristic polynomial of J_ρ obtaining

$$\det(sI - J_\rho) = s^3 + \left(\frac{G}{C_1}\rho + \frac{G}{C_2}\right) s^2$$
$$+ \left(\frac{1}{LC_2} + \frac{G^2}{C_1 C_2}(\rho - 1)\right) s + \frac{G}{LC_1 C_2}\rho$$

where s denotes the complex variable and I_3 is the third-order identity matrix. From the Routh-Hurwitz criterion it follows that J_ρ has a unique positive real eigenvalue if and only if the sequence $\{1, c_1, c_2, c_3\}$ of the leading coefficients of the Routh-Hurwitz table has a unique sign variation [56]. Straightforward computations lead to the following expressions

$$c_1 = \frac{G}{C_1}\rho + \frac{G}{C_2}$$
$$c_2 = \frac{G^2}{C_1 C_2}(\rho - 1) + \frac{1}{c_1}\frac{G}{LC_2^2}$$
$$c_3 = \frac{G}{LC_1 C_2}\rho.$$

Note that c_3 has the same sign of ρ, thus the sequence $\{1, c_1, c_2, c_3\}$ has at least a sign variation for all $\rho < 0$. To prove that there is a unique sign variation in the sequence, it is enough to show that there does not exist any $\rho < 0$ such that $c_1 < 0$ and $c_2 > 0$. This can be readily verified since $c_1 < 0$ implies that $c_2 < 0$. Finally, we observe that the continuity of the roots of the characteristic polynomial with respect to ρ can be used to complete the proof for the isolated negative values of ρ where c_1 and c_2 vanish.

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