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A High-Voltage LDO Voltage Regulator Featuring Enhanced Transient Response and Reduced Area

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Abstract. This paper introduces a high-voltage output-capacitorless voltage regulator designed for fast transient response to supply switching loads digital blocks directly from the high-voltage power rail. The proposed solution based on the current buffer Miller compensation, achieves a load current transient response of about 1.6 ns and reduces silicon area by a factor of 2.25 compared to a high-voltage Flipped Voltage Follower-based topology.

Keywords: Analog ICs, OCL-LDO voltage regulator, FVF, advanced frequency compensation.

1 Introduction

Low dropout (LDOs) voltage regulators are extensively used in the Power Management Integrated Circuits (PMICs) of System-on-Chips (SoCs) to supply the building blocks with a clean, stable and accurate voltage [1].
In a conventional LDO, such as the one shown in Fig. 1a, the slow-loop comprising the Error Amplifier (EA), the output transistor (MP) and the resistive voltage divider provides the regulated output voltage starting from a reference voltage (V_{REF}). An off-chip capacitor ($C_{\mathrm{L-off}}$), in the μF range, is used both to stabilize the voltage regulator and to reduce the output voltage ripple due to fast load current variations. Such a capacitor increases the number of pins and introduces stray inductances (L_{p}) that worsen the load transient response at the point-of-load. Aiming to eliminate the off-chip components, output-capacitorless LDOs (OCL-LDOs) have been developed in the last decades [2].
Referring to the OCL-LDO in Fig. 1b, the on-chip capacitor (C_{L}) is several orders of magnitude smaller than ($C_{\mathrm{L-off}}$). Therefore, its transient performance mainly relies on the capability of the voltage regulator to sense the output voltage variation and quickly adjust the source-gate voltage of the transistor MP[3]. Usually, the unit gain frequency of such voltage regulators is extended using sophisticated compensation networks [5]-[6], which introduce fast-loops featuring larger bandwidth [7], and/or implementing undershoot/overshoot detection circuits that drive the output transistor quickly.
The aforementioned architectures focus on minimizing the load capacitance

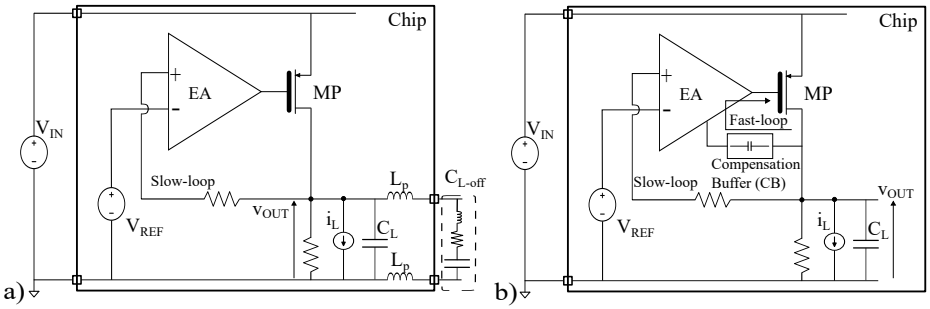


Fig. 1: a) Conventional LDO voltage regulator with off-chip load capacitor and parasitics. b) Output-capacitorless LDO with fast-loop to enhance the transient performance.

while providing fast response time under low power budget. However, to the authors' knowledge, none of the fast transient solutions available in the open literature can handle input-voltage larger than a few Volts. Indeed, a high input-voltage LDO would allow for a further reduction in the number of pins by powering both the low-voltage digital core and the output-power stage of the SoC with the same supply voltage.
Wanting to fill this gap, a high-voltage OCL-LDO voltage regulator that exploits the current buffer Miller compansation (CBMC) approach featuring transient performance comparable to that of low-voltage OCL-LDO regulators and reduced silicon area is proposed.
The paper is organized as follow. Section 2 presents the pros and cons of high-voltage swing OCL-LDOs for the test case of a Flipped Voltage Follower OCL-LDO and analyses the proposed architecture. Simulation results are provided in Section 3 and concluding remarks are drawn in Section 4.

2 Circuit implementation

As highlighted in the introduction, OCL-LDO voltage regulators allow one to save silicon area while preserving excellent transient performance. To achieve this result, OCL-LDOs are typically implemented as multi-loop systems in which a slow-loop ensures the accurate DC regulation, while the fast-loop immediately drives the power device in case of load current variations. Common implementations include the Flipped Voltage Follower(FVF) topology or Advanced Miller compensation-based architectures. In this Section, we first review a reference FVF-based solution, highlighting the critical issues in designing a fast transient high-voltage regulators based on this topology. Then, the proposed current buffer Miller compensated OCL-LDO is presented and compared with the reference one in terms of silicon area reduction.

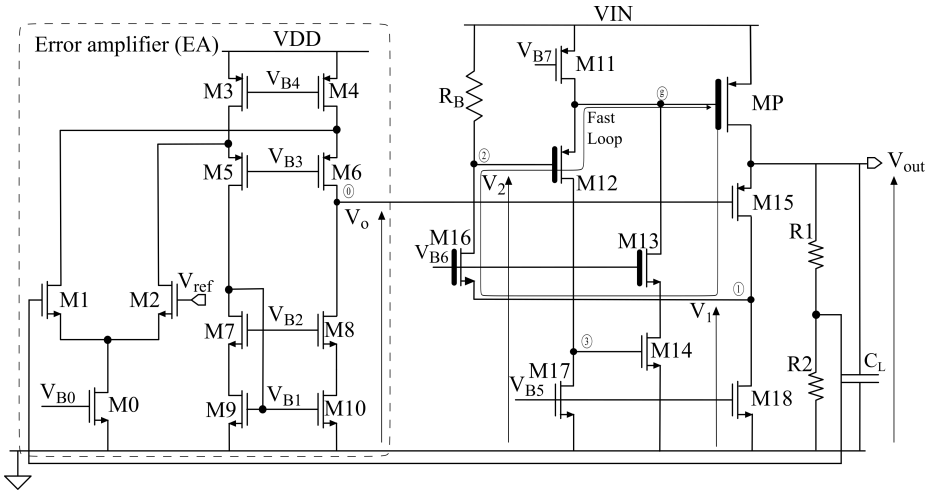


Fig. 2: Schematic of the OCL-LDO based on the cascoded Flipped Voltage Follower topology with Super Source Follower buffer derived by [7]. High-voltage device highlighted with thicker gate line.

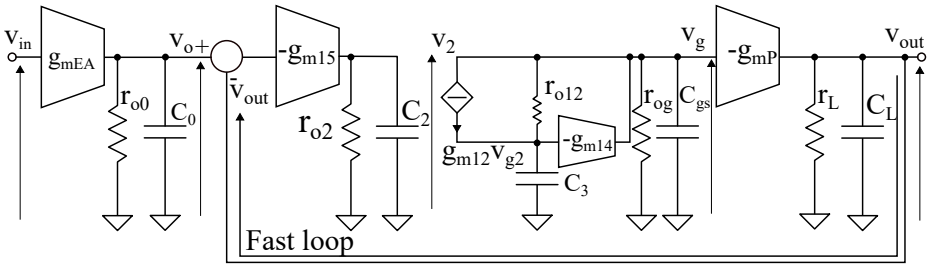


Fig. 3: Small-signal equivalent circuit for the OCL-LDO in Fig. 2.

2.1 High-voltage FVF-based voltage regulator

The FVF is a widely adopted low-voltage architecture for the realization of OCL-LDOs voltage regulators. A high-voltage variant of the topology proposed in [7], shown in Fig. 2, is used as reference architecture for the following analyses. In this solution, the fast-loop consists of: (1) a FVF (M_{15}-M_{16}) with folded cascode stage to sense the output voltage and (2) a Super Source Follower (SSF) buffer (M_{12}-M_{14}) to quickly discharge the input capacitance of the transistor MP. Indeed, since the transient performance of an OCL-LDO relies on the fast-loop bandwidth, the SSF low output impedance allows to move toward high frequencies the non dominant pole associated with MP.
The small-signal model for the circuit of Fig. 2 is shown in Fig. 3. g_{mEA} represents the transconductance of the error amplifier, g_{mP} the transconductance of the power transistor, while r_{oi} and C_{i} are the lumped resistance and capacitance at

the i-th node. The open-loop transfer function of the fast-loop is

$$T = \frac{v_{\text{out}}}{v_{\text{out}} - v_{\text{o}}} \approx \frac{v_2}{v_{\text{out}} - v_{\text{o}}} \frac{v_{\text{g}}}{v_2} \frac{v_{\text{out}}}{v_{\text{g}}}, \tag{1}$$

where equations (2), (3) and (4) are the transfer functions of the cascoded FVF, the SSF and the power transistor.

$$\frac{v_2}{v_{\text{out}} - v_{\text{o}}} \approx \frac{g_{\text{m}_{15}} r_{\text{o}2}}{1 + s r_{\text{o}2} C_2} \approx \frac{g_{\text{m}_{15}} R_{\text{B}}}{1 + s R_{\text{B}} C_2} \tag{2}$$

$$\frac{v_{\text{g}}}{v_2} \approx \frac{1}{s^2 \frac{C_{\text{gs}} C_3}{g_{\text{m}_{12}} g_{\text{m}_{14}}} + s \frac{C_{\text{gs}} + g_{\text{m}_{12}} r_{\text{o}_{12}} C_3}{r_{\text{o}_{12}} g_{\text{m}_{12}} g_{\text{m}_{14}}} + 1} \tag{3}$$

$$\frac{v_{\text{out}}}{v_{\text{g}}} = -\frac{g_{\text{m}_{\text{P}}} r_{\text{L}}}{1 + s r_{\text{L}} C_{\text{L}}} \tag{4}$$

The phase margin is given by

$$\phi_{\text{m}} \approx 90^\circ - tan^{-1} \left(\frac{UGF}{Q \omega_{\text{o}} \left[1 - (UGF/\omega_{\text{o}})^2 \right]} \right) \tag{5}$$

where ω_{o} is the characteristic frequency of the SSF complex poles, Q is their quality factor and UGF represents the loop unity-gain frequency. Wanting to keep a phase margin above 60° one can choose $\omega_{\text{o}} \approx 2UGF$ and $Q \approx \sqrt{2}$. Furthermore, assuming that (1) models a dominant pole system, the load capacitor should be:

$$C_{\text{L}} \geq 2 g_{\text{m}_{\text{P}}} g_{\text{m}_{15}} R_{\text{B}} \sqrt{\frac{C_{\text{gs}} C_3}{g_{\text{m}_{12}} g_{\text{m}_{14}}}}. \tag{6}$$

Equation highlights the tradeoff between area and power consumption in the FVF-based solution, in which the requirement for quiescent current sets a lower bound on R_{B}, thereby limiting the on-chip capacitance reduction.

3 Proposed High-Voltage CBMC voltage regulator

The proposed solution is shown in Fig. 4. It is based on a conventional LDO voltage regulator comprising of an high-voltage output transistor (MP) feeding the load. The output is loaded by the capacitor C_{L}, i.e. the load capacitance or an additional one placed intentionally to make the circuit stable. The slow-frequency regulation loop is composed of the resistive voltage divider (R1, R2) and the error amplifier (EA) which in turn drives the gain stage comprising of the transistors M1-M5. The Compensation buffer (CB), implemented by the transistors M9-M11 and the compensation capacitor C_{m}, sets a low impedance path for the high-frequency components making the voltage regulator stable, thus enhancing its transient performance. Besides the output transistor (MP) only two high-voltage transistors are needed, M4 and M7 respectively. All the others, including the compensation capacitor, are low voltage components, therefore they are much

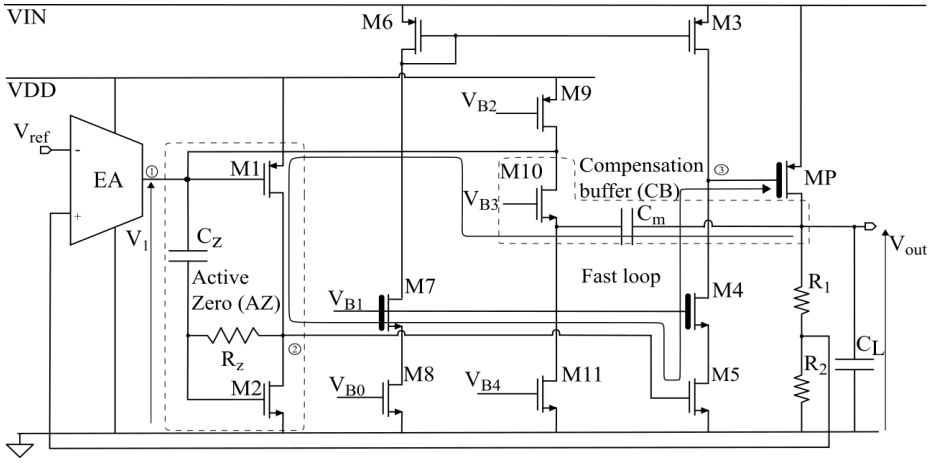


Fig. 4: Schematic view of the CBMC OCL-LDO comprising high-voltage devices.

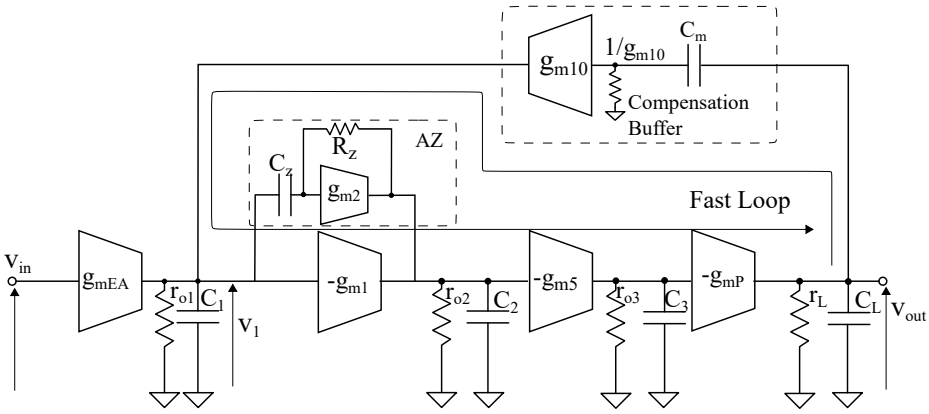


Fig. 5: Small-signal equivalent circuit for the CBMC OCL-LDO.

faster, and they need much less silicon area than their high-voltage counterpart. Furthermore, it should be noted that the EA, a part of the circuit used to drive MP and the compensation circuit are supplied through a low voltage rail (V_{DD}), which takes energy from a pre-regulator (not shown in Fig. 4).

Fig. 5 shows the small-signal equivalent of the circuit in Fig. 4, r_{oi} and C_{i} represent the lumped resistance and the parasitic capacitance at the i-th node. The open loop transfer function of the proposed solution can be written as

$$T = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} \approx A_{\infty} \frac{\left(\frac{C_{\mathrm{m}}/C_1}{1+s(C_{\mathrm{m}}/g_{\mathrm{m10}})}\right) \mathrm{H}}{\left(\frac{C_{\mathrm{m}}/C_1}{1+s(C_{\mathrm{m}}/g_{\mathrm{m10}})}\right) \mathrm{H} + 1}, \tag{7}$$

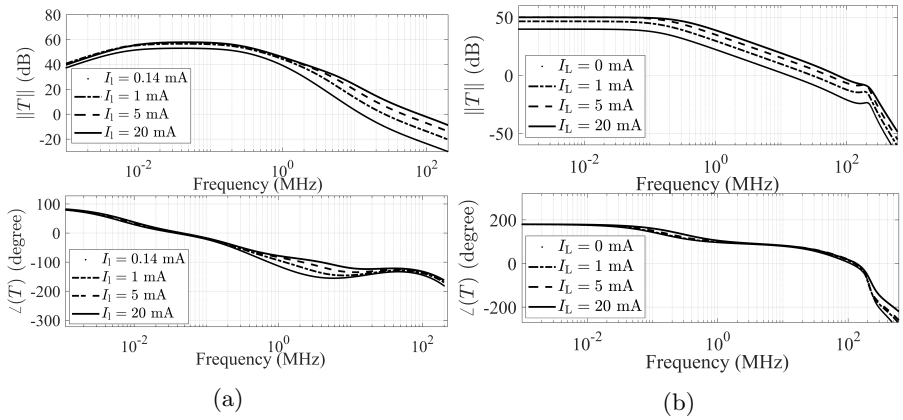


Fig. 6: Simulated open-loop transfer function for the fast-loop (a) CBMC with $\mathrm{C_L} = 80\,\mathrm{pF}$ and (b) FVF with $\mathrm{C_L} = 180\,\mathrm{pF}$. Load current ranging from $I_{\mathrm{L}}^{\mathrm{min}}$ to 20 mA.

where A_∞ is the ideal closed-loop gain (8), H is the transfer function v_{out}/v_1 (9) and C_1 is the parasitic capacitance seen from the EA output node.

$$A_\infty = \frac{g_{\mathrm{mEA}}}{1/g_{\mathrm{m10}} + 1/sC_{\mathrm{m}}} \tag{8}$$

$$H = \frac{v_{\mathrm{out}}}{v_1} \approx -\frac{g_{\mathrm{m1}} g_{\mathrm{m5}} g_{\mathrm{mP}} r_{\mathrm{o3}} r_{\mathrm{L}}}{g_{\mathrm{m2}}} \frac{1 + s\frac{(g_{\mathrm{m1}}+g_{\mathrm{m2}})R_{\mathrm{Z}}C_{\mathrm{z}}}{g_{\mathrm{m1}}}}{s^2\frac{R_{\mathrm{z}}C_{\mathrm{z}}C_2}{g_{\mathrm{m2}}} + s\frac{C_{\mathrm{z}}}{g_{\mathrm{m2}}} + 1} \frac{1}{1 + sr_{\mathrm{o3}}C_3} \frac{1}{1 + sr_{\mathrm{L}}C_{\mathrm{L}}} \tag{9}$$

Provided that the pole introduced by the Compensation Buffer at $g_{\mathrm{m10}}/C_{\mathrm{m}}$ lies at a much higher frequency than the UGF, the CBMC boosts the fast loop UGF by a factor of C_{m}/C_1 w.r.t the standard Miller compensation. Moreover, to ensure the voltage regulator stability in all load conditions, an Active Zero (AZ) circuit was introduced to partially compensate the output pole at $1/(r_{\mathrm{L}}C_{\mathrm{L}})$ thereby boosting the phase around the UGF [6].
As highlighted in [3], improving the loop bandwidth enhances the transient performance of the voltage regulator by reducing the response time (t_{r}). Ensuring the stability of the voltage regulator, a reduction in t_{r}, for a given current step and a specified ΔV_{out} requirement allows for a reduction of C_{L}. Given that the capacitance C_{L} represents a significant fraction of the silicon area, the result of an advanced compensation is a substantial reduction of the silicon area.

4 Simulation results

The proposed high-voltage OCL-LDO was designed and simulated, referring to a 0.35 µm High Voltage (HV) CMOS technology [10], to meet the specifications

Table 1: Specification designed OCL-LDOs

Parameter	**Value**	**Parameter**	**Value**
V_{IN}^{MAX}	24 V	V_{do}	1 V
V_{OUT}	3.3 V	$I_{\mathrm{L}}^{\mathrm{max}}$	20 mA
V_{DD}	3.3 V	Tech.	0.35 µm

listed in Table 1. In the design, the fast-loop bandwidth and the output capacitance (C_{L}) were optimized to limit the output voltage droop to 330 mV (10% of V_{out}). To compare the CBMC OCL-LDO with a reference architecture, the FVF-based voltage regulator in Fig. 2 was also designed to meet the same design specifications.

Figure 6a shows the magnitude and phase of the fast-loop gain for the proposed LDO, achieving a UGF of 81 MHz with a corresponding phase margin of 52.5°. Furthermore, it should be noted that the maximum bandwidth and phase margin occur at the maximum load current $I_{\mathrm{L}}^{\mathrm{max}}$. This ensures the shortest response time without oscillations in the worst case scenario of a load current variation from $I_{\mathrm{L}}^{\mathrm{mim}}$ to $I_{\mathrm{L}}^{\mathrm{max}}$. Analyzing the results of the FVF-based solution (Fig. 6b), at the maximum load current, the fast-loop achieves a UGF of 70.3 MHz and a phase margin of 35°. In accordance with the equation (5), the worst-case phase margin occurs at the maximum load current, potentially leading to oscillations during the response time. Despite both architectures showing comparable bandwidth, the CBMC solution requires a load capacitance ($\mathrm{C_L}$) of merely 80 pF compared to $\mathrm{C_L}$ = 180 pF for the FVF, resulting in an estimated silicon area reduction by a factor of 2.25.

Such a high bandwidth enhances the transient performance of the regulators as shown in Fig. 7. Indeed, for a load current step ranging from 0.14 mA to 20 mA, the output voltage droop remains below 10% of V_{out} for both the CBMC and the FVF LDO. In previous works [5]-[6], when the response time approaches the edge time, t_{r} is estimated as in (10), where ΔV_{out} is the voltage droop at t_{r}. Substituting the results of Fig. 7 in (10) the FVF-based LDO has t_{r} = 2.4 ns while the proposed CBMC OCL-LDO presents t_{r} = 1.6 ns.

$$t_r = \sqrt{\frac{2C_{\mathrm{L}}\Delta V_{\mathrm{out}}T_{\mathrm{edge}}}{\Delta I_{\mathrm{L}}}} \tag{10}$$

Therefore, while both topologies have comparable performance in terms of frequency behavior and response time, the CBMC-based architecture outperforms the conventional FVF-based architecture in reducing the load capacitance. Additionally, the CBMC OCL-LDO shows a response time lower than that of the most recent high-voltage LDOs [8]-[9] comparable to the of state-of-the-art low-voltage OCL-LDOs [5]-[6].

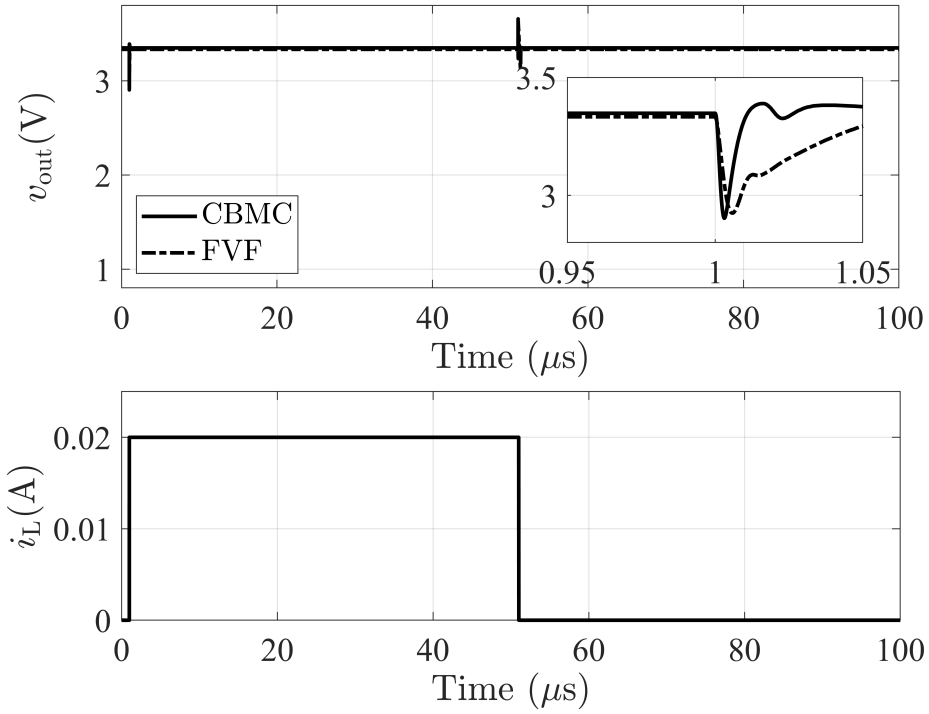


Fig. 7: Simulated load transient response, load current ranging from 0.14 mA and 20 mA, with $T_{\text{edge}} = 1\,\text{ns}$, $V_{\text{IN}} = 9\,\text{V}$ and $V_{\text{IN}} = 3.3\,\text{V}$.

Conclusion

In this paper, an OCL-LDO designed for load current fast transient response and suitable for high-voltage applications has been presented. It exploits the current buffer Miller compensation scheme, which make possible the design of the fast feedback loop using a low-voltage CMOS technology. The CBMC OCL-LDO was designed and its features compared with those of a FVF-based reference architecture. The investigation highlighted that the silicon area occupied by the proposed voltage regulator is 2.25 times smaller than that needed by the FVF-based topology.

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