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A Filtering Single-Ended-to-Balanced Power Divider With Enhanced Ultra-Wideband Suppression

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Abstract. In this paper, a four-parallel-coupled line is applied for the design of a novel filtering single-ended-to-balanced power divider. To facilitate the even- and odd-mode analysis of the symmetric structure, the proposed four-parallel-coupled line is split into two parallel coupled lines, and the closed-form design equations at f_0 are given. Moreover, the coupled lines and open-circuited stubs between the four-parallel-coupled line and balanced output ports can realize performances of high-selectivity filtering and enhanced ultra-wideband common-/differential-mode suppression. By regulating two impedances of the OC stubs, three prototypes with different filtering bandwidths are designed and simulated. Among them, the circuit with the high-selectivity is fabricated and measured. Measurements agree well with simulations and ideal results, which verifies the validity of the theoretical derivations and circuit feasibility.

Keywords: Common-mode, differential-mode, enhanced ultra-wideband suppression, four-parallel-coupled line, high-selectivity filtering, power divider, single-ended-to-balanced.

1 Introduction

As one of the most essential components in microwave and radio frequency (RF) systems, various kinds of power dividers (PDs) are widely used in many wireless communication circuits such as mixers, power amplifiers, multichannel communication networks, and phased array radars, etc. Therefore, the investigation of multifunctional and high-performance PDs has always been one of the top priorities in the field of microwave and RF front ends. As a typical type of PDs, the related researches on the Wilkinson-type PD [1] are very extensive. Coupled lines (CLs) are commonly used to realize the dual frequency band, filtering function, and multi-way outputs of the Wilkinson PD [2–5]. Moreover, the multifunctional reconfigurable filtering PDs in [6] and [7] are also achieved by integrating the CL with varactor diodes.

In addition to the traditional single-ended-to-single-ended (SETSE) structures mentioned above, PDs can also be classified as balanced-to-single-ended (BTSE) PDs,

balanced-to-balanced (BTB) PDs, and single-ended-to-balanced (SETB) PDs according to different types of input and output ports. Compared with the traditional SETSE devices, circuits using the topology of balanced ports are more complex to design, but it can significantly reduce the common-mode (CM) noises, inherent electromagnetic (EM) radiation interference caused by the multifrequency operating modes, and enhance the efficiency of systems as well [13]. Several SETB PD are proposed based on microstrip lines [8–10], the double-sided microstrip-to-slotline structure [11], the defected ground structure [12], CLs [13–14], and the three-parallel-coupled line [15]. However, few researches show advantages of simple structure, outstanding filtering performance, and enhanced wideband CM/DM isolation.

In this paper, a planar filtering SETB PD with enhanced ultra-wideband CM and DM suppression utilizing the four-parallel-coupled (FPC) line is designed, which can be equivalent to a complex system composed of the Wilkinson PD, bandpass filters, and two baluns, as presented in Fig. 1. Advantages of the proposed SETB PD can be summarized as follows. 1) Planar and compact structure with the in-phase characteristic and an equal power division. 2) All five ports are well matched and the closed-form design formulas are derived. 3) High-selectivity filtering performance from SE input port to two balanced output ports. 4) Adjustable filtering bandwidth which is only related to two characteristic impedances of OC stubs. 5) Enhanced ultra-wideband isolation and suppression under the CM/DM excitations of two balanced output ports. 6) Deep and wideband mode-conversion (MC) suppression.

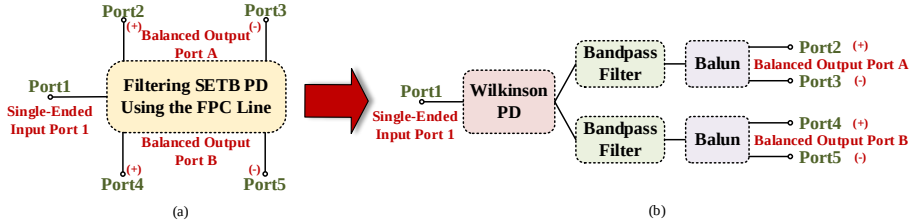


Fig. 1. (a) The proposed filtering FPC-line SETB PD and (b) its equivalent circuit systems.

2 Circuit Theory and Analysis at Center Frequency

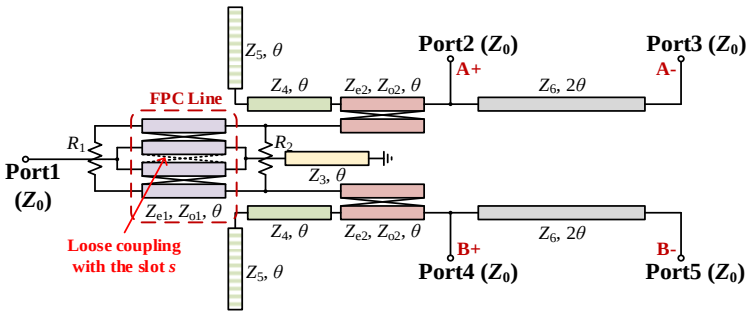


Fig. 2. Circuit schematic of the proposed filtering SETB PD using the FPC line.

2.1 Circuit Analytical Procedures

As depicted in Fig. 2, due to the inherent symmetrical structure of the proposed SETB PD along the horizontal direction, the method of even- and odd-mode analysis can be applied. The generalized even- and odd-mode analytical method is introduced in [16], and the two-step analytical procedure can be adopted as follows.

Step 1. Assuming that the input P1 is well matched, then a symmetric $2n = 4$ network (P2-P5) can be obtained, which has even- and odd-mode scattering matrices expressed as

$$\begin{cases} S^{\mathrm{o}} = \begin{bmatrix} S_{22}^{\mathrm{o}} & S_{23}^{\mathrm{o}} \\ S_{32}^{\mathrm{o}} & S_{33}^{\mathrm{o}} \end{bmatrix} = -\frac{1}{2}\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \\ S^{\mathrm{e}} = \begin{bmatrix} S_{22}^{\mathrm{e}} & S_{23}^{\mathrm{e}} \\ S_{32}^{\mathrm{e}} & S_{33}^{\mathrm{e}} \end{bmatrix} = -\frac{1}{2}\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \end{cases}. \tag{1}$$

Step 2. Ensuring that the input P1 can be perfectly matched when the output ports P2-P5 are all well matched, which means

$$S_{11} = 0. \tag{2}$$

2.2 Specific Theoretical Analysis of the SETB PD Model

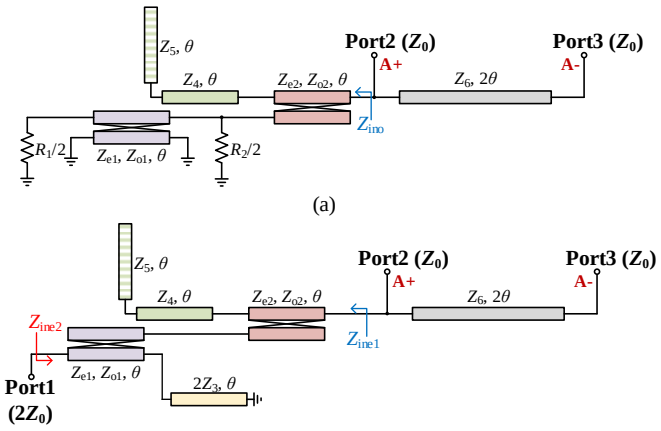


Fig. 3. Model of the split-FPC-line based SETB PD under (a) odd-mode. (b) even-mode.

The proposed filtering SETB PD configuration is composed of an FPC line, two CLs, several TL stubs, and two isolated resistors, as displayed in Fig. 2. The termination impedances of five ports are all Z_0. Referring to the method in [17], to simplify the theory analysis, the FPC line is split into two parallel CLs temporarily due to the as-

sumed loose coupling, and the effect of the slot *s* between the two parallel CLs is discussed in the subsequent section. In this section, the even-/odd-mode models of the proposed SETB PD are discussed, and their characteristic impedances of the CLs are Z_{ei}/Z_{oi} (i = 1, 2), respectively. The electrical length θ is assigned as 90° at f_0.

Odd-Mode Analysis. The odd-mode circuit of the split-FPC-line based SETB PD is displayed in Fig. 3(a). According to the analysis theory of CLs in [18], the input impedance of the filtering CL can be calculated as

$$Z_{\text{ino}} = \frac{(Z_{e2} - Z_{o2})^2[16Z_{e1}^2 Z_{o1}^2 + R_1 R_2 (Z_{e1} + Z_{o1})^2]}{32R_2 Z_{e1}^2 Z_{o1}^2}. \tag{3}$$

According to the network cascade theory and the matrix conversion relationship, the odd-mode *S*-parameters matrix between port 2 and port 3 can be obtained as

$$\begin{bmatrix} S_{22}^{o} & S_{23}^{o} \\ S_{32}^{o} & S_{33}^{o} \end{bmatrix} = \begin{bmatrix} \dfrac{Z_0}{2Z_{\text{ino}} - Z_0} & \dfrac{2Z_{\text{ino}}}{Z_0 - 2Z_{\text{ino}}} \\ \dfrac{2Z_{\text{ino}}}{Z_0 - 2Z_{\text{ino}}} & \dfrac{Z_0}{2Z_{\text{ino}} - Z_0} \end{bmatrix}. \tag{4}$$

Finally, by combining equations (1), (3), and (4), the relationship between the CL impedances and the isolation resistors of the SETB PD should be

$$\frac{(Z_{e2} - Z_{o2})^2[16Z_{e1}^2 Z_{o1}^2 + R_1 R_2 (Z_{e1} + Z_{o1})^2]}{16R_2 Z_{e1}^2 Z_{o1}^2} = Z_0. \tag{5}$$

Even-Mode Analysis. As shown in Fig. 3(b), the termination impedance of port 1 is $2Z_0$ under the even-mode excitation. Therefore, the analytical procedure should be divided into two parts.

Analysis when port 1 is well matched. The even-mode input impedance of the filtering CL viewed from right to left can be obtained by using the analysis theory of CLs in [18] as

$$Z_{\text{ine1}} = \frac{2Z_0 (Z_{e2} - Z_{o2})^2}{(Z_{e1} - Z_{o1})^2}. \tag{6}$$

Similarly, the even-mode *S*-parameters matrix between port 2 to port 3 is

$$\begin{bmatrix} S_{22}^{e} & S_{23}^{e} \\ S_{32}^{e} & S_{33}^{e} \end{bmatrix} = \begin{bmatrix} \dfrac{Z_0}{2Z_{ine1} - Z_0} & \dfrac{2Z_{ine1}}{Z_0 - 2Z_{ine1}} \\ \dfrac{2Z_{ine1}}{Z_0 - 2Z_{ine1}} & \dfrac{Z_0}{2Z_{ine1} - Z_0} \end{bmatrix}. \tag{7}$$

Finally, by combining equations (1), (6), and (7), the relationship between the two CL impedances should meet the condition of

$$\frac{Z_{e2} - Z_{o2}}{Z_{e1} - Z_{o1}} = \frac{1}{2}. \tag{8}$$

Analysis when port 2-5 are all well matched. It is noteworthy that port 1 is shorted under the odd-mode excitation, so the analysis of port 1 matching condition only needs to consider the even-mode excitation, namely

$$S_{11} = S_{11}^{e} = 0. \tag{9}$$

According to the input impedance equation of the TL, the even-mode input impedance of port 1 viewed from left to right can be obtained as

$$Z_{ine2} = \frac{Z_0 (Z_{e1} - Z_{o1})^2}{2(Z_{e2} - Z_{o2})^2} = 2Z_0. \tag{10}$$

It is obvious that the value of Z_{ine2} satisfies the impedance matching condition of port 1 under the even-mode excitation automatically, so the equation (9) is valid.

3 Circuit Design Discussion

3.1 Full-Circuit Simulation

According to the even- and odd-mode theoretical analysis at f_0 = 3.5 GHz in Section 2, as long as the parameters in the SETB PD meet limiting conditions of (5) and (8), the circuit is realizable in practice with arbitrary selected TL impedances of Z_3, Z_4, Z_5, and Z_6. Within the feasibility of the fabrication technology, parameters of the full circuit are selected and calculated as Z_{e1} = 117 Ω, Z_{o1} = 46 Ω, Z_{e2} = 92 Ω, Z_{o2} = 56.5 Ω, R_1 = 240 Ω, R_2 = 39 Ω, Z_3 = 54 Ω, Z_4 = 58 Ω, Z_5 = 44 Ω, Z_6 = 20 Ω, and θ = 90°.

Ideal results of the split-FPC-line based SETB PD are plotted in Fig. 4, which shows advantages of high-selectivity filtering function and ultra-wideband DM isolation (The subscript c, d, and s indicates the CM, DM, and the SE port, respectively). The 6-dB bandwidth of the power division from the SE port to two balanced ports $|S_{dsA1}|$ ($|S_{dsB1}|$) is 20.0%. The 15-dB bandwidths of the SE port return loss $|S_{ss11}|$ and the balanced port DM signals isolation $|S_{ddAA}|$ is 8.6% and 10.3%, respectively. Moreover,

the proposed SETB PD also shows superiorities of enhanced ultra-wideband MC and CM noise suppression, as shown in Fig. 4(b).

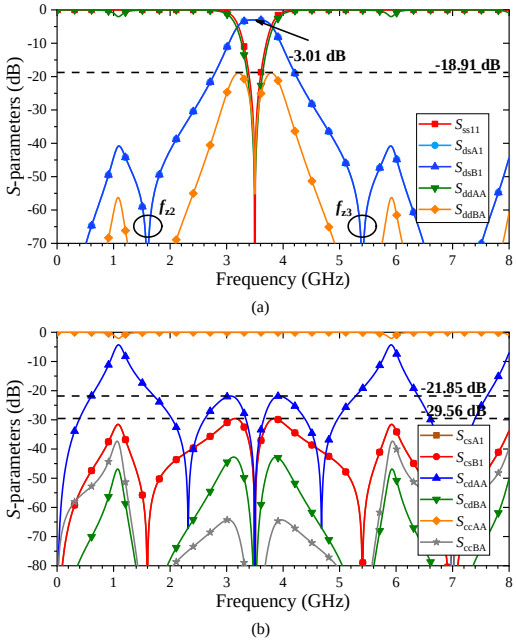


Fig. 4. Ideal results of the split-FPC-line based SETB PD.

The frequencies of transmission zeros (TZs) are shown in (11). It can be seen that impedances Z_4 and Z_5 determine the frequencies of TZ2 and TZ3, and the values of f_{z2} and f_{z3} affect the bandwidth of the circuit directly. Since impedance Z_4 = 58 Ω and Z_5 = 44 Ω, the values f_{z2} and f_{z3} are calculated as 1.60 and 5.40 GHz, respectively, which are consistent with the simulations shown in Fig. 4(a).

$$f_{z1} = 0,\quad f_{z2} = \frac{2f_0}{\pi}\arctan\sqrt{\frac{Z_5}{Z_4}},\quad f_{z3} = 2f_0 - \frac{2f_0}{\pi}\arctan\sqrt{\frac{Z_5}{Z_4}},\quad f_{z4} = 2f_0. \tag{11}$$

3.2 Slot *s* of the FPC Line

For simplification of the previous calculations and theoretical analysis, the FPC line is split into two CLs and the coupling caused by slot *s* between two CLs is ignored. It is worth mentioning that the values of slots between two adjacent lines in the FPC line are all equal to *s*. In Fig. 5, the FPC line structure is compared with the equivalent split-FPC-line structure. It is obvious that the simulations show little difference between two cases, which also validates that a loose coupling exists between two adjacent CLs in the FPC line. Therefore, to minimize the size and simplify the

structure of the circuit as much as possible, the simulation and fabrication of the SETB PD are all carried out according to the FPC line structure in the subsequent analysis and discussion.

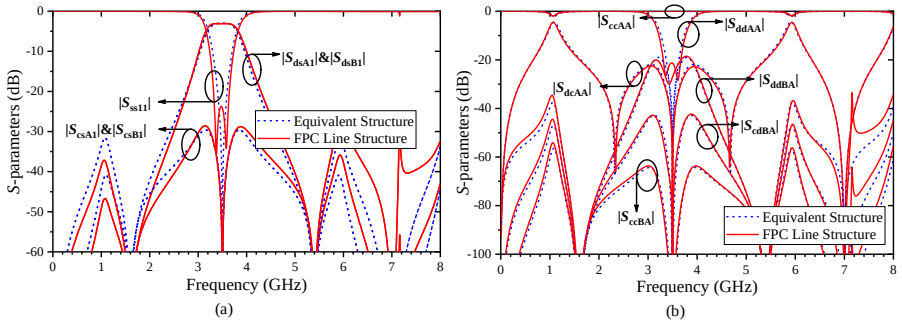


Fig. 5. Simulation comparison of the split-FPC-line structure and the FPC line structure.

3.3 Circuit Analysis With Different Parameters

As discussed previously, the impendences variation of the TLs has no effect to the performance of the proposed circuit at f_0. However, the influences of their variation cannot be ignored within the whole band range.

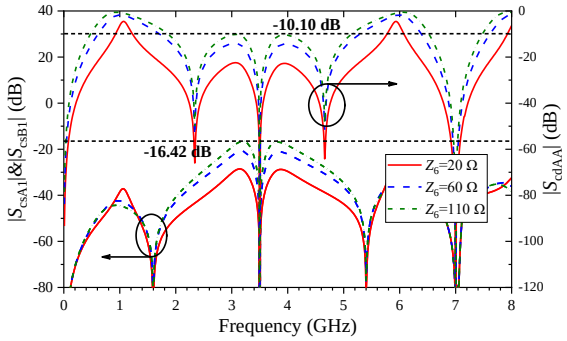


Fig. 6. Simulated *S*-parameters of the FPC-line based SETB PD with different value of Z_6 for $|S_{csA1}|$, $|S_{csB1}|$, and $|S_{cdAA}|$.

The simulated *S*-parameters of the FPC-line based SETB PD with different values of Z_6 are illustrated in Fig. 6. The varying of Z_6 has a great influence on the CM noises and MC suppression performances. As the Z_6 decreases from 110 Ω to 20 Ω, the MC suppression $|S_{cdAA}|$ increases from 10 dB to about 25 dB, meanwhile, the CM noises suppression $|S_{csA1}|$ ($|S_{csB1}|$) also improves from about 16 dB to 30 dB. Apparently, the circuit shows a better performance with a smaller Z_6 within the allowable value range of the fabrication. Moreover, it is also noteworthy that the loss of the SETB PD

can increase undesirably with large values of isolated resistors. Therefore, R_1 and R_2 should be set as small as possible within the appropriate range.

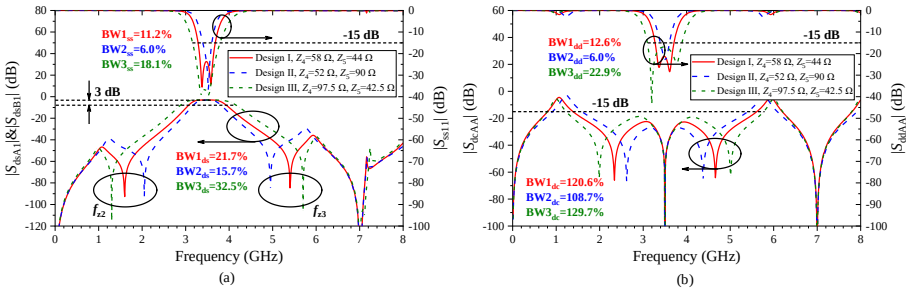


Fig. 7. Simulated *S*-parameters of the proposed SETB PD with different values of Z_4 and Z_5.

As calculated in (11), impedances Z_4 and Z_5 determine the frequencies of TZ2 and TZ3, which affect the bandwidth of the circuit directly, as depicted in Fig. 7 with Design I to III. Circuit parameters of the three designs are listed in Table I. The value of Z_3 should be adjusted slightly for a better performance of simulated *S*-parameters. The width, slot, and length of the FPC line are represented as *w*, *s*, and *l*, respectively. All structures are implemented on the 0.762-mm Rogers RO4350B substrate with ε_r = 3.66 and tanδ = 0.0037.

Table 1. Circuit Parameters of Fig. 7

	Dimensions (mm)			Impedances and Resistors (Ω)							
	w	***s***	***l***	Z_{e2}	Z_{o2}	Z_3	Z_4	Z_5	Z_6	R_1	R_2
Design I	0.54	0.20	13.19	99.7	57.9	54	58	44	20	240	39
Design II	0.56	0.22	13.09	101.7	60.2	56	52	90			
Design III	0.48	0.16	12.93	105.7	56.4	49.9	97.5	42.5			

3.4 Design Procedure

Based on the analysis and discussion mentioned above, the complete design procedure of the proposed SETB PD using the FPC line is summarized as follows.

Step 1. Specify the operating center frequency f_0 of the SETB PD.

Step 2. Simplify the FPC line into two parallel CLs. According to (5) and (8), determine and calculate values of two isolated resistors and the even-/odd-mode impedances of CLs in the circuit.

Step 3. Following the analysis and discussion of Fig. 6, select the appropriate value of Z_6 for a better performance of the SETB PD.

Step 4. Based on the relationship in (11), determine the required bandwidth of the circuit and calculate the values of f_{z2}, f_{z3}, Z_4, and Z_5. Adjust the impedance Z_3 slightly according to the simulated results.

Step 5. Construct the FPC line equivalent to the two parallel CLs, keeping the width *s* of the slot between two adjacent lines equal.

Step 6. Choose the substrate for the prototype implementation, convert the electrical quantities into physical dimensions and optimize if necessary.

4 Experiments and Discussion

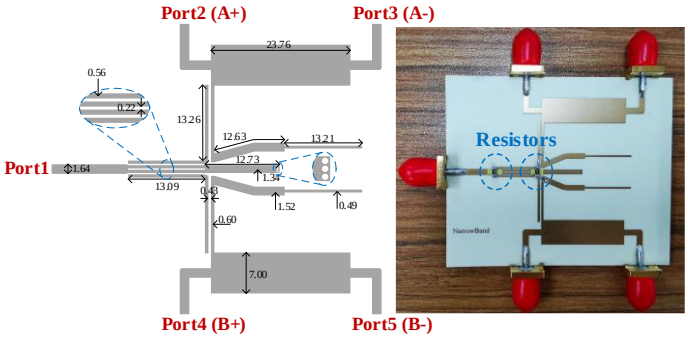


Fig. 8. Layout and photograph of the SETB PD with marked physical dimensions (unit: mm).

For a further verification, the proposed SETB PD with the high-selectivity filtering function (Design II) is implemented, measured, and demonstrated. The ideal model results and schematic simulations are all performed on Advanced Design System (ADS) software, while the measurements are accomplished on the vector network analyzer (VNA) of ROHDE&SCHWARZ ZVA67. Since the VNA is a four-port instrument while the measured SETB PDs have five ports, a 50-Ω load is needed to connect with the no-load port during the measurement. The layout and photograph of the fabricated prototype is presented in Fig. 8 with marked physical dimensions. Ideal results, schematic simulations, and measurements can be seen in Fig. 9.

In Fig. 9(a), the measured DM isolation $|S_{ddAA}|$ ($|S_{ddBB}|$) has a 6.6% 10-dB bandwidth. The DM suppression level $|S_{ddAB}|$ ($|S_{ddBA}|$) is higher than 14.9 dB in the whole frequency range 0-2.3f_0. As shown in Fig. 9(b), the measured $|S_{ccAB}|$ ($|S_{ccBA}|$) shows enhanced ultra-wideband performance of more than 30 dB suppression from 0 to 5.7 GHz (0-1.63f_0), and the CM noises suppression between the SE and balanced ports $|S_{csA1}|$ ($|S_{csB1}|$) has a 121.7% 20-dB bandwidth. In Fig. 9(c), the $|S_{dcAA}|$ ($|S_{dcBB}|$) shows a 112.9% 15-dB bandwidth and the $|S_{dcAB}|$ ($|S_{dcBA}|$) shows a suppression greater than 20 dB in the whole band within 0-2.3f_0.

Finally, the comparisons between simulations and measurements of the SE port isolation, the power dividing, and the phase difference are illustrated in Fig. 9(d). The frequency deviations of $|S_{dsA1}|$ ($|S_{dsB1}|$) and the variation of $\angle(S_{dsA1}/S_{dsB1})$ at TZs can be due to the discontinuities of CLs, the different phase velocities of even- and odd-mode of CLs, the inaccuracy of fabrication, and the reasonable measurement errors. The 15-dB bandwidth of the SE port isolation $|S_{ss11}|$ is about 6.1% and the 6-dB bandwidth of $|S_{dsA1}|$ ($|S_{dsB1}|$) is about 12.9%. The filtering transition bandwidths of $|S_{dsA1}|$ ($|S_{dsB1}|$) from -6 dB to -20 dB are 0.29 and 0.21 GHz at low and high frequencies, respectively, which shows the high-selectivity performance of the SETB PD.

Moreover, the $|S_{dsA1}|$ ($|S_{dsB1}|$) is -4.26 dB (-4.56 dB) at f_0 and the minimum power loss is 1.36 dB at 3.49 GHz. The in-band fluctuation of the phase difference $\angle(S_{dsA1}/S_{dsB1})$ is 0° ± 2°.

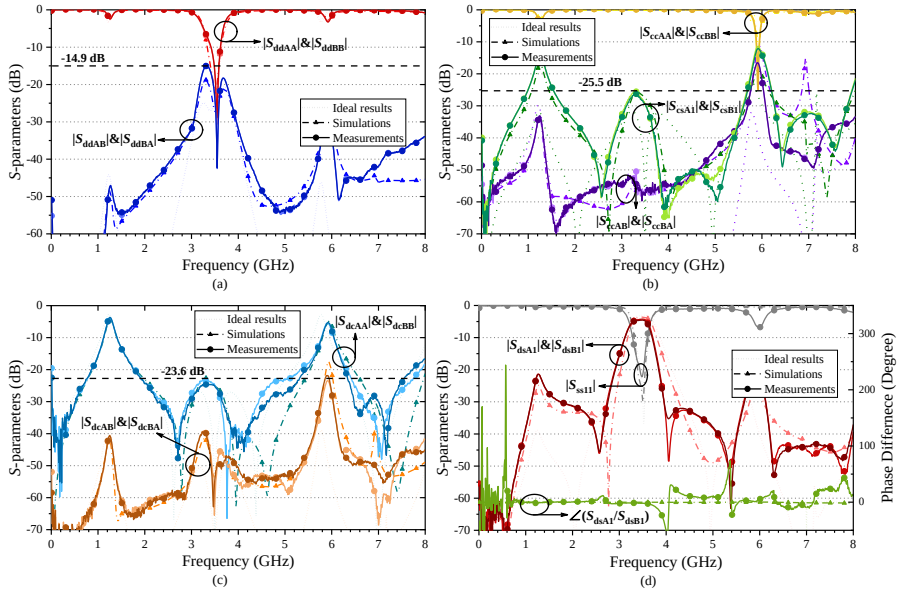


Fig. 9. Ideal results, simulations, and measurements of the SETB PD.

5 Conclusion

In this paper, a high-selectivity filtering SETB PD with enhanced ultra-wideband CM/DM isolation and suppression using the FPC line has been proposed. The closed-form equations, theory analysis, and complete design procedure have also been provided. By adjusting two impedances of the OC stubs, three designs with different bandwidths have been simulated. Moreover, ideal results, schematic simulations, and measurements of the prototype with the high-selectivity filtering function have been given and discussed thoroughly. The enhanced efficiency and the capability of reducing CM noises and the EM interference allow the proposed structure to be widely used in feeding arrays, high-selectivity microwave/RF systems, and multichannel communication networks.

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