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High-Gain and High-Linearity MMIC GaN Doherty Power Amplifier With 3-GHz Bandwidth for *Ka*-Band Satellite Communications

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***Abstract*— This letter presents the design of a Doherty power amplifier (DPA) for satellite applications in the *Ka*-band downlink (17.3–20.3 GHz) implemented on a 100-nm GaN–Si HEMT technology. The design aims to achieve high gain and very high intrinsic linearity over a wide bandwidth of 3 GHz. The experimental characterization on the fabricated chip demonstrates that the DPA can maintain a noise-to-power ratio (NPR) higher than 25 dB and power-added efficiency (PAE) of 30% while providing 36 dBm of output power, when tested with a 100-MHz uniformly distributed signal, achieving state-of-the-art performance among the integrated power amplifiers for satellite communications.**

***Index Terms*— Doherty power amplifier (DPA), GaN, linearity, monolithic microwave integrated circuit (MMIC), noise-to-power ratio (NPR), satellite.**

I. Introduction

ENERGY-EFFICIENT power amplifiers play a crucial role in cost reduction for satellite transmitters, as poor efficiency can affect the power budgets, thermal design, and overall weight considerations [1]. On the other hand, the present trend toward higher carrier frequencies, multicarrier signals, and complex nonconstant envelope modulations such as quadrature amplitude modulation (QAM) [2] significantly influences the design of the PA, impacting not only energy consumption but, most importantly, on linearity.

Regarding efficiency enhancement, the Doherty power amplifier (DPA) [3] has emerged as the benchmark solution at cellular frequencies. However, extending its application to the *Ka*-band poses significant challenges, particularly when faced with conflicting requirements such as the ones of satellite transmissions in terms of high power at the chip level, effective thermal management, and superior linearity across gigahertz bandwidths. The few examples available in the literature [4], [5] present promising results in terms of power, gain, and efficiency, but may not have sufficient intrinsic linearity to be deployed without additional linearizers. Since the removal of linearizers is highly desired to reduce cost, weight, and complexity, the development of very linear PAs that can cope with stringent linearity marks with no additional linearization becomes mandatory, especially in view of their adoption with extremely wide instantaneous bandwidths.

In this research, we present the design and experimental assessment of a three-stage monolithic microwave integrated circuit (MMIC) GaN–Si DPA designed for the satellite downlink *Ka*-band between 17.3 and 20.3 GHz. Adopting a novel approach focused on intrinsic linearity, the DPA demonstrates remarkable performance, achieving in the whole band 36-dBm output power, 24-dB linear gain, PAE higher than 23% both at saturation and 6-dB output power back-off (OBO), and an amplitude-to-phase modulation (AM/PM) always lower than $\pm 12^\circ$. The corresponding noise-to-power ratio (NPR) under 100-MHz uniform white noise excitation is higher than 25 dB, demonstrating the effectiveness of the proposed strategy.

II. Specifications and Design Approach

This design targets to cover the satellite downlink *Ka*-band (17.3–20.3 GHz) with a single-chip GaN DPA able to provide 36 dBm of output power while maintaining a power-added efficiency (PAE) around 35% and a high intrinsic linearity, to avoid employing an external linearizer on board of the satellite. The linearity target is expressed in terms of NPR, which should be higher than 15 dB in all conditions, including when the amplifier is fed by a modulated signal having instantaneous bandwidth close to 3 GHz. Since the NPR is typically difficult to predict at the simulation level during the design, the linearity specification is translated for design purposes to AM/PM, which should be maintained approximately within $\pm 15^\circ$ [4]. Furthermore, the small-signal gain should be of the order of 30 dB, and input and output return losses higher than 15 dB. All specifications should be guaranteed while maintaining the transistors' maximum junction temperature (T_j) below 160 °C in all conditions [6].

The design is carried out in the 100-nm gate length GaN-Si HEMT process by OMMIC, which features around 3 W/mm at 12-V drain supply voltage and was not space-qualified at the time of the design. To comply with the derating rules required by the space applications as well as with the constraint on the maximum T_j, all transistors have to be operated at a reduced drain supply voltage of 9 V. This lowers the effective power density to around 2.25 W/mm, thus requiring the combination of a significant number of transistors in the final stage to comply with the output power specification. On the other side, the target small-signal gain calls for a three-stage architecture,

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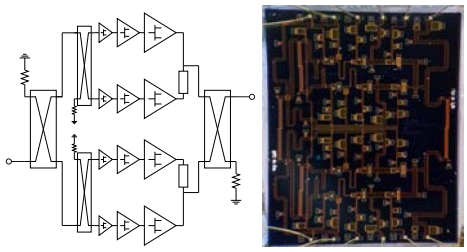


Fig. 1. Block diagram (left) and microscope photograph (right) of the fabricated MMIC DPA (5 × 6 mm^2).

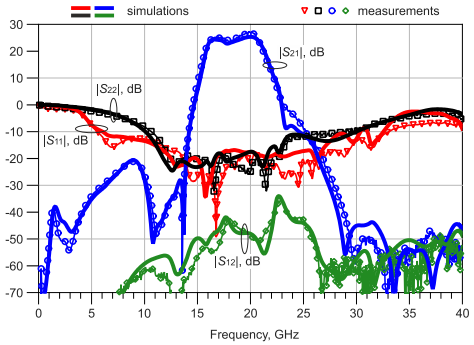


Fig. 2. Simulated (solid) and measured (symbols) scattering parameters.

accounting for the gain penalty typical of the DPAs and a gain of the individual transistors (after stabilization) around 10 dB.

The design of a DPA is strongly based on a reliable large signal model, especially in a frequency range where the reactive parasitics of the transistors have a significant effect and contribute to power- and frequency-dependent signal dephasing. Therefore, the choice falls on the combination of four 8 × 100 μm devices in the final stage, for which the foundry provides a nonlinear and thermal model, and a load–pull measurement campaign is performed [7]. The output return loss requirement is rather critical in a DPA since it typically conflicts with the two-point matching requirements needed for the combiner to synthesize the desired load modulation. Under this respect, the need to combine the power of several transistors at the MMIC level allows for the implementation of two individual DPA cells with half of the target power rating and operation in a balanced configuration using input and output Lange couplers, as shown in the block diagram of Fig. 1.

The DPA can be designed to be linear as well as efficient by appropriate selection of its combiner topology and characteristics [8]. However, the design of the driver stages also has a strong impact on the efficiency and linearity tradeoff sought, both in terms of size, position, and matching. The DPA linearity is only maintained if two conditions are met: the main chain presents a relatively flat phase characteristic in the low-power region when the auxiliary is off; the auxiliary chain has a phase characteristic that compensates the one of the main chains in the high-power (efficiency enhancement) region. The first condition calls for a tradeoff with a small-signal gain since the selected technology does not feature hot vias and therefore the complex architecture requires all the transistors in the main stage to share the same dc bias gate voltage ($V_{G,M}$) to reduce the routing complexity. The selection of the optimum $V_{G,M}$ for AM/PM corresponds to a small-signal gain that is slightly lower than the target one. The combiner topology is based on a 90° impedance inverter on the main side and two 90° line sections on the auxiliary, following an approach similar to [5]. Given the relatively wide operating bandwidth, the combiner is optimized privileging efficiency at the back-off point and output power at saturation. Two driver stages are embedded in each branch of the DPA cell, with the respective periphery of 6 × 50 μm and 2 × 50 μm.

Since a fully symmetric topology is adopted, the same transistor sizes are used in all stages of the main and auxiliary chains. By using the same matching network topology for the main and auxiliary branches, the phase difference is maintained uniformly over frequency. Thanks to the adoption of a Lange coupler as the input splitter of the DPA cell, the phase difference is minimized and no further phase delay is added, thus enhancing the wideband operation. The slow turn-on of the auxiliary and its lower peak current at saturation can be partially compensated by properly tuning the class C bias point of the auxiliary 8 × 100 μm ($V_{G,Af}$) and 6 × 50 μm ($V_{G,Adr}$) devices. The first driver stage, instead, is biased in class AB on both branches to avoid the mismatch and dephasing effect of the power-dependent input capacitance on the input splitter terminations. After layout optimization, the overall circuit fits a chip size of (5 × 6) mm^2. The microscopic photograph of the manufactured chip is shown in Fig. 1.

III. Experimental Characterization

The whole characterization is performed at the nominal bias point: $V_{G,M} = -1.45$ V, $V_{G,Adr} = -2.05$ V, $V_{G,Af} = -2.4$ V, $V_{DD} = 9$ V, corresponding to a total current $I_D = 66$ mA.

The small-signal characterization is performed from 0.1 to 40 GHz. Fig. 2 shows a very good agreement of the measured (symbols) and simulated (solid) scattering parameters over the whole frequency range. The measured small-signal gain is higher than 24 dB from 16.3 to 20.8 GHz, where the associated input and output return losses are better than 20 dB, thanks to the wideband isolation of the Lange couplers. Overall, the target bandwidth is covered with considerable margins, and no frequency shift is experienced.

The continuous-wave (CW) power sweeps at three frequencies in the design band (17.8, 18.8, and 19.8 GHz) are shown in Fig. 3. The desired back-off efficiency enhancement as well as a flat AM/PM characteristic is achieved at all frequencies. The DPA features flat PAE curves in a 5–6 dB OBO range, with values ranging from 23% to 30%, while maintaining a rather limited gain compression and a phase distortion always lower than 12° with no additional linearization. The measured performance reproduces very well the one expected from simulation, in terms of gain levels and compression, dc current consumption, and, especially, AM/PM. There is also a fairly good prediction of the position of the efficiency peaks, although the measured absolute values are around five points lower at comparable output power. The cause of this could be partially ascribed to thermal effects, since the chips are not brazed, but mounted on the carriers adopting a low-temperature conductive epoxy.

The measured CW performance over the target operating band is summarized in Fig. 4. The DPA can cover the 17.3–20.3-GHz frequency range, maintaining saturated power higher than 36 dBm with corresponding PAE and gain higher than 23% and 15 dB, respectively. At 6-dB OBO, the PAE is maintained at the same level as at saturation, with an associated gain higher than 22 dB. Meanwhile, the AM/PM is maintained within ±12° from the back-off to the saturation condition at all frequencies.

The system-level linearity of the DPA is determined by measuring NPR [13] employing the notch technique, which utilizes band-limited white noise with a small central notch as the input signal. The experimental setup used for NPR characterization is depicted in Fig. 5. The baseband signal

TABLE I

PERFORMANCE OF STATE-OF-THE-ART GaN PAs FOR *Ka*-BAND SATELLITE APPLICATIONS

Substrate	Architecture	Freq. (GHz)	$P_{out,sat}$ (dBm)	PAE_{sat} (%)	$PAE_{6dB\,OBO}$ (%)	$Gain_{sat}$ (dB)	Modulation (Type/Bandwidth)	OBO (dB)	$NPR_{@\,OBO}$ (dB)	Ref.
SiC	class-AB	20.5–25.5	38	30	–	20	–	–	–	[9]
SiC	class-AB	27–31	43	25	–	22	–	–	–	[10]
SiC	DPA	20	35	37	18*	17*	Band-limited Gaussian/–	2.5^{+}	15^{+}	[11]
SiC	DPA	17.3-20.3	41.5	35	28	20	DVB-32 APSK/1-GHz	4	15	[4]
Si	DPA	16.3–20.3	36.6	21	19	18	Gaussian/100-MHz	4	17.7	[5]
Si	DPA	17.3-20	36.3	24	18	20	–	–	–	[12]
Si	**DPA**	**17.3–20.3**	**36**	**23**	**23**	**15**	**Uniform/100-MHz**	**1**	**25**	**T.W.**

* Value extrapolated from graphs $^{+}$ Simulated performance

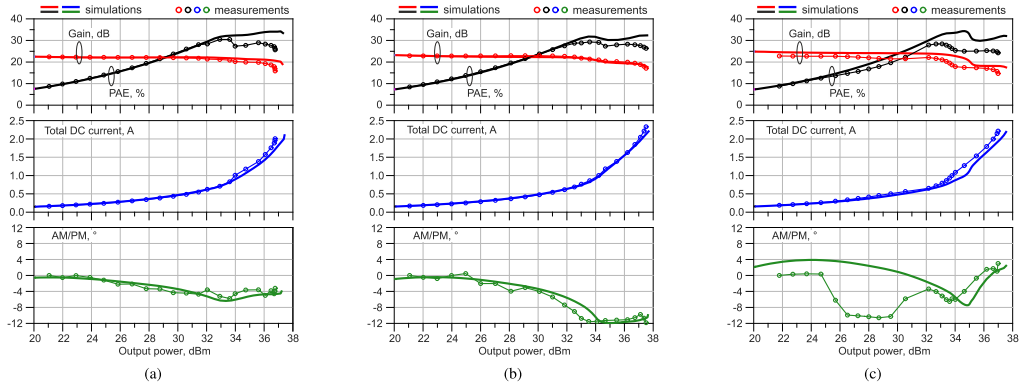


Fig. 3. Comparison of simulated (solid) and measured (symbols) CW power sweeps at (a) 17.8 GHz, (b) 18.8 GHz, and (c) 19.8 GHz.

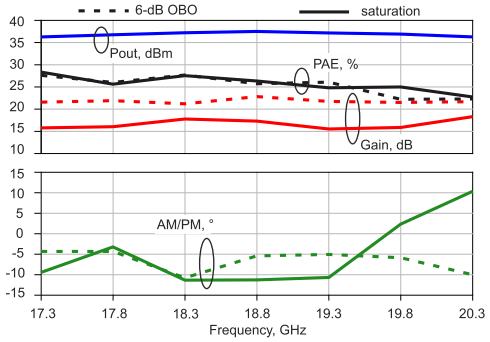


Fig. 4. Measured CW performance from 17.3 to 20.3 GHz.

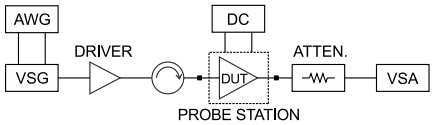


Fig. 5. Experimental setup for the NPR characterization.

is generated using the Keysight M8190A arbitrary waveform generator (AWG), followed by upconversion to the desired carrier frequency using the Keysight E8267D vector signal generator (VSG). Predrivers amplify the input signal to the required power level while ensuring high linearity, with an isolator included for protection. A directional attenuator adjusts the DPA output signal for NPR evaluation using the Keysight N9041B vector signal analyzer (VSA), for the downconversion and waveform capture.

For preliminary assessment, the linearity of the DPA is measured using a low-PAPR white uniform noise with 100-MHz bandwidth, crafted using a multitone technique [14]: 2001 tones evenly distributed across the band, with the central 201 tones deactivated to create a notch. The other tones maintain equal magnitude and phases to ensure uniform statistics for the NPR signal. NPR is evaluated at the DPA output by comparing the average power spectral density of the deactivated tones to the one of the activated tones.

The results of this system-level characterization affirm the excellent intrinsic linearity of the DPA, which maintains NPR higher than 25 dB over the whole dynamic range. The associated average PAE is 30% over a 5-dB average output power range, which is almost compliant with the target efficiency performance and substantiates the hypotheses of thermal effects coming into play in the CW characterization.

The achieved performance is compared to the state of the art in Table I. The designed DPA covers the full 17.3–20.3 GHz while complying with almost all the requirements in terms of output power, gain, and PAE. The GaN-SiC DPAs have slightly better peak performance at saturation, thanks to the better thermal properties of the substrate with respect to pure Si, but the back-off performance is comparable. On the other hand, the advantage offered by DPAs in back-off compared to class-AB PAs is evident. The comparison in terms of NPR is particularly difficult, given that many factors affect the linearity including, but not limited to, the bandwidth and the statistical distribution of the modulated signal [15]. The DPA has excellent linearity with 100-MHz signals, but conclusive tests will require wider modulation bandwidths and Gaussian distribution to achieve the PAPR required by SatCom.

IV. CONCLUSION

This letter has presented the design strategy and experimental characterization of a GaN MMIC DPA with high gain and high intrinsic linearity. The target application is that of satellite downlink in *Ka*-band, where additional linearization is impractical and often unfeasible. The DPA design is based on AM/PM minimization, which is successfully maintained within $\pm 12^{\circ}$ over the whole dynamic range and frequency band while delivering the target power of 36 dBm and demonstrating successful back-off efficiency enhancement. This challenges the current state of the art for similar applications. The system level characterization with a uniform white noise signal having 100-MHz instantaneous bandwidth confirms the effectiveness of the design, demonstrating NPR higher than 25 dB and associated PAE of 30%. These results allow consideration to adopt modulations with higher PAPR and wider bandwidth than the current one, which represents the main challenge in SatCom applications, where PAs are typically loaded with full-band modulated signals.

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