Navigating Challenges in Doherty Power Amplifier Design for Millimeter-Wave Frequencies

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Anna Piacibello[#1], Vittorio Camarchia[#2]
[#]Department of Electronics and Telecommunications (DET), Politecnico di Torino, ITALY
{[1]anna.piacibello, [2]vittorio.camarchia}@polito.it

***Abstract*— The paper addresses some of the challenges associated with implementing multi-stage Doherty power amplifiers at millimeter waves. The routing of the bias lines is analyzed for several configurations, including two-way and three-way, highlighting how it can impact performance in the presence of significant crosstalk between the metal layers in integrated technologies. Additionally, the paper discusses and provides a quantitative estimate of the Doherty gain penalty with respect to corporate amplifier configurations, a factor that may hinder the adoption of this architecture at millimeter waves and that calls for a careful trade-off between intrinsic technology gain and number of driver stages.**

***Keywords*— crosstalk, Doherty, gain, millimeter-wave systems, power amplifier, wireless communications.**

I. Introduction

Present wireless communication systems, whether ground-based [1], [2] or space-based [3], are experiencing a notable evolution towards millimeter-wave and beyond. This transition is driven by the ever-growing demand for capacity and the congestion observed in traditional sub-6 GHz bands. This evolution is deeply affecting the architecture of all transmitter building blocks, with a particularly significant impact on power amplifier design. At the technological level, the availability of robust processes with high gain at device level are crucial enabling factors. For non-constant envelope modulation schemes, the popular Doherty PA (DPA) architecture [4] faces challenges, especially for wide bandwidth and high gain requirements, that further complicate routing and necessitate precise control of crosstalk, also in consideration of the intrinsic necessity of DPAs of asymmetric bias conditions ultimately increasing the necessity of specific bias lines.

In this work we focus on the challenges related to the implementation of high-gain DPAs (both two- and three-way) requiring multi-stage architectures and accurate planning and implementation of the many bias lines routing typical of DPAs, with increasing impact on the performance of the amplifier as the operating frequency increases [5], [6].

II. Bias Lines Routing and Crosstalk in MMIC PAs

When designing MMIC DPAs that allow for on-wafer testing, the DC as well as the RF paths need to be routed to the boundaries of the chip. Typically, RF pads are located east-west and the DC ones north-south, although this is not the only option. While it is simple enough to provide north-south DC routing for corporate amplifiers, where all transistors in the same position along the amplifying chain share the same bias voltage, it can be more complex for DPAs, where in principle any transistor can have a different bias.

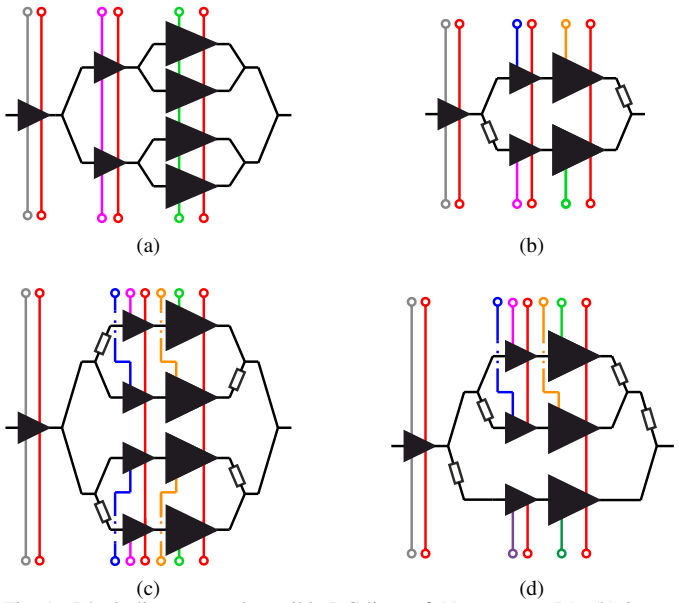


Fig. 1. Block diagrams and possible DC lines of (a) corporate PA, (b) 2-way DPA, (c) parallel-combined DPAs and (d) 3-way DPA.

A key difference exists between two-way single DPAs and N-way or parallel-combined DPAs. The former category does not suffer in principle from any DC routing limitation, because there are only two amplifying chains (a north one and a south one). The latter instead has three or more amplifying chains, which implies that at least one of them will not be along a chip edge, thus calling for air bridges or crossing to route its DC lines to the edges in a planar integrated technology.

This is illustrated by the block diagrams of Fig. 1, which considers a possible 3-stage architecture for each category and highlights the number of different bias lines. Note that, for simplicity, the drain supply (red) is considered common to all transistors, which is often the case although not strictly mandatory. The sample DPA architectures assume a driver stage embedded in the Doherty structure and an extra driver outside of it. While embedding one driver stage in the DPA is a rather common choice when the gain of the power stage is limited, several other variants exist for which the DC routing would be slightly different.

The availability of few metal levels in most III-V MMIC technologies makes crosstalk a critical issue, especially as the frequency increases. Two sample technologies are compared in this respect, namely the D01GH (100 nm GaN/Si HEMT, T1) from Ommic (now MACOM ESC) and NP15 from Win Semiconductors (150 nm GaN/SiC HEMT, T2). Fig. 2 reports the crosstalk ($|S_{31}|$) and the insertion loss ($|S_{21}|$) in a structure composed of two microstrip lines (where the one between ports 3 and 4 is a DC line which bridges under the main RF line connecting ports 1 and 2) crossing each other by means of an air bridge structure. An analogous structure is analyzed for the two sample technologies, considering three different widths of the RF line while keeping the DC line width (20 µm) unchanged. Note that, as shown in Fig. 2(a), to comply with the layout rules, when the width of the RF line increases it is necessary to split the air bridge into several parallel paths.

It stands out that losses in the GaN/Si technology are higher than in the GaN/SiC one, while also having a stronger dependence on the line width. For instance, at 20 GHz, the $|S_{21}|$ of T1 varies between -0.1 dB and -0.3 dB, whereas it is limited to -0.05 dB for T2. However, the main aspect affecting the routing is the amount of unwanted coupling between the RF and the DC line. Besides increasing with frequency, as expected, the $|S_{31}|$ is roughly 10 dB higher at all frequency for T1 compared to T2. This immediately reflects in an impact on the MMIC layout planning and possibly on performance, unless adequately addressed.

If the presence of RF and DC lines crossings cannot be avoided, T1 will be less suited to high frequency designs than T2 despite its lower gate length. Two MMIC PAs designed in these two technologies and presenting analogous DC routing challenges are analyzed. The T1 MMIC is a parallel-combined DPA for Ka-band satellite applications (17.3–20.3 GHz) [5]. The T2 MMIC is a 3-way DPA for 5G FR2 applications at 28 GHz [7]. Fig. 3 reports the MMIC photographs and the corresponding DC routing scheme.

Fig. 2 evidences that the crosstalk for T1 MMIC is more critical than for T2 MMIC, despite the lower operating frequency. In fact, a crosstalk always lower than -24 dB has been verified to have no significant impact on in-band performance for T2 MMIC. This simplifies the routing planning and alleviates the need for additional fine-tuning of the matching networks after the layout has been defined. However, the possible impact of the crosstalk on high-frequency stability should still be considered during the design. On the contrary, the in-band performance as well as the stability of T1 MMIC are affected by the routing of its DC lines. Fig. 4 shows the simulated small and large signal performance without and with the effect of the crosstalk between the RF and the DC lines, around the band of interest. The comparison demonstrates that the crosstalk present in the air bridge structures, although foreseen since the early stages of the layout, has an impact on the in-band performance of the DPA. In particular, it affects the gain flatness and the phase alignment of the branch signals, thus impacting on the efficiency and saturated power too. Optimizing the

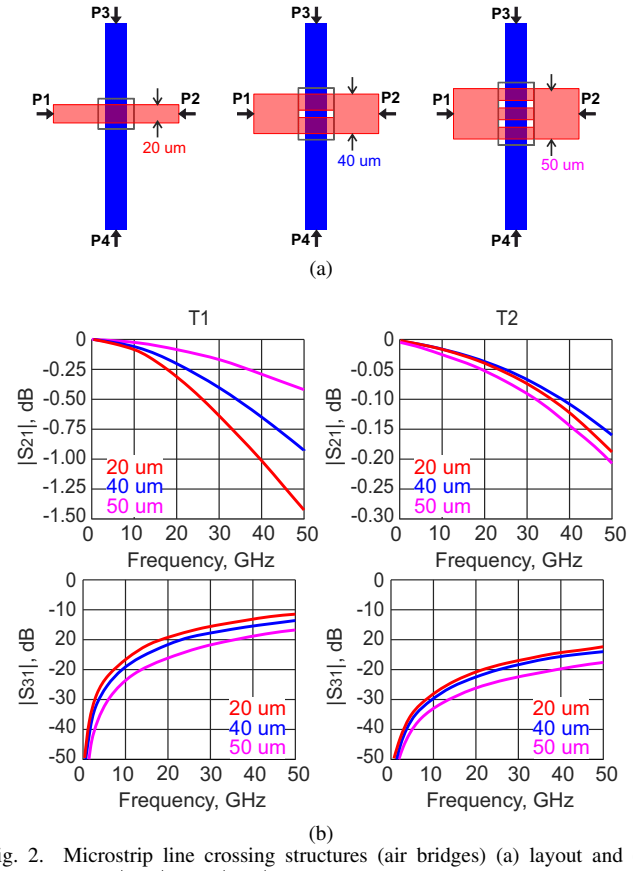
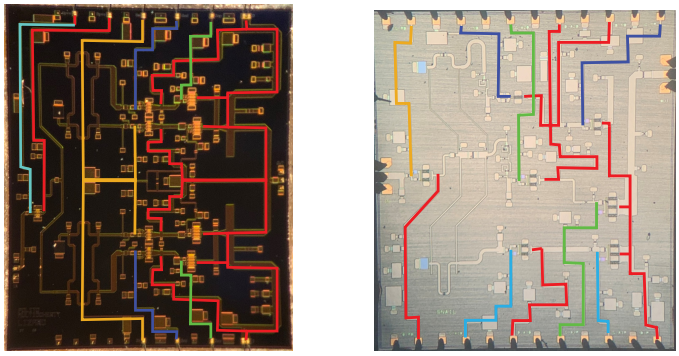


Fig. 2. Microstrip line crossing structures (air bridges) (a) layout and (b) corresponding $|S_{21}|$ and $|S_{31}|$ for different widths in the two analysed technologies (T1 left, T2 right).



(a) (b)

Fig. 3. Photographs of (a) T1 and T2 MMIC (b) with DC routing highlighted.

performance under these conditions is complicated, due to the fact that the impedance presented by the DC line at the crossing point in the 17.3–20.3 GHz range is difficult to control and hardly predictable before the final layout has taken shape, especially over a wide bandwidth.

III. The DPA Gain Issue

Reaching watt-level output powers requires the adoption of monolithic microwave integrated circuit (MMIC) based on compound semiconductors such as GaAs and GaN, featuring gate lengths smaller than 150 nm. However, the gain of

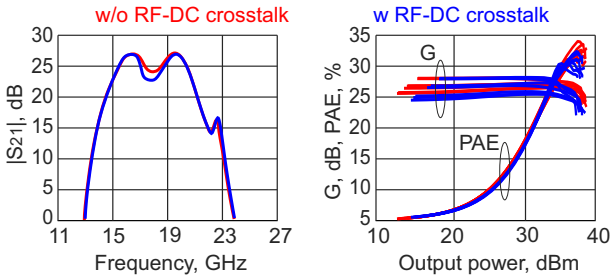


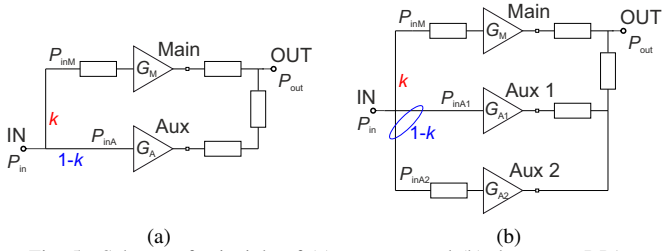
Fig. 4. Simulated effect of the crosstalk between the RF and the DC lines on the small (left) and large (right) signal performance of the T1 MMIC.

individual devices alone cannot ensure the amplification required to the entire amplifier, thus making multi-stage architectures imperative.

This challenge increases as frequencies move towards the millimeter-wave range, and particularly impacts on the Doherty architecture (and its derivatives) due to its inherent additional gain penalty compared to corporate amplifiers. This is due to the fact that Auxiliary stage(s) are typically biased in class C, and not only it compels to cascade multiple stages to attain the requisite amplifier gain, but it also deeply affects other vital performance metrics such as power-added efficiency (PAE). While this challenge already poses a significant constraint for symmetric two-way Doherty configurations, it drastically increases its importance for asymmetric or multi-way topologies, potentially hampering the effective utilization of the architecture altogether. Indeed, the inherent 3 dB gain penalty of a symmetric splitter can increase to levels exceeding 10 dB in three-way stages, especially if deep Output Power Back-off (OBO) is required.

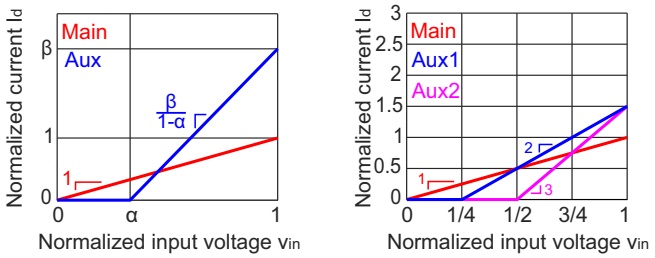
To quantify the impact of this issue, the small signal gain of the topologies of Fig. 5 is computed under some simplifying assumptions. In particular, the drain current profiles assumed for the computation, which are shown in Fig. 6, are derived according to the class-B bias point approximation, and their validity is then extended to the case where the Main stage has a non-zero linear gain G_{M}, which is strictly speaking inconsistent but can be considered acceptable as a rough estimation to guide the design choices, as demonstrated by many DPA designs [8]–[11].

The input splitter is considered lossless, hence in general $P_{\mathrm{in}} = P_{\mathrm{in,M}} + P_{\mathrm{in,A}_1} + \cdots + P_{\mathrm{in,A}_N}$. The small signal gain of the DPA is computed assuming that the Main is the only



(a) (b)

Fig. 5. Scheme of principle of (a) two-way and (b) three-way DPAs.



(a) (b)

Fig. 6. Drain current profiles for (a) 2-way DPAs designed for N-dB OBO, and (b) 3-way DPA designed for 6- and 12-dB OBO.

stage that is on:

$$G_{\mathrm{DPA}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{G_{\mathrm{M}} P_{\mathrm{in,M}}}{P_{\mathrm{in}}} = \frac{G_{\mathrm{M}}}{k}, \tag{1}$$

where $k = P_{\mathrm{in,M}}/P_{\mathrm{in}}$ is the input splitting ratio relative to the Main branch, and consequently $(1-k) = \sum_i P_{\mathrm{in,A}_i}/P_{\mathrm{in}}$.

A. *N-dB two-way DPA*

The current profiles that allow a DPA to achieve maximum efficiency at N dB OBO as well as at maximum power are the ones shown in Fig. 6(a). In this case, the turn-on point of the Auxiliary α can be related to the OBO as $N = 10\log_{10}\alpha^2$. In turn, the maximum currents ratio is $\beta = (1/\alpha) - 1$. The slope of the currents on the $(v_{\mathrm{in}}, I_{\mathrm{d}})$ plane are related to the devices' transconductance and to the input power splitting ratio as follows:

$$\frac{\Delta I_{\mathrm{d_{M,A}}}}{\Delta v_{\mathrm{in}}} = \frac{\Delta I_{\mathrm{d}}}{\Delta v_{\mathrm{gs_{M,A}}}} \cdot \frac{\Delta v_{\mathrm{gs_{M,A}}}}{\Delta v_{\mathrm{in}}} = g_{\mathrm{m_{M,A}}} \cdot \sqrt{\frac{\Delta P_{\mathrm{in_{M,A}}}}{\Delta v_{\mathrm{in}}}} \tag{2}$$

$$\text{where} \quad \frac{\Delta P_{\mathrm{in_{M,A}}}}{\Delta P_{\mathrm{in}}} = \begin{cases} k & \text{for M} \\ 1-k & \text{for A.} \end{cases} \tag{3}$$

Since both axes are normalized, $\Delta I_{\mathrm{d_M}}/\Delta v_{\mathrm{in}}$ is always equal to 1, whereas $\Delta I_{\mathrm{d_A}}/\Delta v_{\mathrm{in}} = \beta/(1-\alpha)$. Accounting for the assumption that $g_{\mathrm{m_M}} = g_{\mathrm{m_A}}$ leads to

$$k = \frac{(1-\alpha)^2}{\beta^2 + (1-\alpha)^2}. \tag{4}$$

Fig. 7 plots the gain penalty $K = 10\log_{10} k$ as a function of N. It is apparent that, as N increases, the ratio between Auxiliary and Main drain currents becomes higher and the input splitter becomes increasingly asymmetric, further increasing the DPA gain penalty K. It is interesting to note that K is almost equal, although not strictly identical, to N. In particular, the gain penalty for a 6-dB DPA ($\alpha = 1/2$) is of 7 dB, for a 9.6-dB DPA ($\alpha = 1/3$) is of 10 dB, and it becomes 12 dB for a 12-dB DPA ($\alpha = 1/4$). In fact, it is not common for these deep-OBO architectures to under-utilize the Auxiliary stages to achieve the desired current profile, since the periphery ratio is already quite large even when all stages are fully utilized.

For the most common case of a 6-dB two-way DPA, a different way of synthesizing the same response exists,

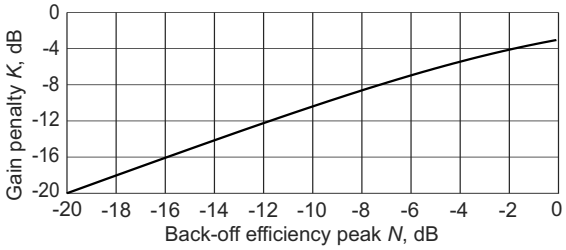


Fig. 7. Gain penalty K of an N-dB two-way DPA.

namely adopting a symmetric (i.e., even, $k = 1/2$) input splitter and doubling the Auxiliary active periphery. In this way, the Auxiliary presents an equivalent transconductance that is double than the Main and can therefore achieve the same maximum current in half of the input voltage dynamics. The advantage of this approach is that the gain penalty reduces to 3 dB, at the price of under-utilizing the Auxiliary device, whose periphery is only half exploited.

There are other techniques to mitigate the gain penalty issue, which in fact would be even more severe if one accounted for the class-C bias point of the Auxiliary [12] in a precise way. One of these is the adoption of a higher supply voltage for the Auxiliary [13]. In the case drivers are embedded in the DPA architecture, which is often the case especially for applications beyond 6 GHz [14], these often allow to achieve the desired modulation with a reduced asymmetry in the input power splitter, while also enhancing the PAE.

B. 6-12-dB three-way DPA

Three-way DPAs are in general even more critical under the gain penalty aspect. On the other side, they theoretically allow to reduce the efficiency drop over a wide back-off range, which can make them appealing despite the implementation difficulties. In this case, the current profiles to be synthesized depend on the type of combiner.

For the combiner of [7], targeting two efficiency peaks at 6 dB and 12 dB OBO, the reference current profiles are those of Fig. 6b. The required input power splitting can be derived to be $k = 1/14$ by extending the formulation of (2),(3) that holds for two-way DPAs. The remaining $1-k = 13/14$ is split unevenly between the two Auxiliaries, in such a way that $P_{\mathrm{in_{A2}}}/P_{\mathrm{in_{A1}}} = 9/4$, to allow them to achieve the same maximum currents in different dynamic sub-ranges. It follows that $G_{\mathrm{DPA}} = G_{\mathrm{M}}/14$, corresponding to a small signal gain reduction of 11.5 dB for the overall DPA.

IV. Conclusion

In this paper we have presented and discussed the impact of DC lines routing, crosstalk and small signal gain reduction on the design of multi-stage Doherty power amplifiers. Transitioning towards very high frequencies necessitates accompanying the implementation of the DPA architecture, particularly for deep OBO, with technologies that offer adequate gains. This enhances the feasibility of this architecture beyond its current frequency limitations, maintaining a manageable number of stages and minimizing the efficiency drop.

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References

[1] X. Wang, L. Kong, F. Kong, *et al.*, "Millimeter Wave Communication: A Comprehensive Survey," *IEEE Commun. Surveys Tuts.*, vol. 20, no. 3, pp. 1616–1653, 2018. DOI: 10.1109/COMST.2018.2844322.

[2] R. Lombardi, "Millimeter-wave technology and research trends for 5G Access and Wireless Transmission applications An industry view," in *2019 13th European Conference on Antennas and Propagation (EuCAP)*, 2019, pp. 1–1.

[3] R. Giofrè, A. Piacibello, P. Colantonio, and V. Camarchia, "Gallium Nitride Power Amplifiers for Ka-Band Satcom Applications: Requirements, Trends, and the Way Forward," *IEEE Microw. Mag.*, vol. 24, no. 12, pp. 74–86, 2023. DOI: 10.1109/MMM.2023.3314321.

[4] A. Grebennikov and S. Bulja, "High-Efficiency Doherty Power Amplifiers: Historical Aspect and Modern Trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190 –3219, 2012, ISSN: 0018-9219. DOI: 10.1109/JPROC.2012.2211091.

[5] A. Piacibello, R. Giofrè, R. Quaglia, *et al.*, "A 5-W GaN Doherty Amplifier for Ka-Band Satellite Downlink With 4-GHz Bandwidth and 17-dB NPR," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 8, pp. 964–967, 2022. DOI: 10.1109/LMWC.2022.3160227.

[6] C. Ramella, V. Camarchia, A. Piacibello, M. Pirola, and R. Quaglia, "Watt-Level 21–25-GHz Integrated Doherty Power Amplifier in GaAs Technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 5, pp. 505–508, 2021. DOI: 10.1109/LMWC.2021.3069555.

[7] A. Piacibello, V. Camarchia, P. Colantonio, and R. Giofrè, "3-Way Doherty Power Amplifiers: Design Guidelines and MMIC Implementation at 28 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 5, pp. 2016–2028, 2022. DOI: 10.1109/TMTT.2022.3225316.

[8] N. Srirattana, A. Raghavan, D. Heo, P. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 3, pp. 852–860, 2005. DOI: 10.1109/TMTT.2004.842505.

[9] A. Barthwal, K. Rawat, and S. K. Koul, "A Design Strategy for Bandwidth Enhancement in Three-Stage Doherty Power Amplifier With Extended Dynamic Range," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1024–1033, 2018. DOI: 10.1109/TMTT.2017.2751044.

[10] H. Lyu, Y. Cao, and K. Chen, "Linearity-Enhanced Quasi-Balanced Doherty Power Amplifier With Mismatch Resilience Through Series/Parallel Reconfiguration for Massive MIMO," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 4, pp. 2319–2335, 2021. DOI: 10.1109/TMTT.2021.3056488.

[11] A. Piacibello, P. Colantonio, R. Giofrè, and V. Camarchia, "A 3-Way GaN Doherty Power Amplifier for 28 GHz 5G FR2 Operation," in *2023 IEEE MTT-S International Microwave Symposium Digest*, 2023, pp. 327–330. DOI: 10.1109/IMS37964.2023.10187996.

[12] P. Colantonio, F. Giannini, and E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers* (Microwave and Optical Engineering). John Wiley & Sons, 2009, ISBN: 9780470746554.

[13] Y. Xu, J. Pang, X. Wang, and A. Zhu, "Enhancing Bandwidth and Back-Off Range of Doherty Power Amplifier With Modified Load Modulation Network," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 4, pp. 2291–2303, 2021. DOI: 10.1109/TMTT.2021.3056402.

[14] A. Alt and J. Lees, "Improving efficiency, linearity and linearisability of an asymmetric doherty power amplifier by modulating the peaking Amplifier's supply voltage," in *2017 47th European Microwave Conference (EuMC)*, 2017, pp. 464–467. DOI: 10.23919/EuMC.2017.8230890.