Summary

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The design and experimental test results for two monolithic CMOS radiation sensor prototypes developed for sub-nanosecond time resolution applications in high-energy physics experiments are presented. The prototypes were fabricated using LFoundry's 110 nm commercial CIS process within two ARCADIA project engineering runs. ARCADIA is an INFN project aimed at developing novel CMOS radiation sensor platforms with full substrate depletion and various designs and active thicknesses ranging from 50 to 500 μm, targeting a wide range of applications, including X-rays, medical imaging, space satellites, and high-energy physics experiments. This work is conducted within the ALICE 3 Time of Flight working group, which is investigating new technology for the ALICE 3 upgrade of the ALICE experiment at CERN, planned for 2035. The upgrade considers the adoption of monolithic CMOS sensors in its 46 m^2 Time of Flight layers, requiring an RMS time resolution of 20 ps for hadron and electron identification, with spatial granularity below 1×1 mm^2.

Silicon sensors are the standard in track reconstruction and are increasingly considered for timing detectors due to their continuously improving timing performance. At present, the most widespread solution is using hybrid silicon detectors, with the sensor bump-bonded to the electronics channels. In silicon timing layers, Low Gain Avalanche Detectors (LGADs) based hybrid technologies are mostly adopted. In the monolithic approach, the sensor and the readout electronics are integrated into the same silicon wafer, offering advantages such as a lower material budget, reduced costs, and easier assembly. The ALICE experiment already employs Monolithic Active Pixel Sensors (MAPS) in its inner tracking system with excellent performance; however, state-of-the-art monolithic sensors currently do not meet the required timing performance on a large integration area. Recent studies at the University of Geneva demonstrated a 17 ps time resolution with a monolithic sensor fabricated in a custom process with SiGe HBT, but large-area detectors necessitate commercial processes.

The first prototype explores the timing capabilities of ARCADIA technology with a dedicated optimized sensor and front-end electronics design. Although results suggest that a time resolution with MIPs in the hundreds of picoseconds is feasible, achieving the target resolution is not possible. Thinner active substrates enable better sensor resolution but worsen jitter performance due to reduced charge collection from the smaller active volume. To address this problem, a second prototype was fabricated with a different design and an additional mask introducing a p-type implant under the pixel electrode, generating

low amplification of the signal charge in the sensor, thereby enabling better jitter performance with thinner sensors. To focus on the first critical stages, the electronics were reduced to a fast trans-impedance amplifier implemented on-pixel, with analog outputs buffered out-of-chip in the periphery. Experimental results showed that the Monolithic CMOS Avalanche Detector prototype achieves full substrate depletion and internal amplification as demonstrated with optical tests. There is good agreement between electronics test results and simulations, though the sensor gain is 3 to 5 times lower than expected, impacting jitter performance. Initial measurements with MIPs indicated a time resolution of 234 ps for the minimum sensor thickness of 48 μm. This performance was partly attributed to the reduced sensor gain and non-optimized biasing conditions. A new production using the same mask set, but with different gain configurations, is currently being tested. The ongoing activity aims to control process parameters and optimize pixel geometry and substrate for better weighting field uniformity of the sensor.