A Comparison of Spread Spectrum and Sigma Delta Modulations to Mitigate Conducted EMI in GaN-Based DC-DC Converters

# A Comparison of Spread Spectrum and Sigma Delta Modulations to Mitigate Conducted EMI in GaN-Based DC-DC Converters

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***Abstract*—GaN power transistors offer significant advantages with respect to Si ones, but introduce challenges in meeting EMC regulations due to their high switching frequencies. This paper compares two modulation schemes, Spread-Spectrum Modulation (SSM) and Sigma-Delta Modulation ($\Sigma\Delta$M), for reducing the conducted Electromagnetic Interference (EMI) delivered by GaN-based DC-DC converters. The study analyzes how these techniques impact converter performance and evaluates their effectiveness in reducing conducted EMI at low frequencies. The findings provide valuable insights for designers seeking the most effective strategy for EMI mitigation.**

***Index Terms*—EMI, Buck, Sigma-Delta, Spread-Spectrum**

## I. Introduction

Last-generation GaN power transistors have gained significant interest, particularly in automotive applications, due to their higher power-density, lower switching losses and better thermal performance compared to Si and SiC counterparts [1]. The high switching speed of GaN power transistors has led designers to adopt switching frequencies ranging from 100 kHz to 1 MHz [2]. However, this also results in higher conducted Electro Magnetic Interference (EMI) at low-frequency, meaning below a few MHz. Passive input EMI filters are typically placed at the input of DC-DC converters to meet the strict limits imposed by automotive EMC standards [3]. However, the weight and the volume of these filters are usually significant, thereby limiting the benefits of GaN technology [4].

To reduce the volume of EMI filters and fully leverage the advantages of GaN power transistors, EMI mitigation techniques effective at the source can be employed. Some techniques focus on controlling the switching transients of power transistors [5], however, they are mainly effective for frequencies higher than 10s MHz. To reduce conducted EMI at low frequencies, some propose alterations to the converter topology, such as by inserting an additional switching leg [6]–[8]. To avoid hardware modifications, alternative modulation strategies to traditional Pulse Width Modulation (PWM) can be adopted, as they can shape the frequency spectra of disturbance sources at low frequencies.

Among these techniques, the modulation of the switching frequency, also known as Spread-Spectrum Modulation (SSM), has been extensively used in DC-DC converters to reduce the delivered EMI [9]. The SSM is based on the spreading of energy around the harmonics of the switching waveforms, with the result of lowering the magnitude of peaks generated by PWM. Frequency modulation is mainly effective when the harmonics to be reduced are in the MHz range, as in case of GaN-based DC-DC converters, since large frequency deviation can be exploited [10], [11].

In addition to SSM, Sigma-Delta Modulation ($\Sigma\Delta$M) has garnered increasing interest [12], [13]. Compared to traditional PWM, a $\Sigma\Delta$ modulator offers a finer control over the output voltage level, which is particularly advantageous when high switching frequencies are adopted. Additionally, $\Sigma\Delta$ modulators naturally vary the switching frequency of their output signal, thus leading to a spread spectrum effect [13]. From an EMI perspective, [14] was one of the first to investigate the reduction of conducted EMI in $\Sigma\Delta$M modulated DC-DC converters, reporting a reduction of approximately 10 dB. More recently, [12], compared the spectrum of switching waveforms in case of PWM and $\Sigma\Delta$M. However, the studied frequency range only partially covers that mandated by automotive standards. Furthermore, no insight is provided on the effects of the modulation parameters on the conducted EMI and converter performance. To sum up, previous studies have not conducted a detailed analysis of the achievable EMI reduction in $\Sigma\Delta$M DC-DC converters, nor the impact of modulator parameters on converter performance and conducted EMI has been investigated. Moreover, no comparison has been performed between software-based techniques for EMI reduction, clearly highlighting advantages and disadvantages of each method.

The present paper provides a systematic comparison between two modulation schemes, namely SSM and $\Sigma\Delta$M, with particular regard to the conducted EMI mitigation in a GaN-based DC-DC converter. The comparison also includes

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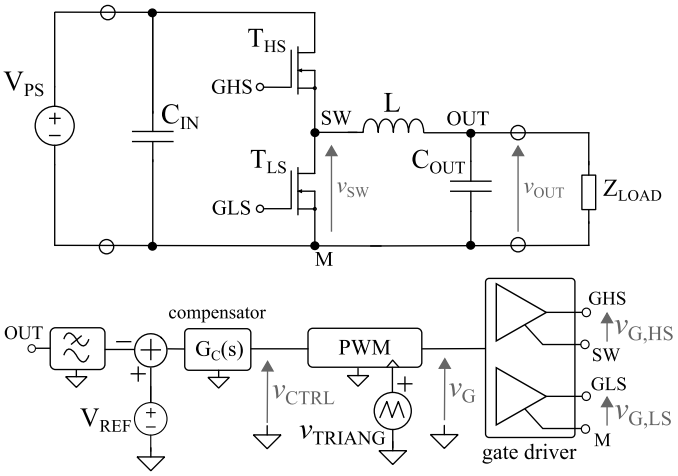


Fig. 1. Block diagram of a synchronous buck converter. The power stage is shown at the top, the controller at the bottom.

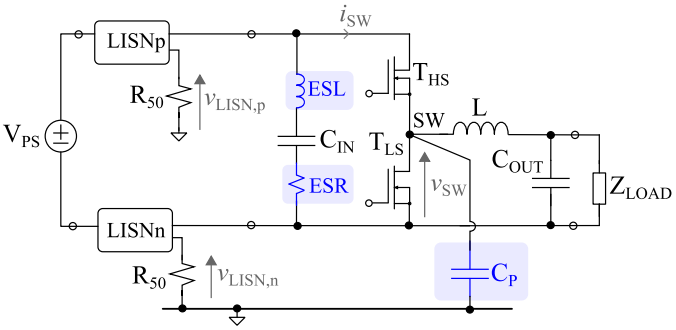


Fig. 2. Setup for measurement of conducted EMI delivered by the synchronous buck converter shown in Fig. 1. The main parasitic elements related to CM and DM disturbances have been enclosed in a box.

the effects of the two techniques on converter performance, providing valuable insights for designers to determine the most effective strategy.

This paper is organized as follows. The conducted EMI delivered by a buck converter are briefly recalled in Sect. II. The SSM and $\Sigma\Delta$ modulators are then introduced in Sect. III and IV, respectively. Sect. V reports the simulation results when these modulations are applied to the buck converter exploited as test-case. Concluding remarks are in Sect. VI.

## II. Conducted EMI of a Synchronous Buck Converter

The conducted EMI delivered by DC-DC converters can be discussed, without loss of generality, referring to a synchronous buck converter, as that shown in Fig. 1. The converter is comprised of two main blocks, i.e., the power stage and the controller. The DC input voltage to be regulated ($V_{\rm PS}$) is provided to a half-bridge consisting of a high-side ($T_{\rm HS}$) and a low-side ($T_{\rm LS}$) transistor. Such power switches are turned on and off in complementary fashion, causing the $v_{\rm SW}$ voltage to vary between $V_{\rm PS}$ and 0 V. The inductor $L$ and the output capacitor $C_{\rm OUT}$ are exploited as a second order low-pass filter to isolate the average value of $v_{\rm SW}$. Regarding the controller, a continuous-time architecture is shown in Fig. 1. The output voltage of the buck converter ($v_{\rm OUT}$) is typically attenuated, low-pass filtered, and subtracted from a reference voltage ($V_{\rm REF}$). The resulting error signal is fed to the compensator ($G_{\rm C}(s)$), which is designed to minimize the DC error and to provide the controller with a given bandwidth. The compensator output ($v_{\rm CTRL}$) is an analog signal proportional to the instantaneous duty cycle the voltage $v_{\rm SW}$ should have to regulate $V_{\rm PS}$ to the desired $V_{\rm OUT}$. The modulator, represented by the PWM block, compares $v_{\rm CTRL}$ with a triangular waveform ($v_{\rm TRIANG}$) with fixed frequency $f_{\rm sw}$, and outputs a PWM square wave ($v_{\rm G}$). By exploiting suitable gate driver and dead time insertion circuits, driving signals of the high-side and low-side power transistors ($v_{\rm G,HS-LS}$) are generated.

To assess the compliance of a such a DC-DC converter with EMC regulations, the setup shown in Fig. 2 is used. Two Line Impedance Stabilization Networks (LISNs) are placed between the input power supply and the Device Under Test (DUT), i.e., the buck converter shown in Fig. 1, as prescribed by the CISPR-25 standard [3]. The conducted disturbances are measured across the $R_{50}$ resistances, which model the input impedance of the measuring instrument. The conducted EMI can be analyzed by considering the Common Mode (CM) and Differential Mode (DM) disturbances separately. The former is defined as

$$v_{\rm LISN,CM}(t) \triangleq \frac{v_{\rm LISN,P}(t) + v_{\rm LISN,N}(t)}{2}, \qquad (1)$$

where $v_{\rm LISN,P}(t)$ and $v_{\rm LISN,N}(t)$ are the voltages across the measurement ports of the LISNs, and the latter as

$$v_{\rm LISN,DM}(t) \triangleq v_{\rm LISN,P}(t) - v_{\rm LISN,N}(t). \qquad (2)$$

The main parasitic elements responsible for the CM and DM conducted disturbances are highlighted in Fig. 2, and they are enclosed in a box to be found at a glance. More precisely, DM emissions are related to the equivalent series inductance (ESL) and resistance (ESR) of the input capacitors, modeled by $C_{\rm IN}$ in Fig. 2. ESL and ESR increase the equivalent impedance of the input capacitors at high frequencies, causing the switching current $i_{\rm SW}$ not to flow entirely through $C_{\rm IN}$. Regarding CM EMI, capacitance $C_{\rm P}$ models the coupling of the power devices to the heat-sink, which is typically ground-connected. Due to the high $dv/dt$ experienced by the SW node during the fast commutations of the power transistors, a CM current flows through $C_{\rm P}$ at every commutation of $v_{\rm SW}$ [15]. According to this simplified analysis, the primary source of CM (DM) EMI is identified as the switching voltage $v_{\rm SW}$ (switching current $i_{\rm SW}$).

With power transistors $T_{\rm LS}$ and $T_{\rm HS}$ driven by the PWM modulator shown in Fig. 1, the frequency spectra of $v_{\rm SW}$ and $i_{\rm SW}$ are characterized by prominent peaks at multiples of the switching frequency $f_{\rm SW}$. As a result, the energy of CM and DM conducted disturbances is concentrated/focused

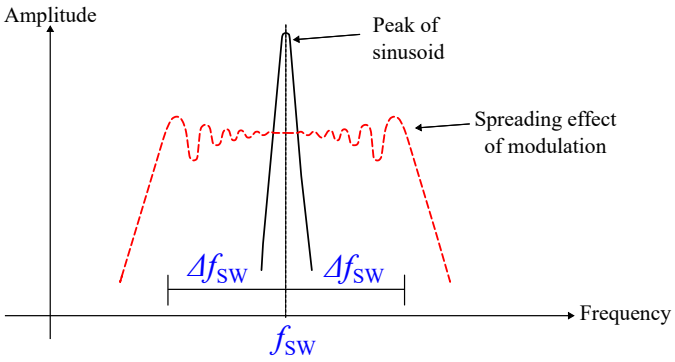


Fig. 3. When SSM is applied to a sinusoid, the energy associated to the fundamental frequency is spread over the Carson's bandwidth.

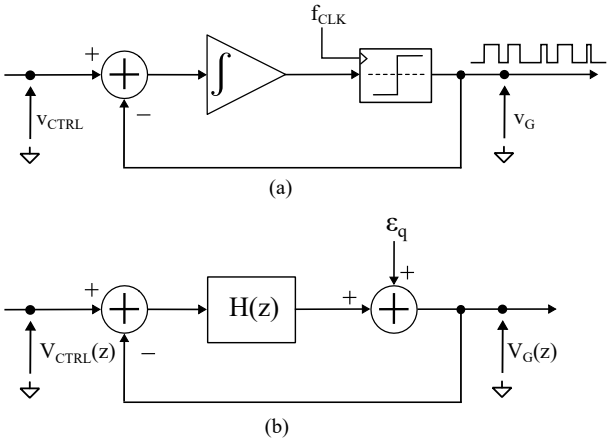


Fig. 4. Block diagram of (a) 1-bit Sigma-Delta modulator of the first order, and in (b) the corresponding linear model.

around the harmonics of $f_{\mathrm{SW}}$. Assuming $v_{\mathrm{SW}}$ and $i_{\mathrm{SW}}$ to be trapezoidal, the highest peak in their frequency spectra occurs at $f_{\mathrm{SW}}$. It is worth noting that in the case of GaN-based DC-DC converters, $f_{\mathrm{SW}}$ is typically higher than 150 kHz, meaning that the fundamental frequency falls within the regulated range. To reduce the magnitude of these peaks, which in turn determine the CM and DM conducted EMI levels, modulations different from standard PWM can be adopted.

## III. Spread-Spectrum Modulation

A solution adopted both in DC-DC converters and digital systems to reduce the magnitude of peaks at the harmonics is using Spread-Spectrum Modulation (SSM) instead of traditional PWM. Such a technique consists in introducing an intentional variation of the switching frequency $f_{\mathrm{SW}}(t)$, according to a specific modulation profile. Assuming a sinusoid at the switching frequency, the modulated signal can be written as

$$s(t) = A \cdot cos\left[2\pi f_{\mathrm{SW}} + 2\pi \cdot \int_0^t \Delta f_{\mathrm{SW}} \cdot \psi(\tau) d\tau\right] \quad (3)$$

where $A$ is the amplitude, $\Delta f_{\mathrm{SW}}$ is the peak deviation of the instantaneous frequency and $\psi(t)$ is the periodic modulating profile. The effect of the modulation is that of spreading the energy of the sinusoid in Carson's bandwidth, which is a range of frequencies defined as $[f_{\mathrm{SW}} - \Delta f_{\mathrm{SW}}, f_{\mathrm{SW}} + \Delta f_{\mathrm{SW}}]$, as shown in Fig. 3.

When SSM is applied to modulate the fundamental frequency of a trapezoidal signal, such as $i_{\mathrm{SW}}$ or $v_{\mathrm{SW}}$, it results in the spreading of each harmonic the signal is comprised of. More precisely, the energy of the $k^{th}$ harmonic is spread over a frequency band of $2k\Delta f_{\mathrm{SW}}$. The effective reduction of peak magnitude depends on the parameters of the modulation. Indeed, peak reduction increases with the frequency deviation ($\Delta f_{\mathrm{SW}}$). However, practical considerations limit the maximum frequency deviation that can be used in a DC-DC converter [10]. Moreover, if $\Delta f_{\mathrm{SW}}$ is too large, the sidebands of adjacent harmonics may overlap, thus reducing the SSM efficacy [11]. The modulation index parameter is defined as

$$m = \frac{\Delta f_{\mathrm{SW}}}{f_{\mathrm{m}}} \quad (4)$$

where $f_{\mathrm{m}}$ is the frequency of the modulation profile $\psi(t)$. Previous studies have shown that an optimal $m$ exists for each $\Delta f_{\mathrm{SW}}$, yielding the maximum peak reduction. Conversely, if the modulation becomes too fast or too slow, its efficacy decreases [10].

In order to implement SSM in the synchronous buck converter shown in Fig. 1, the fixed-frequency triangular generator ($v_{\mathrm{TRIANG}}$) can be replaced by one with instantaneous frequency varying according to $\psi(t)$. In such a way, all other blocks remain unchanged. Moreover, by choosing $\Delta f_{\mathrm{SW}} << f_{\mathrm{SW}}$, the average current ripple in the inductor $L$ is that of traditional PWM, meaning that the design of the power stage is not affected by SSM. Due to these considerations, periodic SSM can be effortlessly integrated into existing DC-DC converters, and it can provide both DM and CM EMI reduction. However, a critical aspect of using SSM is choosing the proper modulation parameters, i.e, $m$ and $\Delta f_{\mathrm{SW}}$, which otherwise may result in a negligible EMI reduction.

## IV. Sigma-Delta Modulation

Besides applying SSM to the PWM modulator shown in Fig. 1, the peaks at the $f_{\mathrm{SW}}$ harmonics of the switching waveforms $i_{\mathrm{SW}}$ and $v_{\mathrm{SW}}$ can be reduced by using a different strategy than pulse-width modulation. In the context of power converters, Sigma-Delta ($\Sigma\Delta$) modulators can be exploited as an alternative to PWM. A $\Sigma\Delta$M converts an analog signal into a Pulse Density Modulated (PDM) signal. This means that the $\Sigma\Delta$ output is a digital bitstream where the amplitude of the input signal determines the density of pulses. In a PDM bitstream, the pulse width is a multiple of the $\Sigma\Delta$ clock period, making the bitstream a frequency-modulated signal.

The block scheme of a 1-bit $\Sigma\Delta$ modulator is shown in Fig. 4(a). It is a feedback-based structure where the adder performs the difference between the input voltage $v_{\mathrm{CTRL}}$ at step $i$ and the output voltage $v_{\mathrm{G}}$ at step $i-1$. Such a difference is then fed to the integrator. Finally, the clocked comparator acts as a two levels quantizer, thus providing a bitstream at the output.

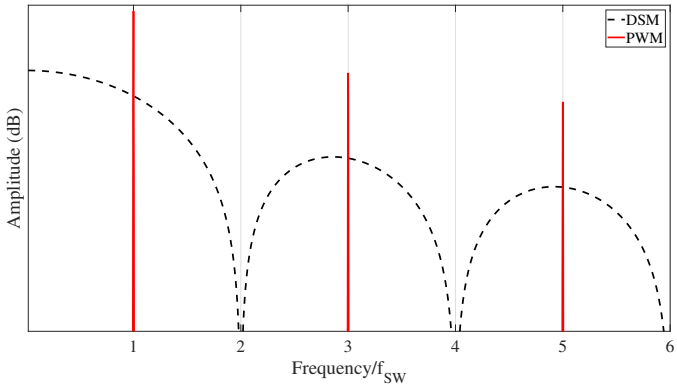


Fig. 5. STF of a ΣΔ modulator (dashed line) compared to the output spectrum of a PWM modulator (solid line). It is assumed that the modulator is clocked with a frequency $2f_{\mathrm{SW}}$.

The linearized model of the ΣΔ modulator (see Fig. 4(a)) is shown in Fig. 4(b), where $\varepsilon_{\mathrm{q}}$ is the quantization error introduced by the quantizer and $H(z)$ is the transfer function of the integrator. According to such a model, the modulator output can be written, in the time discrete domain $z$, as

$$V_{\mathrm{G}}(z) = STF(z)V_{\mathrm{CTRL}}(z) + NTF(z)\varepsilon_{\mathrm{q}}, \tag{5}$$

where the Signal Transfer Function (STF) is

$$STF(z) = \frac{H(z)}{1+H(z)} \tag{6}$$

and the Noise Transfer Function (NTF) is

$$NTF(z) = \frac{1}{1+H(z)}. \tag{7}$$

As far as $H(z)$ is concerned, for a first-order discrete-time integrator it is $H(z) = (z{-}1)^{-1}$, yielding a high-pass response of $NTF(z)$. This represents the fundamental property of a ΣΔ modulator, which is the noise-shaping, namely, the capability to move the quantization noise out of band.

The shape of the STF, which is shown in Fig. 5, suggests that the output spectrum is smooth, with no switching harmonics. Such a behavior can be exploited to reduce the EMI delivered by the converter in Fig. 1, by replacing the PWM block with a ΣΔ modulator. However, this change affects several figures of merit of the converter, e.g., stability and conversion efficiency. When the clock frequency of the comparator ($f_{\mathrm{CLK}}$) equals to the PWM switching frequency ($f_{\mathrm{SW}}$), the half-bridge control signal $v_{\mathrm{G}}$ generated by a ΣΔ modulator has fewer commutations than that generated by a PWM modulator, as the ΣΔ modulator holds the same output value for at least one clock period. This increases the converter efficiency by reducing the switching losses of power transistors, but also increases the current ripple of the power inductor. By setting $f_{\mathrm{CLK}} = k \cdot f_{\mathrm{SW}}$, where $k$ is an integer, previous studies have shown that ΣΔ and PWM modulators can achieve the same power conversion efficiency provided that $k \geq 2$ [16]. As far as the stability of the DC-DC converter is concerned, the phase margin decreases when employing a ΣΔ modulator because the STF in (6) includes a delay factor. Such a delay contributes a phase rotation of $360° \cdot f_{\mathrm{T}}/f_{\mathrm{CLK}}$, where $f_{\mathrm{T}}$ is the crossover frequency of the closed-loop converter [16].

TABLE I
BUCK CONVERTER PARAMETERS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_{\mathrm{PS}}$ | 48 V | L | 4.7 µH |
| $V_{\mathrm{OUT}}$ | 12 V | $C_{\mathrm{IN}}$ | 125 µF |
| $I_{\mathrm{OUT}}$ | 10 A | $C_{\mathrm{OUT}}$ | 375 µF |
| $T_{\mathrm{LS}}, T_{\mathrm{HS}}$ | [17] | $C_{\mathrm{p}}$ | 10 pF |
| $f_{\mathrm{SW}}$ | 400 kHz | $ESL$ | 28 pH |
| $\Delta v_{\mathrm{OUT}}/V_{\mathrm{OUT}}$ | $1.37{\cdot}10^{-3}$ | $ESR$ | 240 µΩ |
| $\Delta i_L/I_{\mathrm{OUT}}$ | 0.5 | | |

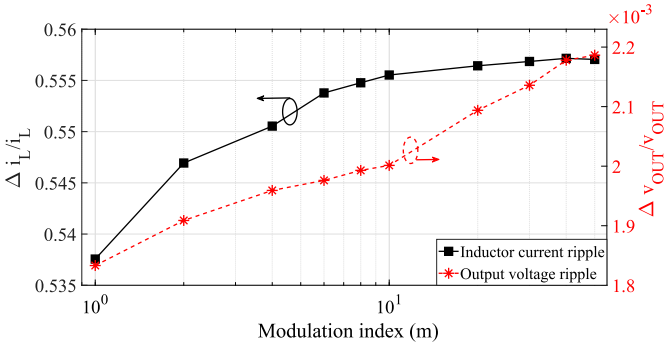


Fig. 6. Inductor current ripple normalized to nominal output current (star) and voltage output ripple normalized to nominal output voltage (square marker) in the case of SSM.

First order ΣΔ modulators are known to suffer from limit cycles. This phenomenon occurs when a constant voltage is present at the input of the modulator, resulting in a repeating pattern in the output bitstream. This leads to idle tones in the output frequency spectrum, worsening EMI performance. The magnitude of the tones can be reduced either by adding of a dither signal at the input of the quantizer or by increasing of the order of the modulator. The former solution introduces noise at the output of the converter, while the latter may worsen the stability of the modulator itself, leading to a more complex design procedure. In contrast, first-order modulators are always stable.

## V. CIRCUIT ANALYSIS

The synchronous buck converter shown in Fig. 1 has been used as case study to compare the aforementioned modulation schemes, i.e., PWM, SSM and ΣΔM. To this purpose, PWM, SSM and ΣΔM modulator blocks have been utilized with the same power stage and controller. The main parameters of the analyzed converter are listed in Table I for reference. Time-domain simulations have been carried out with Spectre [18], a SPICE-like simulator, to assess EMI reduction, converter efficiency, as well as voltage and current ripple for the various modulation schemes. As far as SSM is concerned, a fixed $\Delta f_{\mathrm{SW}} = 60\,\mathrm{kHz}$ was employed, and the modulation index

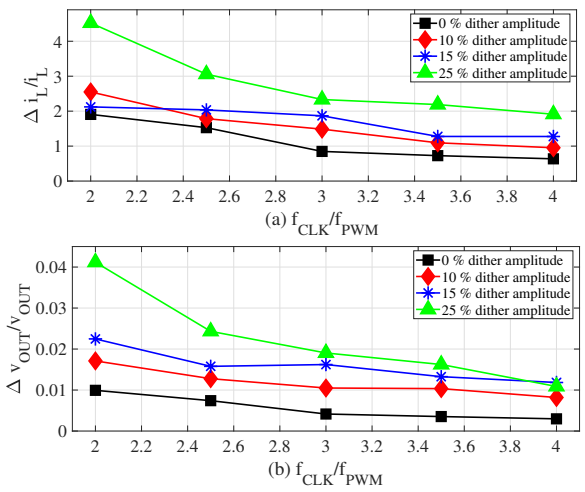


Fig. 7. Inductor current ripple normalized to nominal output current (at the top) and output voltage ripple normalized to nominal output voltage (at the bottom) in the case of ΣΔM.

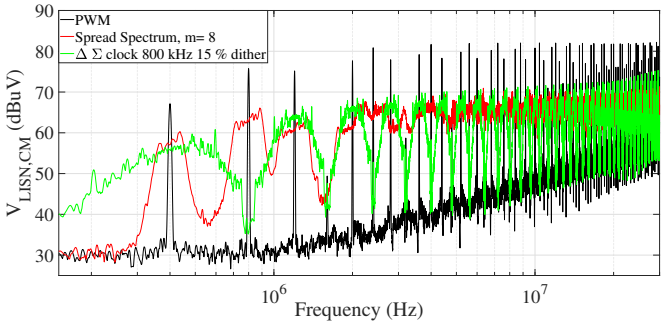


Fig. 8. Comparison of frequency spectrum of CM EMI between PWM, SSM with $m = 8$ and ΣΔM clocked at 800 kHz.

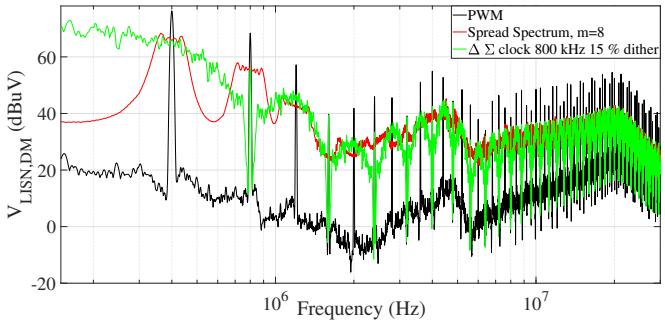


Fig. 9. Comparison of frequency spectrum of DM EMI between PWM, SSM with $m = 8$ and ΣΔM clocked at 800 kHz.

defined in (4) was varied between 1 and 50. Regarding the ΣΔ modulator, the clock frequency $f_{\mathrm{CLK}}$ was in the 0.8-1.6 MHz range, and different levels of the dither noise were investigated to address the issue of limit cycles.

The inductor current ripple ($\Delta i_{\mathrm{L}}$) normalized to the nominal output current ($I_{\mathrm{OUT}}$), and the output voltage ripple ($\Delta v_{\mathrm{OUT}}$) normalized to the nominal output voltage ($V_{\mathrm{OUT}}$), are shown in Fig. 6 for the SSM case. More precisely, $\Delta i_{\mathrm{L}}/I_{\mathrm{OUT}}$ is plotted on the left y-axis, while $\Delta v_{\mathrm{OUT}}/V_{\mathrm{OUT}}$ on the right y-axis. Comparing these normalized normalized ripples with those obtained using traditional PWM with fixed $f_{\mathrm{SW}}$, as detailed in Table I, the use of SSM results in a 10 % (50 %) increase of the inductor current (output voltage) ripple. Referring to the ΣΔM case, $\Delta i_{\mathrm{L}}/I_{\mathrm{OUT}}$ and $\Delta v_{\mathrm{OUT}}/V_{\mathrm{OUT}}$ are shown in Fig. 7 at the top and the bottom, respectively. The ΣΔ clock frequency was normalized to that of PWM, i.e., $f_{\mathrm{SW}}$=400 kHz. By increasing the clock frequency, voltage and current ripples reduce, as the average switching period decreases. Conversely, current and voltage ripples worsen when increasing the dither amplitude. Regarding the current ripple, a limit case is when $\Delta i_{\mathrm{L}} = I_{\mathrm{OUT}}$, meaning that the current in the inductor reaches 0 A. For such a reason, a maximum dither amplitude of 15 % (circle marker) of the reference signal $v_{\mathrm{CTRL}}$ was considered in what follows.

To assess the conducted EMI delivered by the converter when exploiting SSM, PWM and ΣΔ, the setup shown in Fig. 2 was employed. More precisely, the voltages across the LISNs measurement ports ($v_{\mathrm{LISN,P}}$ and $v_{\mathrm{LISN,N}}$) were analyzed to assess the CM and DM contribution according to (1) and (2). The resulting signals were processed using the virtual EMI receiver described in [19], which was configured with a 9 kHz resolution bandwidth (RBW) and peak detector, as prescribed by the standard [3]. The resulting frequency spectra in the 150 kHz-30 MHz range are shown in Fig. 8 and 9 for the CM and DM contribution, respectively. The spectra in case of SSM modulator refer to a modulation index ($m$) equal to 8, those in case of ΣΔ modulator to a 800 kHz clock frequency ($f_{\mathrm{CLK}}$) and 15 % dither amplitude. SSM and ΣΔ modulators exhibit comparable performances in reducing the magnitude of peaks, except when the nulls of the ΣΔ signal transfer function (see Fig. 5) align with some of the PWM peaks. In such cases, the ΣΔ modulator exhibits a significant reduction. However, despite the addition of dithering, idle tones remain visible in the EMI spectra, such as at 200 kHz and 600 kHz for the CM EMI in Fig. 8.

To further compare the two modulation techniques in terms of CM and DM EMI reduction, the Relative Amplitude (RA) was defined as

$$RA = \max_{[f_{\mathrm{sw}}-\Delta f, f_{\mathrm{sw}}+\Delta f]}(V_{\mathrm{LISN,CM,PWM}}) - \max_{[f_{\mathrm{sw}}-\Delta f, f_{\mathrm{sw}}+\Delta f]}(V_{\mathrm{LISN,CM,Mod}}) \tag{8}$$

which represents the difference between the peak of the PWM spectrum and the maximum EMI value achieved with an alternative modulator around $f_{\mathrm{SW}}$. Such a relative amplitude is shown in Fig. 10 for (a) the SSM and (b) ΣΔM cases, with a $\Delta f$=20 kHz. For SSM, the achievable reduction depends on the modulation index, with an optimal index $m$ of 8 resulting in an $RA$ of 9 dB for both CM (square) and DM (star markers). In contrast, ΣΔ modulator achieves an $RA$ of around $RA$=10 dB.

Finally, the conversion efficiency of the DC-DC converter was evaluated and reported in Table II for the considered

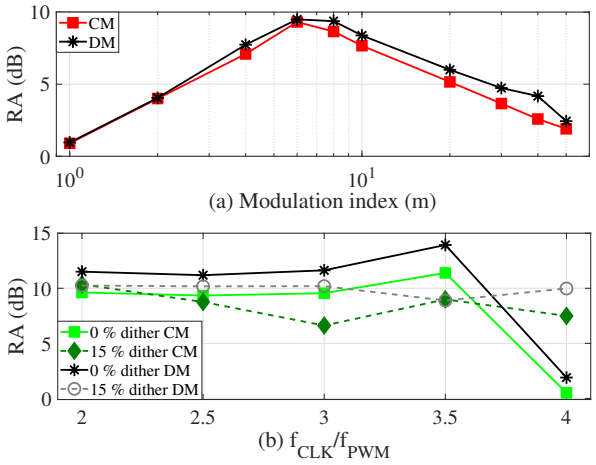


Fig. 10. Conducted EMI attenuation around 400 kHz when employing SSM (at the top) and ΣΔM (at the bottom) for CM (square) and DM (star) components.

TABLE II
EFFICIENCY COMPARISON

| Case study | Value | Case study | Value |
|---|---|---|---|
| PWM | 99.03 % | SS (m=8) | 99.03 % |
| ΣΔ 800 kHz, 0% dither | 99.21 % | ΣΔ 800 kHz, 15% dither | 98.99 % |
| ΣΔ 1.2 MHz, 0% dither | 99.17 % | ΣΔ 1.2 MHz, 15% dither | 98.98 % |
| ΣΔ 1.6 MHz, 0% dither | 99.06 % | ΣΔ 1.6 MHz, 15% dither | 98.92 % |

modulation schemes. The use of SSM does not impact the efficiency, while increasing the clock frequency in ΣΔ modulators moderately reduces the efficiency. This observation aligns with what discussed in Sect. IV, as switching losses increase with higher clock frequencies. Additionally, a minor decrease in efficiency is noted with the addition of dithering.

## VI. CONCLUSIONS

This work compares Spread Spectrum Modulation (SSM) and ΣΔ modulators applied to a DC-DC converter, focusing on their effectiveness in reducing conducted EMI at low frequency compared to traditional PWM modulators. Such an aspect is crucial in GaN-based power converters, which operate at switching frequencies above the lower bound of conducted EMI regulated range, i.e., 150 kHz. The study found that both SSM and ΣΔ modulators exhibit comparable performance in reducing CM and DM EMI reduction, achieving around 10 dB reduction with optimal parameter settings. However, the output voltage ripple with the ΣΔ modulator was approximately 10 times higher than that with SSM.The conversion efficiency was marginally affected by the choice of modulator. These findings underscore the importance of selecting appropriate modulator parameters to optimize EMI reduction. These insights are also relevant for power converters using transistors other than GaN, offering a means to reduce conducted EMI at the source by changing the type of modulator used in the controller.

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