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Integrated 5-W GaN Doherty Power Amplifier for 5G FR1 Bands with 19 dB Gain Over a 41% Bandwidth

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***Abstract* — This paper presents the design of a Doherty power amplifier for 5G applications in the FR1 5G bands, implemented with WIN's 150 nm GaN/SiC HEMT technology. The design aims to achieve real-case scenario performance for power and gain while covering the full N77 & N79 bands, which corresponds to a 41% bandwidth. This is accomplished by developing a two-stage design with an optimized combiner architecture. The fabricated chip achieves 37 dBm of saturated output power, 19 dB of linear gain and a minimum PAE of 20% over a 6 dB back-off range in the 3.3 GHz-5 GHz band, achieving state-of-the-art performance for a multi-stage Doherty architecture.**

***Keywords* — 5G, doherty power amplifier, GaN, MMIC, wideband.**

I. Introduction

The use of complex modulation schemes with non-constant envelopes and the adoption of a large number of antennas in multiple input/multiple output configurations typical of 5G architectures result in signals with a high peak-to-average power ratio (PAPR), thus requiring the power amplifier (PA) to operate at lower power levels with respect to saturation, specifically within a given back-off (OBO) range.

The Doherty power amplifier (DPA) [1] has become one of the most popular solutions for back-off efficiency enhancement thanks to the rather simple design. On the other hand, a distinctive feature of 5G systems is the wide modulation bandwidth, which requires high-performing PAs capable of covering multiple frequency bands [2]. This aspect is challenging for any PA, but becomes particularly critical for DPAs, where load modulation and phase alignment must be guaranteed in the full bandwidth [3].

Single-stage hybrid DPAs demonstrators with excellent bandwidths, even exceeding one octave, have been presented in the literature [4], [5], [6], [7], but they have limited gain. When moving to real scenarios, the required linear gain must exceed 15 dB and the multi-stage examples available present considerably narrower bandwidths [8], [9], [10].

In this work, we report the design and experimental characterization of a Monolithic Microwave Integrated Circuit (MMIC) GaN DPA for the 5G FR1 frequency bands N77 (3.3-4.2 GHz) and N79 (4.4-5 GHz) [11], falling in the small-cell power range (1-10) W for 5G base stations. Adapting a wideband design strategy from the literature [12] to extend its validity, the DPA achieves 37 dBm output power and 19 dB linear gain, while maintaining a power added efficiency (PAE) higher than 20% over a 6-dB OBO range from 3.3 GHz to 5 GHz.

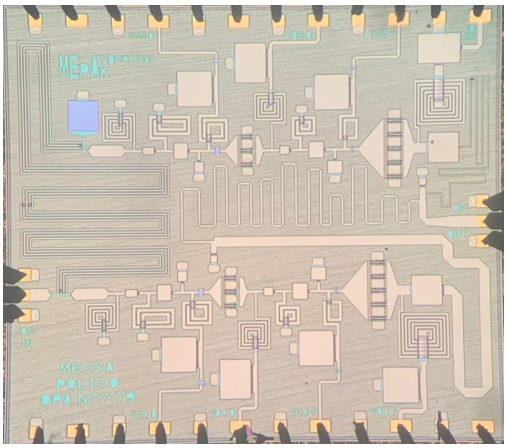


Fig. 1. Microscope photograph of the fabricated MMIC DPA ($3.7\times3.3\text{mm}^2$).

II. Design and implementation

The selected technology is the 150-nm gate length GaN/SiC HEMT process by WIN Semiconductors, which features around 4 W/mm at 28 V drain supply voltage and was at a pre-commercial development stage at the time the design was performed. The SiC substrate has superior thermal properties than its pure Si counterpart [13] and is beneficial in terms of achievable power density.

Fig. 2 shows the complete circuit schematic of the symmetric topology adopted, with identical transistor sizes for the Main and Auxiliary amplifiers and equal input power splitting. Its simplicity enables achieving a wideband design while limiting the chip size and minimizing losses. By using the same devices and matching networks (MNs) for the Main and Auxiliary branches the phase difference between the two branches is minimized, no further components must be introduced for phase compensation and the overall bandwidth is enhanced.

The target saturated output power (Psat) of 37 dBm is increased by 2 dB to account for the output combiner losses, resulting in 39 dBm of target output power for the final stage. Combining two $10\times100\,\mu$m devices in a symmetric Doherty configuration fulfils the required Psat without further power combination since each device can deliver 36 dBm of output power. Furthermore, the $10\times100\,\mu$m device has an intrinsic optimum load close to the target output impedance of $50\,\Omega$, which is beneficial for synthesising wideband matching networks due to the low impedance transformation ratio.

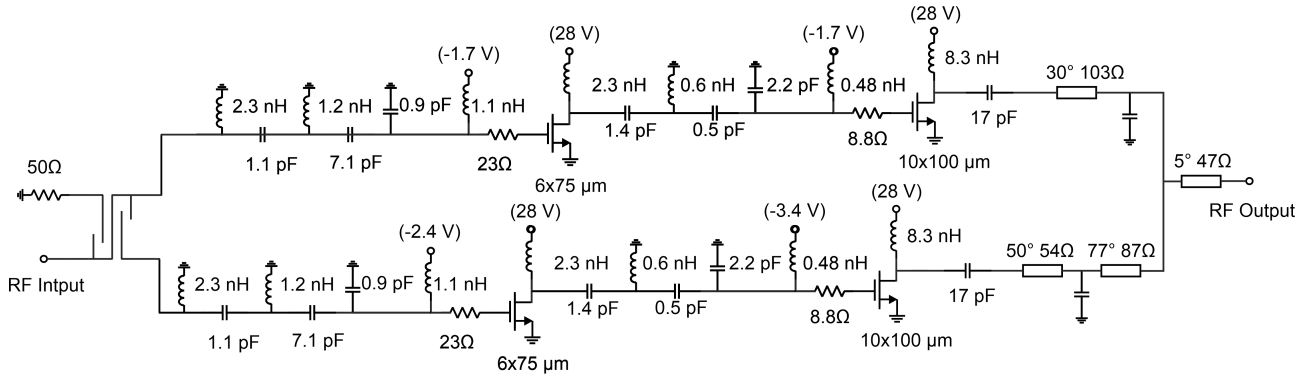


Fig. 2. Complete circuit schematic of the proposed symmetric MMIC DPA.

The small signal analysis of the device shows a gain of about 15 dB after stabilization, so a driver is inserted in the chain to meet the overall gain specification of about 20 dB and to compensate for Doherty's small signal 3 dB gain penalty [14]. In agreement with [15], a dual-driver topology with one driver for each branch of the DPA is chosen to maximize efficiency, even in the case of limited final stage gain. To limit the driver's compression and thus its impact on the linearity of the DPA, a 6×75 µm device is chosen for both branches, corresponding to a periphery ratio of roughly 1:2 with respect to the final stage.

The combiner is one of the limiting factors for the design of a wideband DPA due to the required $\lambda/4$ impedance inverter. This design applies for the first time to a two-stage architecture the combiner topology from [12], which was proved to achieve more than 80% of fractional bandwidth in a hybrid single-stage Doherty configuration. The combiner topology foresees a λ/4 impedance inverter on the Main branch and two λ/4 sections on the Auxiliary branch, with different characteristic impedances. Besides, despite the relatively low operating frequency compared to the process cutoff (f_{T} ≈32 GHz, $f_{\max}$ ≈187 GHz), the reactive parasitic effects of the transistors are non-negligible and need to be accounted for in the design. As in [12], the output parasitics are embedded in the combiner design by introducing a shunt capacitor after each branch's first λ/4 section and by increasing the characteristic impedance of the lines.

Although not explicitly discussed in [12], it is found that the design strategy is not always fully applicable. In fact, the desired wideband operation is only achieved when the load trajectory seen by the Main in back-off intercepts the real axis in two distinct points, corresponding to two separate frequencies in the target band. In this case, the shape of the back-off load trajectory over frequency shows a curled behaviour concentrated near the centre of the Smith Chart, as in Fig. 3 (a). This is accomplished by imposing that, at the lowest frequency, the back-off load has a positive imaginary part that is smaller than a limit value. Such value has to be defined for the specific design and will keep the load trajectory from spreading too far from the optimal impedance over frequency. As shown in Fig. 3(b), in our scenario, the back-off load at the lowest band limit would have an imaginary part that is rather high, corresponding to a spread-out load trajectory with the crossings of the real axis that are almost coincident. This would ultimately result in a narrower bandwidth.

A further limitation for the MMIC implementations is posed by the feasibility of the lines width when considering layout compactness and current handling limits. This constrains the characteristic impedance within a given range, which was identified as (10–90) Ω in this design. In fact, starting from the ideal combiner design of Fig. 3(b), the characteristic impedances of the lines must be increased to embed parasitic compensation, but the initial values are already close to the feasibility limit. To partially overcome these limitations, the original formulation was adapted and the target back-off and saturation loads were selected according to a trade-off between output power, efficiency and desired behaviour of the resulting trajectory over frequency. Despite these countermeasures, the achieved load modulation could not cover an 80% bandwidth. However, as shown in Fig. 3(c) (continuous line), the synthesized load trajectories allow to cover the target 40% bandwidth.

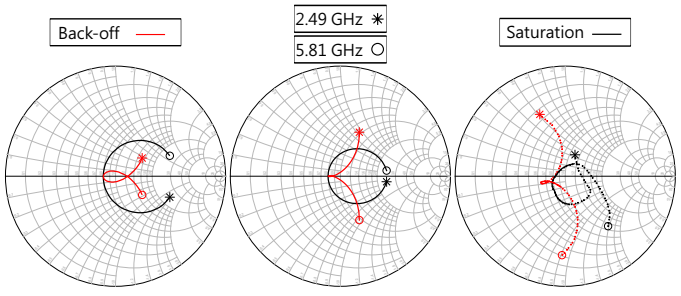


Fig. 3. Load trajectories presented to the Main in back-off (red) and at saturation (black) on a (2.49–5.81) GHz bandwidth: (a) ideal target in agreement with [12]; (b) present design with ideal lines; (c) synthesized by the final microstrip circuit. The optimum loads at back-off and saturation conditions, respectively, are used to normalise the Smith charts.

Once the combiner parameters are obtained, the layout is optimized with particular care for choosing the most compact solution, since the combiner represents the most bulky component of the DPA at sub-6 GHz frequencies. A

lumped implementation could certainly offer a more compact alternative, but it would prevent from effectively covering a 41% relative bandwidth with comparable performance. The resulting combiner implements a uniform load modulation for the Main, whose intrinsic load is modulated by a factor 1.6 over the whole bandwidth, close enough to the target load modulation factor 2 of an ideal 6 dB Doherty [16].

The complexity of the interstage and input MNs is then determined as a trade-off between chip size and bandwidth, considering the 40% bottleneck imposed by the combiner. A lumped topology based on LC sections is selected both at the interstage and input. While the lumped implementation has higher losses, these are limited by the relatively low order, and their effect impacts mainly on the gain, whereas the efficiency is only slightly reduced. Since the same MNs are adopted for both branches, the matching has to be optimized by considering the different impedances presented by the class-AB Main and the class-C Auxiliary devices.

The input power splitter is based on a Lange coupler designed on 50 Ω to divide the power evenly between the two branches while embedding the required 90° phase delay on the Main branch. The Lange coupler is chosen over a Wilkinson power divider and a branch line coupler thanks to its very wide bandwidth.

The bulky microstrip lines lead to a packed layout, and EM simulations are crucial to assess the performances and stability of the DPA. The overall circuit fits a compact chip size of $(3.7\times3.3)\,\mathrm{mm}^2$, and low-frequency decoupling capacitors are added off-chip on the DC lines to guarantee stability. The microscope photograph of the manufactured chip is shown in Fig. 1.

III. Experimental Characterization

The small signal characterization is performed at the nominal bias point: $V_{\mathrm{G,M}}$=-2 V, $V_{\mathrm{G,A}}$=-3 V, V_{DD}=28 V, I_{D}=36 mA. Fig. 4 shows a good agreement of the measured (symbols) and simulated (solid) scattering parameters over the (0-10) GHz frequency range. In the design bandwidth, the measurement results show an S_{11} and S_{22} lower than -15 dB and -5 dB, respectively. The minimum S_{21} is 19.2 dB, with a variation of less than 0.5 dB with respect to simulations and a gain variation of only 2 dB over the bandwidth. Overall, the bandwidth is maintained, with some margin especially at lower frequencies, no frequency shifts and good performance.

The continuous wave (CW) in-band power sweeps from 3.3 GHz to 5 GHz are shown in Fig. 5 with an optimized Main devices' bias point of -2.1 V. The 37 dBm saturated power requirement is satisfied for all frequencies, with a power variation over the bandwidth of 1.6 dBm. Saturated and 6 dB back-off PAE values are rather consistent across the band and remain higher than 25% and 20%, respectively, showing the effective efficiency enhancement behaviour of the circuit. The gain remains above 10 dB at saturation. With consistent outcomes across the bandwidth, the measured results track well with the simulated ones.

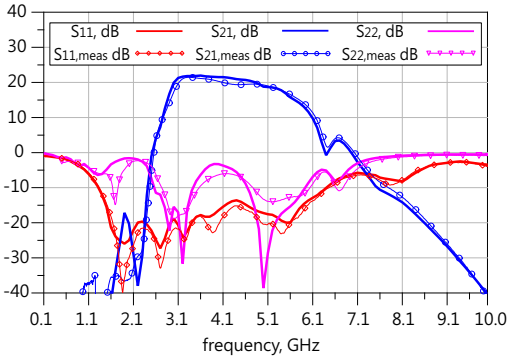
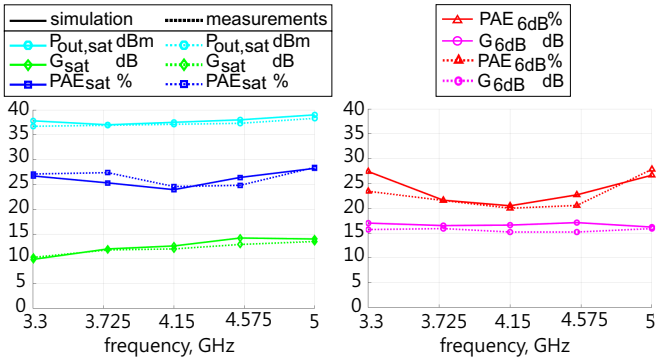


Fig. 4. Measured (symbols) and simulated (solid) small signal parameters.



(a) (b)

Fig. 5. Comparison of simulated (solid) and measured (dotted) CW performance at saturation (a) and at 6 dB OBO (b).

A system level characterization is also performed to evaluate the DPA's linearity, exploiting the digital signal synthesis features of a Keysight N5242B PNA-X. The adopted modulation is a 256-Quadrature Amplitude Modulation (QAM) with 50 MHz instantaneous bandwidth and 7.2 dB PAPR. The linearizability of the DPA is assessed by exploiting the direct digital predistortion (DPD) routine embedded in the PNA-X. Fig. 6 shows the output spectra of the 256-QAM 50 MHz signal at 4.15 GHz before and after DPD. With no DPD, the DPA delivers 33 dBm average output power with corresponding 23% efficiency and a good inherent linearity; with an adjacent channel power ratio (ACPR) lower than -32 dBc and an error vector magnitude (EVM) lower than 4.5%. After DPD, the average efficiency is increased to 24% while ACPR and EVM further improve to -46 dBc and 1.2%, respectively.

The achieved performances are compared to the state of the art of sub-6 GHz DPAs in Table 1. The designed DPA achieves the widest bandwidth among the two-stage architectures with comparable gain, while providing output power and back-off PAE that challenge the broadband single-stage hybrid demonstrators.

IV. Conclusion

This paper presented a GaN MMIC Doherty power amplifier in the FR1 band (3.3-5) GHz. The DPA achieves

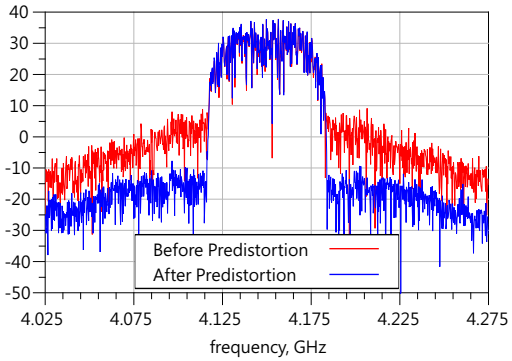


Fig. 6. Output power spectrum of a 256-QAM 50 MHz signal at 4.15 GHz. Performance before predistortion (red): average output power 33 dBm, average efficiency 23%, ACPR -32 dBc, EVM 4.5%. After predistortion (blue): average output power 33 dBm, average efficiency 24%, ACPR -46 dBc, EVM 1.2%.

Table 1. Comparison with state-of-the-art GaN DPAs for 6 dB OBO.

Ref.	Sub.	Freq. (GHz)	BW (%)	G_{SS} (dB)	P_{sat} (dBm)	$\mathrm{PAE}_{6\mathrm{dB}}$ (%)	Impl.
[4]	SiC	1.6-2.4	36	10	39	39	Hybr.
[5]	SiC	1.5-3.8	87	10	43	33	Hybr.
[6]	SiC	1.3-2.8	73	8	42	35	Hybr.
[7]	SiC	2.1-3.1	38	10	42	46	Hybr.
[8]	SiC	2.14	–	19.6	41	40	MMIC
[9]	SiC	4.4-5.1	15	17.5	41	40	MMIC
[10]	Si	3.2-4.7	38	8	29	31	MMIC
T.W.	**SiC**	**3.3-5.0**	**41**	**19**	**37**	**20**	**MMIC**

real-case scenario performance for small-cell type 5G base stations with 37 dBm of saturated output power and 19 dB of small-signal gain, with uniform performance over the state-of-the-art bandwidth for a two-stage Doherty architecture. The PAE is above 25% and 20%, at saturation and 6 dB back-off, respectively, showing the effective efficiency enhancement behaviour of the circuit over the state-of-the-art 41% bandwidth.

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