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A GaN-Based MMIC Doherty Power Amplifier With Class F Peaking Branch

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***Abstract* — This paper presents a novel design approach to enhance the performance of the Peaking branch of a Doherty Power Amplifier (DPA), by properly manipulating its input harmonics through a suitable nonlinear driver stage. In particular, aiming to implement a Class F harmonic termination for the final stage, a third harmonic voltage component is injected at its input with a driver, so that the phase of the third harmonic current at the output of the final stage is reversed with respect to its normal evolution, allowing a Class F design strategy for a class C biased device. The design strategy is described together with the design and experimental characterization of a prototype for X-Band application. The DPA is realized on the 120 nm gate-length GaN-on-SiC technology available at WIN Semiconductors. The MMIC provides more than 36 dBm and 40% of output power and efficiency, respectively, at 10 GHz.**

***Keywords* — Doherty Amplifier, Gallium Nitride, High efficiency, Waveform engineering.**

I. Introduction

Current wireless communication systems exploit complex modulation schemes which involve signals with large Peak-to-Average-Power-Ratio (PAPR) to increase data transmission rate [1]. In order to manage signals with significantly time-varying envelope, different architectures of power amplifiers (PAs) have been used over the years, and the Doherty power amplifier (DPA), which exploits the load modulation concept, is one of the most interesting in terms of trade-off between achievable performance and complexity of the design [2].

A standard DPA is realized by properly combining a Carrier (or Main) device, typically biased in class AB, with a Peaking (or Auxiliary) one, biased in class C, exploiting the active load modulation concept of the latter onto the former over a predefined power range (OBO). However, the use of a class C bias for the Peaking device raises two main issues:

- a gain degradation due to both the power losses at its input and the inherently lower gain with respect to the Carrier device;
- a lower fundamental harmonic current component generated at the output, with respect to the Carrier device, which requires an uneven splitter to be properly addressed.

Having in mind the mechanisms at the bases of the current harmonics generation of an active device as a function of its conduction current angle [3], such drawbacks could be mitigated by adopting suitable waveform engineering approaches. Indeed, by squaring the input voltage waveform of a class C biased device, for instance by introducing a second harmonic component, it is still possible to synthesize a proper Class F harmonic termination at its output [4]. However, the introduction of a second harmonic leads to an input voltage waveform that is flattened on one side and has a peak on the other side, which could be close to the gate source breakdown voltage of the transistor.

In this work, we proposed an alternative approach, in which a Class F design strategy for the Peaking final stage is made possible by squaring its input voltage waveform through the injection of a third harmonic component provided by a nonlinear driver device, thus preventing any breakdown problems. The approach has been adopted to design a 2-way DPA with 6 dB of OBO in X-Band, by using the NP12 technology process of WIN Semiconductors (120 nm gate-length GaN-on-SiC). For the Carrier branch, a single stage Class F amplifier was considered. The good agreement between measurements and simulations has confirmed the validity of the proposed approach, with the prototype achieving good performance over the frequency range 9.6-10.4 GHz with a peak power of 36 dBm and an efficiency larger than 40% at 10 GHz.

II. Peaking Amplifier Design Strategy

The NP12 process operates with a drain bias voltage (V_{DD}) of 28 V, and shows a knee and pinch-off voltages of about 5 V and -2 V, respectively. The Peaking branch uses a 6x100 µm device in the final stage driven by a 2x100 µm. The latter periphery was selected to be compliant with the power level required to saturate the final stage while providing good efficiency levels. Both devices were made unconditionally stable through a classical lumped solution (R-L network in parallel and R//C in series to the gate). In particular, and differently with respect to the classical approach, the stability network of the final stage was optimized to not penalize the maximum achievable gain attainable in the third harmonic frequency range (i.e., 28.8 GHz to 31.2 GHz).

The final stage is biased in class C with $V_{GS} = -2.6\,V$ and its output matching network (OMN) was designed to guarantee the following behavior:

- to show, at the intrinsic current generator plane, the optimum Class F loading conditions, i.e., a short circuit at the second harmonic and, as close as possible, an open circuit at third harmonic;
- at fundamental frequency, to show the optimum resistive load of $R_{OPT} = 133\,\Omega$.

To identify the optimum input conditions for such a device, in order to properly generate the corresponding output out-of-phase current harmonic components (I_1 and I_3) to allow a Class F waveform shaping, the behaviour of the driver stage was firstly emulated by using a two-tone power source (at fundamental and third harmonic frequencies). The optimum ratio (≈ 0.1) and phase difference ($\approx 180°$) among the fundamental ($V_{G,1}$) and third ($V_{G,3}$) harmonic components of the gate voltages were identified. Then the power source was replaced with the driver stage. For its design, the active device was biased in class C with $V_{GS} = -3.2\,V$, also to keep the overall Peaking branch off in the low power region of the DPA, and the inter stage matching network (ISMN) was designed to:

- transform the final stage input impedance in the optimum load for the 2x100 µm device at fundamental frequency (i.e., $R_{OPT,D} = 550\,\Omega$);
- short circuit the second harmonic component;
- control the third harmonic impedance in order to provide the amplitude ratio and phase difference between $V_{G,1}$ and $V_{G,3}$ previously identified.

The double stage was finally matched to $50\,\Omega$ at the input synthesising a proper input matching network (IMN).

Fig. 1 shows the simulated load lines at the intrinsic current generator plane of the 6x100 µm device for different input power, clearly showing a Class F working condition.

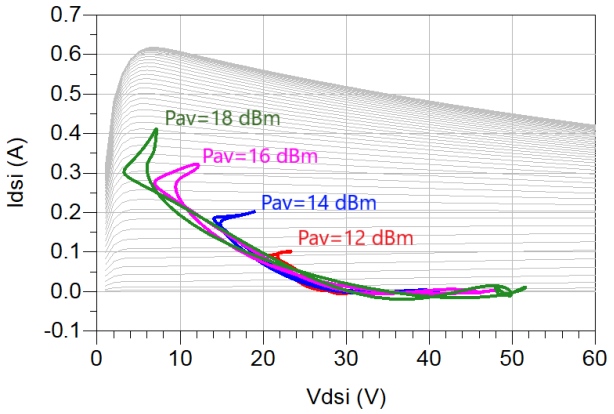


Fig. 1. Simulated load lines at the intrinsic current generator plane of the device in the Peaking final stage.

III. Carrier branch design and DPA integration

For the Carrier amplifier, the same 6x100µm device was considered. It was biased in class AB ($I_D = 30\,mA$) and made unconditionally stable by using the same stabilization network of the 6x100µm device in the Peaking branch. A Class F design strategy is adopted in order to maximize the delivered output power and the efficiency, exploiting the favorable phase relationship between the first and the third current harmonics of the class AB. The same topology of the OMN adopted for the Peaking final device was used, while the values of the components were slightly tuned to compensate for the difference of the parasitic effects associated to the different biasing condition. Furthermore, in this case, being the target OBO of 6 dB, the OMN was also optimized to show, at the intrinsic plane $2R_{OPT} = 266\,\Omega$ in back-off condition and $R_{OPT} = 133\,\Omega$ at saturation. In the Carrier branch, no driver stage was adopted to save efficiency, thus a simple IMN was designed to match this branch to $50\,\Omega$. Then, both Carrier and Peaking branches were combined as shown in Fig. 2.

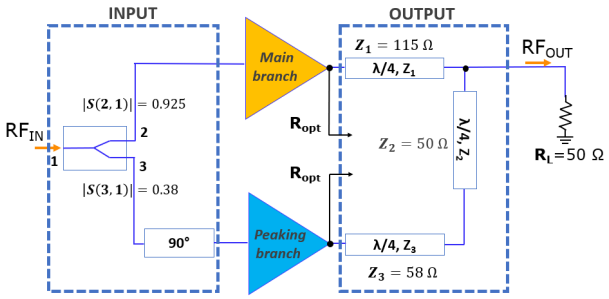


Fig. 2. Simplified scheme of the combination structure for the proposed DPA.

For the output combiner, the structure proposed in [5] was adopted, avoiding the use of a post-matching network by properly optimizing the characteristic impedances of the $\lambda/4$ elements. The latter were then realized with a semi-lumped solution to reduce the resulting size.

At the input, it was required an uneven power divider unbalanced towards the Carrier branch and with a 90° of phase shifting. For this splitter, an uneven branch line was designed by using semi-lumped approach as well. A picture of the realized MMIC is shown in Fig. 3, resulting in a chip area of 3.65 x 3 mm^2.

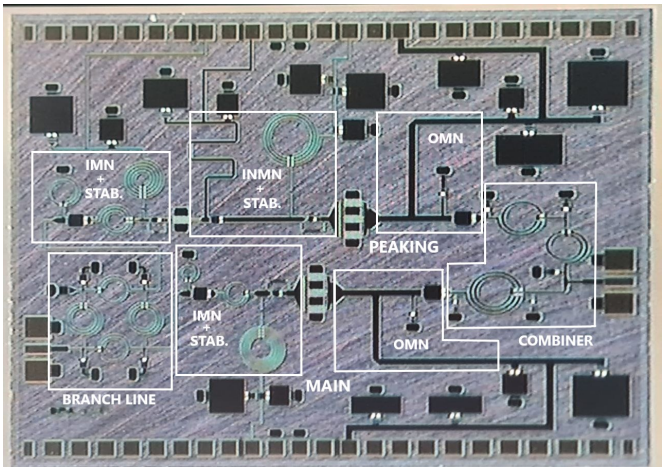


Fig. 3. Photo of the fabricated MMIC DPA (size: 3.65 mm x 3 mm), the various sub-networks are highlighted.

IV. Experimental results

The characterization of the fabricated DPA is carried out considering the nominal drain voltage $V_{DD} = 28V$ and the following gate bias points for the three devices involved:

- $V_{GG} = -3.2\,V$ (deep class C) for the driver stage of the Peaking branch;
- $V_{GG} = -2.6\,V$ (shallow class C) for the final stage of the Peaking branch;
- $V_{GG} = -1.83\,V$, $I_{D,Q} = 30\,mA$ (class AB) for the Carrier amplifier.

A. Small Signal Performance

The comparison between simulated (solid line) and measured (circle symbols) scattering parameters is shown in Fig. 4. Notably, a good agreement has been registered all over the frequency range from 0.1 to 20 GHz. The measured small-signal gain is about 10 dB at 10 GHz with an input and output return loss of about 9.2 dB and 9.3 dB, respectively.

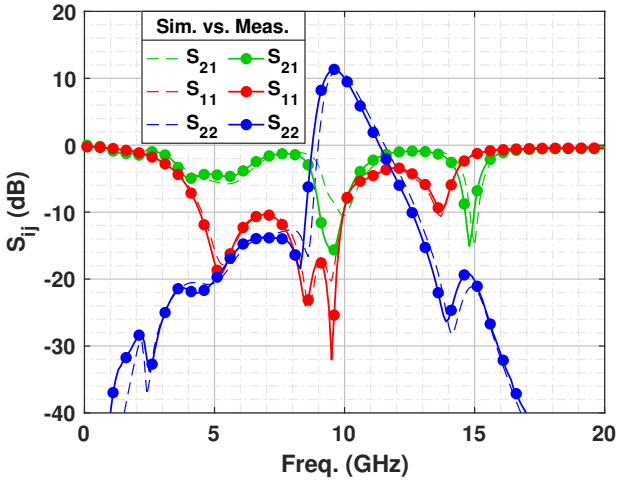


Fig. 4. Comparison between simulated (solid lines) and measured (circle symbols) small signal parameters of the realized DPA from 0.1 GHz to 20 GHz

B. Large Signal Performance

Fig. 5 shows the comparison between measured and simulated nonlinear performance of the DPA at center frequency. The agreement is quite good for both output power and gain, whereas the efficiency is not accurately predicted by the models when non-linearities become relevant. Anyway, the measured output power is larger than 36 dBm with an associated gain and efficiency of 9 dB and 40%, respectively. Finally, Fig. 6 shows the same features over frequency both at saturation and 6 dB output power back-off. At saturation, the output power is slightly lower than 36 dBm over the upper side of the bandwidth. A similar trend is also experienced for the efficiency, which, however, remains always higher than 33%. Notably, the gain compression in the 6 dB OBO is very limited, which demonstrates the proper synchronization of both DPA branches.

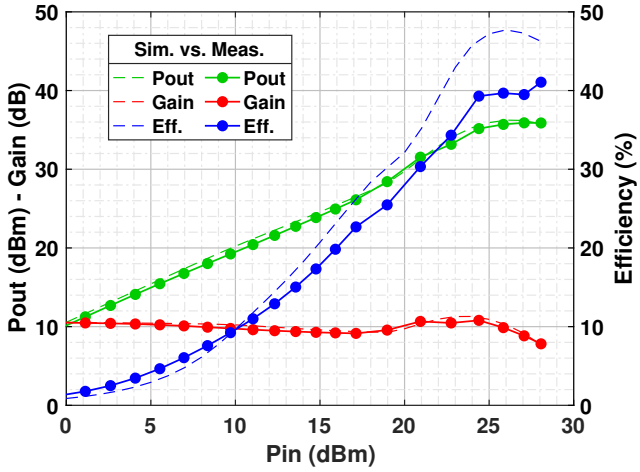


Fig. 5. Measured and simulated output power, efficiency and Gain at 10 GHz as functions of the input power.

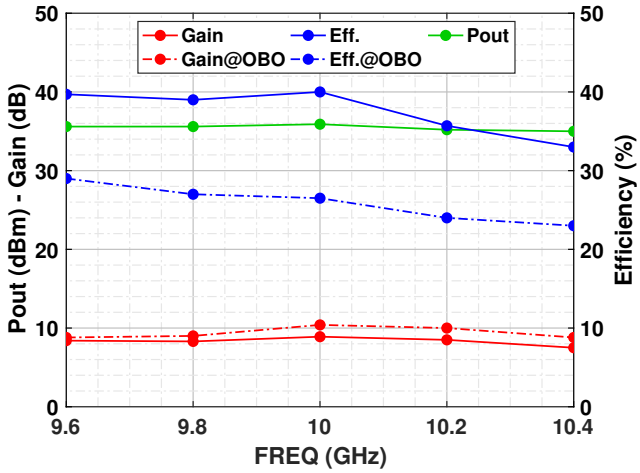


Fig. 6. Measured output power, efficiency and gain over the bandwidth at saturation and 6 dB OBO.

V. Conclusion

This paper has presented a design strategy suitable to improve the performance of a DPA Peaking branch by exploiting the nonlinear interaction between a driver and final stage to synthesise a Class F configuration in both stages. The experimental results of the realized GaN MMIC prototype for X-band applications have shown the potentiality of the proposed approach, achieving a peak of 36 dBm output power, 40% efficiency and 9 dB gain at saturation.

Acknowledgment

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