A 6-bit Low-Area Hybrid ADC Design For System-on-Chip Measurements

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***Abstract*—In recent years, with the declining dimensions of transistors, the system-on-chips (SoCs) have had more physical defects. These physical defects ultimately result in failures that cannot be tolerated in functional safety applications such as electric cars, aerospace, etc. For the digital peripherals of the SoCs, there are well-known methods such as scan chains, whereas there are methods for analog circuits such as analog scan chains or Analog Test Bus (ATB).**

This paper presents a 6-bit, low-area Analog-to-Digital Converter (ADC) for SoC analog voltage measurements. The advantage of the proposed ADC design is the low additional area cost to the design of the SoC and increasing the testability of the analog peripherals. This ADC design converts the analog signals, which are difficult to observe, to the digital domain, which is easy to route and observe. This architecture comprises two small ADCs for doing coarse and fine conversions. The ADC for the coarse conversion is a 3-bit SAR ADC, and the ADC for the fine conversion is a 3-bit flash ADC. The suggested ADC is implemented using the 130 nm technology of the Infineon, and it has a total area of 0.007 mm^2. The fine ADC of the proposed ADC can be shared between the peripherals nearby inside the SoC, and the additional area per peripheral would be only 0.0015 mm^2. The Signal-to-Noise Distortion Ratio (SNDR) of the design is 37dB, and the Figure of Merit (FoM) is 2.15 pJ/conv.

***Index Terms*—Analog-to-Digital Converter, ADC, System-on-Chip, SoC, Analog Test Bus, Testing.**

I. Introduction

RECENT developments in the field of automotive applications have led to a rising interest in automotive System-on-Chips (SoCs). These automotive SoCs are widely used in applications such as robotics, aerospace, electric cars, and so on. With the shrinking dimensions and increasing speed of the transistors, they are more prone to physical defects. These physical defects result in errors, and the propagation of these errors causes failure in the final application. Thus, there are more advancements in the design complexity of integrated circuits. In safety-critical applications where the failure is unacceptable, it is necessary to have robust mechanisms to detect the faulty units inside SoCs. Therefore, testing the SoCs during the production and application phases is essential.

Every SoC consists of several analog, digital, analog/mixed-signal peripherals; for each type, there are techniques to test them [1]. In order to test the digital peripherals, there are several methods, such as scan chains [2], the functional test used for testing different parts of the CPUs [3], [4]. Moreover, innovative methods are applying the same scan chain idea for the analog circuits [5], or some other methods that aim to have a Built-in Self-Test (BIST) for self-testing the Analog to Digital Converters (ADCs) [1]. In the field of design for testability of analog circuits, there are some attempts to have an automated way of hardware addition for testing the analog circuits [6]. Another solution for testing the analog components inside a SoC is to have an Analog Test Bus (ATB). The testing methods for the digital components are more advanced than those for the analog domain, and they can detect most of the physical defects. Nevertheless, it is more challenging for analog components to have controllability and observability over analog signals [7]. ATB architecture has multiple analog routings, and due to the shrinking transistor dimensions and overall chip die area, it is difficult to route analog signals around the chip because these analog routings are susceptible to noise and cross-talk.

In this work, we present a new low-area ADC architecture for converting the analog signals inside the peripherals to digital values, which are easy to route. The proposed ADC has a very low die area so that it can be used inside the peripherals close to the analog signals. In this case, the analog signals are less susceptible to noise and cross-talk because the converted values are in the digital domain. Routing these signals in the digital domain is more effortless than routing them with the original analog signals.

This novel ADC design is a hybrid ADC made of two small ADCs to perform coarse and fine measurements inside the chip. The main advantage of this design is the low additional area to each peripheral inside the SoC. This design can reduce the analog routings around the chip related to the ATB design by converting analog signals to digital domains. The result of the conversion can be used by the user or Automated Test Equipment (ATE) to test the analog peripherals.

This article outlines the guiding fundamentals required to understand the proposed design in section II. After explaining the basic concepts, in section III, we present the proposed ADC design in detail. Then, in section IV, the proposed approach's performance is evaluated and compared with the available designs in the state-of-the-art. Lastly, we draw conclusions about this work in section V.

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II. Background

This part of the work provides the essential groundwork required to grasp the workings of the different ADCs and ATB circuits and critically examine their respective limitations and advantages. By exploring these constraints, we are better positioned to suggest innovative strategies to alleviate or completely resolve the identified issues.

A. Successive Approximation Register (SAR) ADC

Figure 1 provides a clear representation of the fundamental architecture of a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) circuit. This circuit comprises four integral subcircuits:

1) **Sample and Hold (S/H) Unit:** This module takes in the analog voltage, holds it constant, and forwards this stable input to the comparator for evaluation.
2) **Digital-to-Analog Converter (DAC):** The DAC is crucial for converting the tentative digital output of the SAR logic back into an analog signal for comparison against the held sample.
3) **Comparator:** Acting as the decision-maker, the comparator receives the held analog voltage at its positive terminal and the analog output from the DAC at its negative terminal, comparing the two voltages.
4) **SAR Logic Circuit:** This is the digital brain of the operation, which controls the DAC and interprets the comparator's results to refine the digital output iteratively.

By employing this binary search strategy, the SAR ADC effectively narrows down the possible values for the digital output, homing in on the correct representation bit by bit until the conversion is complete. Each step refines the approximation, leading to a precise digital equivalent of the input analog signal.

The output voltage is generated through a carefully orchestrated process, as depicted in Fig. 2, which utilizes a binary search method. This methodical approach to digital signal processing involves several steps:

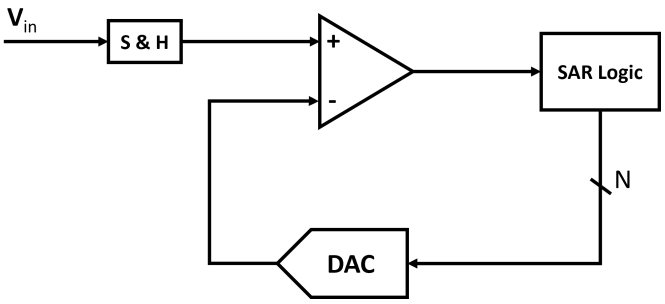

Fig. 1. Schematic presentation of the SAR ADC architecture.

1) **Initialization:** The algorithm begins by setting the most significant bit (MSB) in the digital code to one.
2) **Comparator Decision:** According to the comparator's feedback, the algorithm determines whether to retain the MSB at its current value (one) or to reset it to zero.

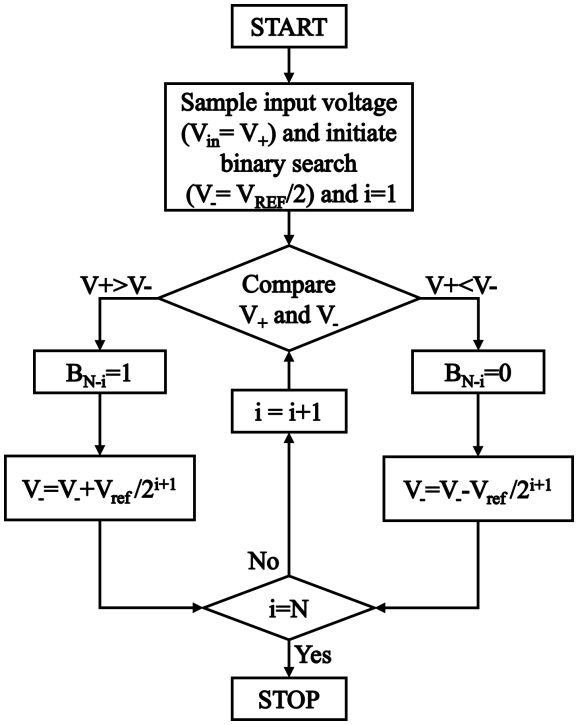

Fig. 2. Algorithm of SAR ADC

3) **Subsequent Approximations:** The algorithm estimates the next significant bit once the MSB is set. This estimation is done by assigning a value of one to the MSB-1 bit and observing the comparator's response.
4) **Bitwise Iteration:** The process repeats the previous steps, moving from higher-order bits to lower-order ones. At each step, the comparator's output guides whether to keep or adjust the bit being guessed.
5) **Finalization of Conversion:** This iterative process ends with evaluating the least significant bit (LSB). Determining the LSB's value marks the end of the conversion cycle.
6) **Resulting Digital Code:** The final result of these sequential decisions yields a digital code that accurately represents the original analog input voltage.

Several error sources need to be corrected for the accuracy and resolution of this architecture. These inaccuracies may stem from flaws within the architecture's DAC component or other parts of the circuit. Nearly every ADC design incorporates a DAC, and many of the remaining errors are heavily influenced by the specific layout and structure of the architecture.

B. Flash ADC

The flash ADC is another type of ADC architecture. The circuit schematic of the classic flash ADC is provided in Fig.3. A flash ADC comprises a linear voltage divider, numerous comparators, and a decoder circuit. For each generated voltage by the divider, there is a comparator that compares the input voltage with the generated voltage levels. [8], [9] The delay

of this circuit is one clock cycle, and there are 2 to the power of the number of the bits. There are comparators and voltage levels. The voltage divider is based on the voltage division based on the ladder made by resistors or capacitors. Once all the comparisons are done, the comparator outputs go to a decoder circuit, which generates the output code.

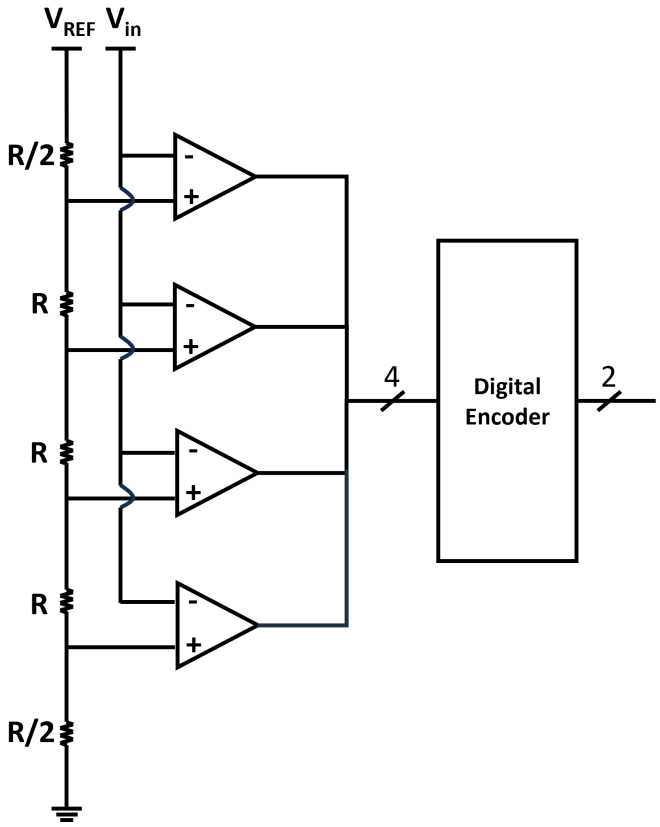

Fig. 3. Flash ADC circuit schematic.

C. Analog Test Bus (ATB)

The ATB design facilitates connecting analog components within the SoC, with Fig. 4 providing a visual guide to its framework. This setup features analog switches, known as Analog Multiplexers (AMUX), which enable the selection and routing of analog signals, the internal connections that carry these signals and a central unit that controls the entire operation.

At the heart of the ATB, a comprehensive unit houses the necessary switches to facilitate signal choice, a control module to guide the AMUX selection for the desired intellectual property (IP) signal, and an Analog-to-Digital Converter (ADC) for translating analog inputs into their digital counterparts. The digital signals are then relayed to the SoC's test pin, making them accessible to external Automatic Test Equipment (ATE).

Within the layout of the ATB, the analog routings are especially susceptible to noise, often arising from the signal traces' inherent parasitic capacitance and inductance. This susceptibility to interference is observed when specific IPs,

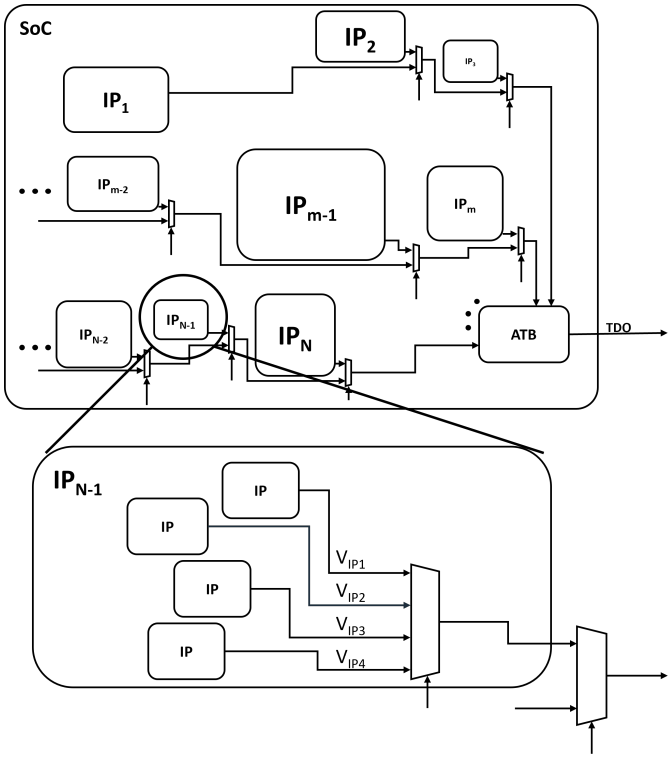

Fig. 4. A simple schematic of the ATB.

such as switching regulators and phase-locked loops (PLLs), generate high-frequency voltage spikes.

This noise impacts the efficacy of the ATB and leads to a degradation in the chip's overall performance [7]. Implementing strategies for digitization at a local level is essential to mitigate these performance issues. Furthermore, adopting alternative approaches, such as using voltage buffers across the SoC, could prove beneficial; however, these solutions demand a considerable trade-off concerning the chip's area.

III. Proposed Approach

This section presents the proposed hybrid ADC design. The proposed circuit, depicted in Fig.5, shows the circuit schematic of the hybrid ADC. The hybrid ADC in this work is for locally measuring the analog signals of the SoC. In this 6-bit hybrid ADC, the conversion is done in two coarse and fine steps, where coarse and fine ADCs are used to measure the 3 MSBs and 3 LSBs. The reason behind choosing six bits for the ADC design is based on the limitations on additional area per IP and the required accuracy.

The proposed circuit can be split into two elements:

1) **The SAR ADC:** This circuit is used for the coarse measurement of the DC signal. This circuit provides the 3 Most Significant Bits (MSBs).
2) **The flash ADC:** This circuit is used for the fine measurement. The flash circuit provides the 3 Least Significant Bits (LSBs).

Inside an SoC, this circuit can be divided into two parts. As provided in Fig.5, each IP can have a 3-bit SAR ADC

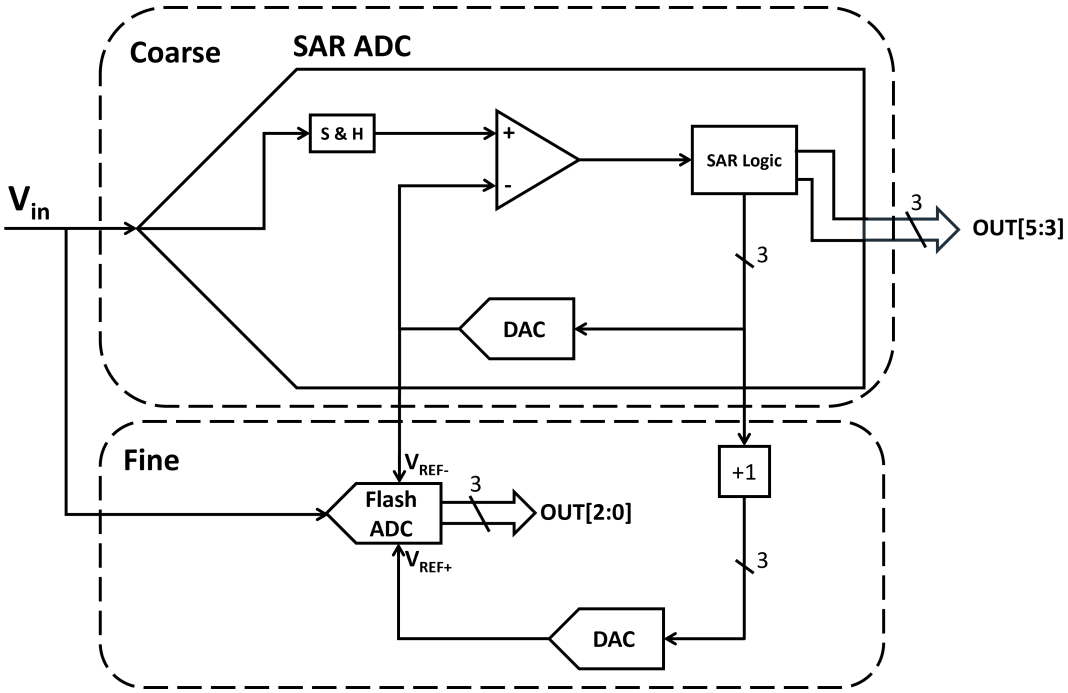

Fig. 5. The proposed hybrid ADC circuit schematic.

for coarse measurement and a shared Flash ADC for fine measurements. This section provides more details about the proposed circuit and the possibility of the splitting this circuit for SoC measurements.

The design of the proposed ADC involves converting analog voltages from integrated peripherals (IPs) through a two-step process consisting of coarse and fine phases:

- In the coarse phase, as detailed in Fig.6, the SAR ADC is responsible for generating the three MSBs of the digital output.
- Subsequently, these three MSBs are incremented by '001' (equivalent to "+1" as visualized in Fig.5). This specific incrementation is needed to establish the threshold values for the next phase.
- The incremented value feeds into two separate Digital-to-Analog Converters (DACs), as indicated in Fig.5. These DACs set the upper and lower voltage limits for the final conversion stage.
- The fine phase occurs with the Flash ADC taking the high and low voltages defined by the DACs to compute the three LSBs precisely.
- Once the Flash ADC has resolved the 3 LSBs, the digital conversion is deemed complete, ending in the full digital representation of the original analog input.

One advantage of the proposed hybrid approach is that it enables the fast generation of the pass/fail signal, which can be used to test the analog signals inside each IP. Generally, there is a pass range for the analog signals inside the IPs. Using the coarse conversion of the hybrid architecture enables pass/fail signal generation by comparing the coarse conversion value with the pass range value.

Typically, the number of bits in a SAR ADC is limited to

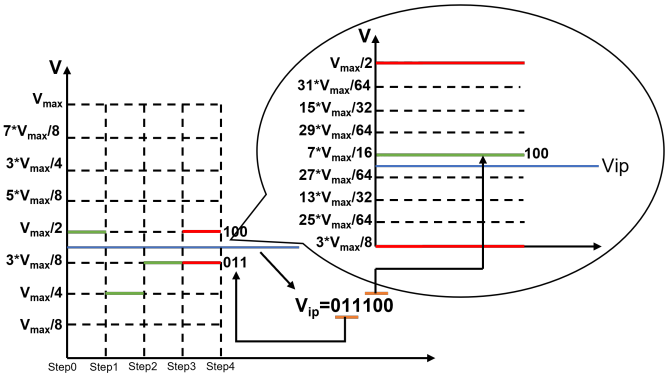

Fig. 6. An example of the measurement in the proposed hybrid ADC.

12 bits with a low hardware cost. This limitation is because of the need for a high-precision reference voltage. Moreover, we have an enormous additional area due to the calibration of the DAC. Additionally, the possible area overhead we can add to each IP is limited, and adding a high area ADC per IP is not reasonable. Taking into account the aforementioned limitations, the feature of the design should be adding a very low area to the IP. The area of the flash ADC is higher than the SAR ADC, based on the dominant contribution of the comparators to the area of the ADC circuits. In a flash ADC, the number of comparators is proportional to the power of two of the number of bits, but SAR ADC has the same number of comparators for any number of bits. Thus, in the proposed ADC design, the area of the fine flash ADC is high, and the area of the coarse SAR ADC is low. In order to have this hybrid ADC functioning in the SoC, one idea is to use the entire architecture inside the IP or have the SAR ADC inside

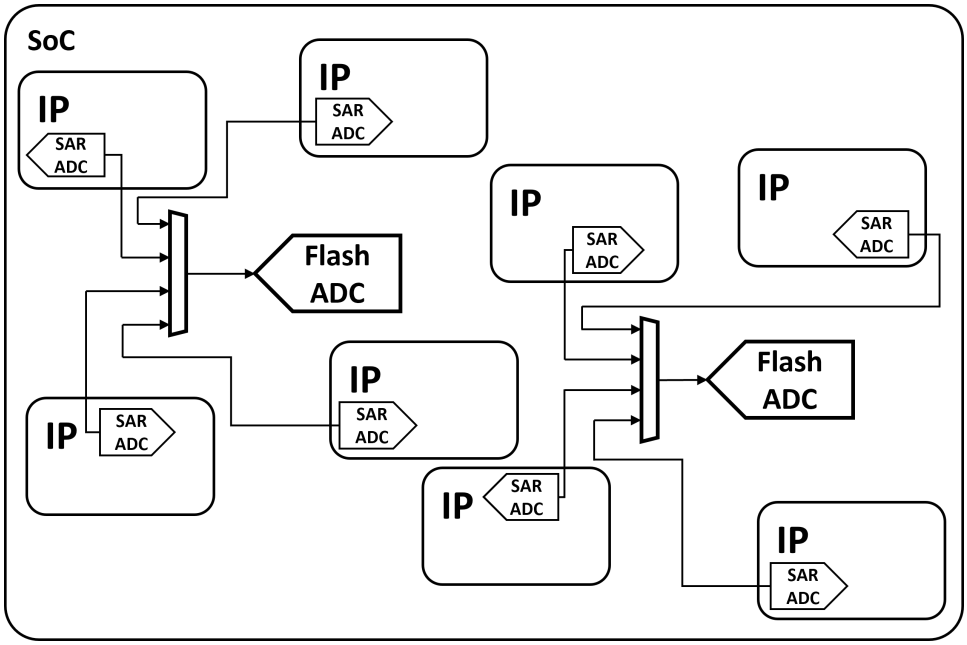

Fig. 7. Schematic of the sharing fine part of the hybrid ADC.

the IP, which is small, and share the flash ADC, which is large, with the other IPs using some multiplexers as shown in fig.7. Therefore, we can use this architecture to measure the analog signals inside the SoC instead of the classical ATB approach.

IV. Experimental Results

This section reports the essential characteristics of the hybrid ADC design proposed in this work. These characteristics are area, number of bits, integration technology, and so on. Then, it compares the proposed design with the other state-of-the-art designs.

A. Performance Evaluation

The proposed hybrid ADC design is implemented using the Infineon 130nm CMOS technology. The supply voltage of the ADC architecture is 1.5V, and the accuracy of the ADC is 20mV. The total area of this design is $0.007mm^2$, and the area occupied by the coarse part of the ADC is $0.0015mm^2$. Meanwhile, the area occupied by the fine part is $0.0042mm^2$. The rest of the area is occupied by the +1, and the DAC circuit is used to provide the high and low supplies of the fine part. This ADC has a power consumption of 1.12mW and a Figure of Merit(FoM) of 2.15pJ/conv. The performance analysis of the proposed ADC circuit is provided in the tableI.

TABLE I
Performance Analysis of the proposed ADC.

Technology	130 nm
Total Area	0.007 mm^2
Coarse part area (Area per IP)	0.0015 mm^2
Fine part area	0.0042 mm^2
Sampling frequency	10 MHz
# Bits	6
Supply voltage	1.5 V
Power consumption	1.12 mW
FoM	2.15 pJ/conv
SNDR	37 dB

B. Comparison with State-of-the-art

In this section, in order to have a clearer idea about the presented ADC's performance, we compare the ADC in this work with similar architectures in terms of precision and topology found in the state-of-the-art. In table II, the proposed hybrid ADC is compared in parameters such as area, Signal-to-Noise Distortion Ratio (SNDR), Figure of Merit (FoM), power consumption, and number of bits.

To more accurately evaluate the ADC area efficiency, we tried to have all of the architectures integrated into the same technology. Generally, the area does not scale linearly with the integration technology in mixed-signal circuits. However, regarding the area, the proposed ADC design has a remarkable area efficiency with a total area of $0.007mm^2$. The closest competitor to the proposed design is the design of the [10] with a die area of $0.03mm^2$, considering that it is implemented in 28 nm integration technology.

The table II indicates a standardization at 6 bits for most ADCs, including the proposed work, which is adequate for applications that do not require high-resolution conversions. Two ADCs ([11], [12]) offer higher resolution at 10 bits, catering to applications necessitating greater precision.

The proposed ADC achieves an SNDR of 38 dB, outperforming several counterparts like those referenced in [10], [11], [13] and showing a moderate improvement. It is, however, surpassed by ADCs [12], [14], which present exceptionally high SNDR values above 50 dB, indicative of superior

TABLE II
COMPARISON OF THE PROPOSED ADC WITH THE STATE-OF-THE ART.

	[15]	[11]	[14]	[12]	[13]	[10]	This work
Architecture	Flash	Flash	Hybrid ***ST	Hybrid **SF	Hybrid SAR	*TI Hybrid	Hybrid SAR
F_s (MHz)	1200	1600	0.25	1000	0.2	2400	10
Area (mm^2)	0.12	0.13	0.04	N/A	0.097	0.03	0.007
#Bits	6	6	10	6	10	6	6
SNDR (dB)	35.5	30	53.7	35.56	56.91	34.8	38
Technology (nm)	130	130	90	28	180	28	130
FoM (pJ/conv) ($\frac{Power}{2^{ENOB}.f_{sample}}$)	2.2	2.6	2.02	0.0477	0.015	21	2.15
Power (mW)	160	180	0.0002	2.33	0.002	23	1.12

*TI: Time-Interleaved, **SF: SAR Flash, ***ST: SAR Time-domain, F_s: Sampling Frequency

noise performance and precision.

The proposed ADC reports a competitive FoM of 2.15 pJ/conv, which measures energy efficiency per conversion. It is on par with other designs but is outclassed by ADCs [13], [14], which demonstrate exceedingly low power consumption per conversion, with [14] having an impressive FoM of 0.015 pJ/conv.

In terms of power, the proposed ADC is highly efficient, consuming only 1.12 mW, which is significantly lower than most of the compared works, except for [12], [14]. These two ADCs exhibit ultra-low power consumption but at the expense of higher area and lower technology nodes.

In summary, the proposed ADC offers an excellent balance between size, power consumption, and performance, with a particular advantage in its compactness. While it does not lead in every category, such as SNDR or FoM, where the 10-bit ADCs outperform it, its overall specifications suggest that it is a competitive design in the context of low-power and space-efficient applications, which is the main target of this work. This analysis underscores the trade-offs inherent in ADC design, highlighting that the best choice of ADC architecture depends on the specific requirements of the intended application.

V. CONCLUSION

This work presented a new hybrid ADC architecture for converting the analog signals inside the analog peripherals of the SoCs. This architecture is implemented in the 130 nm CMOS technology of the Infineon. The total area of this architecture is the same as that of similar architectures available in the state of the art. However, because of the possibility of sharing the fine part of the proposed design with some peripherals, there is a low area overhead per peripheral. The total area of the ADC is 0.007 mm^2, and the additional area per peripheral is 0.0015 mm^2.

The proposed approach still has analog routings related to routing the reference voltage and the analog signal to the fine ADC. However, in comparison to the original architecture of the ATB, there is a significant reduction in the length of analog routings.

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