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Device-Aware Test for Anomalous Charge Trapping in FeFETs

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ABSTRACT

The development of Ferroelectric Field-Effect Transistor (FeFET) manufacturing requires high-quality test solutions, yet research on FeFET testing is still in a nascent stage. To generate a dedicated test method for FeFETs, it is critical to have a deep understanding of manufacturing defects and accurately model them. In this work, we introduce the unique defect, Anomalous Charge Trapping (ACT), in FeFETs. The ACT-defective FeFET is characterized, and the physical mechanism of the defect is explained. Then, we apply the Device-aware Test (DAT) method to design a specific ACT-defective FeFET model, which includes the physical impact of the defect on the electrical parameters of defect-free models, and calibrate the model with measurement data. Fault modeling is performed based on circuit-level simulations, and dedicated test solutions are proposed.

CCS CONCEPTS

• **Hardware** → **Defect-based test**; **Emerging technologies**.

KEYWORDS

Memory test, FeFET, device-aware test, defect modeling, fault modeling, charge trapping

*Both authors contributed equally to this research.

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1 INTRODUCTION

Ferroelectric Field-Effect Transistors (FeFETs) emerged as a promising Non-Volatile Memories (NVMs) technology, which has shown potential in a wide range of fields, like the embedded system, the storage class memory, and the Computing-in-Memory (CIM) system [1–7]. However, the current development of FeFET still faces challenges, one of which is its vulnerability to defects [8]. The FeFET test is in its nascent stages. To develop high-quality test solutions suitable for high-volume production of FeFETs, it is crucial to understand the defect mechanisms and derive accurate defect and fault models.

Currently, most of the works on FeFETs focus on the fault-free devices. As far as we know, [8] is the first and the only published paper discussing FeFET testing. However, it applied the FeFET model based on Technology Computer-Aided Design (TCAD), which is not compatible with circuit-level simulations. Hence, it is critical to developing a dedicated test solution for FeFETs; a starting point is previous works state-of-the-art memory testing. Works on regular memories, like SRAMs and DRAMs, model defects as linear resistors, and generate write/read-based test solutions [9–11]. The same method has also been utilized for some NVMs, like RRAMs and MRAMs [12–14]. However, some works show that due to the specific physical mechanisms of devices in NVMs, they may present unique types of defects [15]. These defects cannot be modeled by

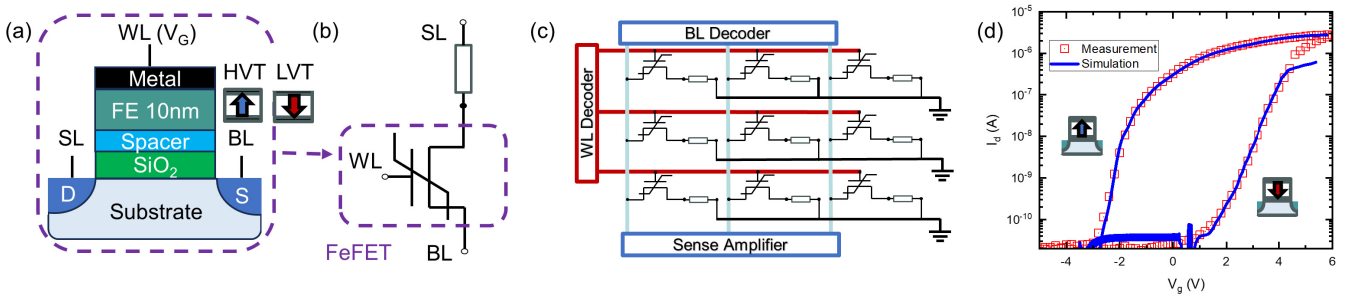

Figure 1: (a) FeFET device; (b) 1T-1R cell; (c) 3×3 array; (d) FeFET measurement and model calibration

resistors, since NVMs behave irregularly in their presence. Hence, the Device-aware Test (DAT) method is proposed, in which specific compact models for defective NVMs are designed by incorporating the impact of physical (manufacturing) defects on electrical and magnetic behavior [16–18]. Dedicated fault models and test solutions are generated thanks to these defective NVM models. For example, the DAT approach has been employed for modeling and testing Ion Depletion defects in RRAMs [19] and Back-Hopping defects in MRAMs [20]. Similar to the case of RRAMs and MRAMs, both methods (i.e., modeling defects with linear resistors and the DAT method) can be employed in FeFETs to develop low escape test solutions.

In this paper, we introduce a new unique defect in FeFETs: the Anomalous Charge Trapping (ACT). The observed defect is attributed to an excessive injection of electrons into the gate stack. This results in a reduction of the Memory Window (MW), which consequently leads to write/read faults. The DAT is applied to detect this defect following four steps: 1) defect characterization, 2) defect modeling, 3) fault modeling, and 4) test generation. The main contributions of this paper are as follows:

- Characterize the ACT-defective FeFETs, and explain the physical mechanism of this defect.
- Design the device-aware defect model for the ACT defect and calibrate it with measurement data.
- Perform the fault modeling based on circuit-level simulations and derive specific fault models.
- Put forward both March tests and Design-for-Test (DfT) methods to detect ACT.

The rest of this paper is structured as follows. Section 2 introduces the background of FeFETs. Section 3 measures the ACT-defective FeFETs, and explains the physical mechanism. Section 4 designs the specific ACT-defective FeFET, and calibrates the model with the measurement data. Section 5 performs the fault modeling to derive dedicated fault models. Section 6 designs the march test and the DfT method for ACT. Section 7 performs discussions on the charge-trapping phenomenon. Section 8 concludes this paper.

2 BACKGROUND

2.1 FeFET device

Fig. 1(a) presents the FeFET device architecture utilized in this work [5]. The FeFET features a structure similar to Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), comprising the substrate, the Source/Drain (S/D), and the multi-layer gate stack. The gate stack comprises a metal layer, a ferroelectric (FE) layer, a spacer (e.g., a thin metal layer), and a SiO_2 layer. The FE layer is made of multi-domain material; when all domains are polarized positively ('↑'), the FeFET exhibits a high threshold voltage (V_{th}), also known as High Threshold Voltage (HVT) or logic 0'. Conversely, when all domains are polarized negatively ('↓'), the FeFET demonstrates a Low Threshold Voltage (LVT), or logic '1'. A critical parameter for assessing FeFET performance is the Memory Window (MW), defined as MW = HVT − LVT. A large MW signifies superior FeFET performance. Fig. 1 (d) presents $I_d - V_g$ (drain current vs gate voltage) measurement data of defect-free FeFETs, in which the hysteresis phenomenon is observed, and the HVT curve is the horizon shift of the LVT curve. The FeFET compact model is described in [21], and calibrated with the measurement.

2.2 FeFET cell

Fig. 1 (b) presents the 1T-1R FeFET cell structure, with three terminals connected to the Bit Line (BL), Source Line (SL), and Word Line (WL), respectively [22]. During write operations, a large gate voltage V_g is applied to the WL while the SL and BL are grounded. The FE domain domains switch to 'positive' or 'negative' states depending on whether V_g is positive or negative, corresponding to $w0$ or $w1$ operations. In read operations, a small V_g selects the cell, and the voltage between BL and SL detects the FeFET channel resistance. In the '0' state, characterized by a high V_{th}, the inversion layer is not formed (i.e., the MOSFET works in the cutoff region), resulting in high channel resistance. Conversely in the '1' state, characterized by a low V_{th}, the inversion layer is formed, leading to low channel resistance (see Fig. 1 (d)).

2.3 FeFET array

Fig. 1 (c) presents the 3×3 FeFET array with associated peripheral circuits, where cells in the same row share the same WL, cells in the same column share the same BL and SL [22, 23]. Peripheral circuits consist of the WD decoder, the BL decoder, and the sense amplifier. The WD decoder selects the cell, and applies a V_g to perform write or read operations. The sense amplifier extracts the channel resistance. Here the array applies a structure similar to the NOR Flash. The testing method of this work can also be applied to other structures (e.g., structures similar to NAND Flash).

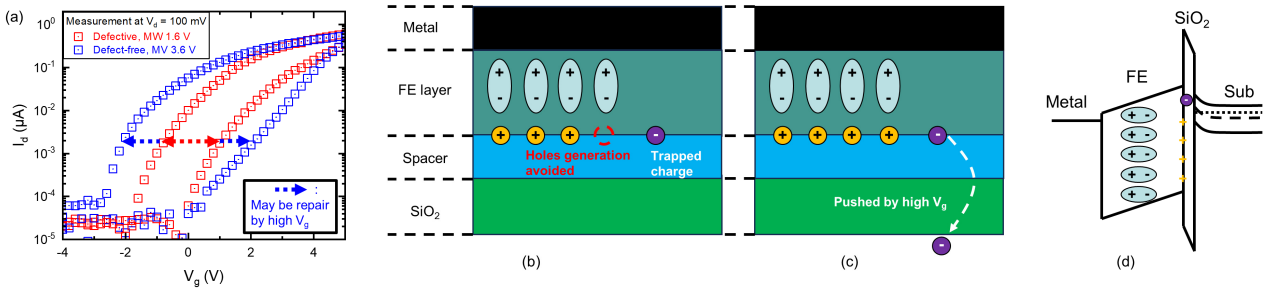

Figure 2: (a) defect characterization; (b) physical mechanism of charge trapping; (c) physical mechanism of repair; (d) energy band diagram with trapped charge.

3 DEFECT CHARACTERIZATION

This section presents the performance of ACT-defective FeFETs, and compares it with the defect-free ones.

3.1 Identification of ACT

Charge trapping is a common phenomenon in FeFETs, which refers to the phenomenon that unwanted charges are injected into the gate stack during the manufacturing process or by voltage pulses [24]. Typically, optimizing the fabrication process and producing a high-quality gate stack can minimize the charge injection. However, certain issues in manufacturing (e.g., spacer sputtering leading to SiO_2 damage) can facilitate the electron injection, thus introducing a defect called 'Anomalous Charge Trapping (ACT)'.

Fig. 2 (a) compares the $I_d - V_g$ hysteresis measurement data of ACT-defective and defect-free FeFETs. The measurement is performed by sweeping V_g and keeping $V_d = 100$ mV, and V_{th} is defined by the V_g at $I_d = 1$ nA. The V_g sweep starts from -6 V to 6 V, and then reverses back from 6 V to -6 V. The defective result is depicted by the blue line in Fig. 2 (a), showing a reduced MW of 1.6 V. The same measurement on defect-free FeFETs is performed, and the measurement data is presented by the red line in the figure, indicating an MW of 3.6 V. Notice that the red hysteresis line is in the middle of the blue hysteresis line. For the defective FeFETs, the V_{th} in the LVT is increased, while the V_{th} in the HVT is decreased, implying a higher channel resistance in logic '1' and a lower channel resistance in logic '0; this potentially leads to reading faults. Moreover, the reduced MW may cause the FeFET to fall into the undefined state ('U' state, where the FeFET channel resistance between normal high state in logic '0' and normal low state in logic '1'). This may further cause Hard-to-Detect (HtD) faults [18].

Some charge trapping phenomena are reported repairable [24]. For example, if we apply a large V_g to the defective FeFET, the MW may be increased to close to that of defect-free FeFETs, implying the device has been repaired. However, applying a large V_g requires additional circuits while posing a significant risk of breakdown. Moreover, there is no guarantee that all defective devices can be successfully repaired.

3.2 Physical mechanism

Fig. 2 (b) presents the mechanism of the ACT defect, and Fig. 2 (d) presents the related energy band diagram. The V_{th} shift of defect-free FeFETs is based on the FE layer exerting the field effect onto the transistor channel through the FE polarization charge (i.e., the blue ellipse boll in the figure) [25]. Charges (e.g., holes, the yellow bolls in the figure) are generated to balance the polarization. When electrons (the purple circles) are injected into the gate stack, they will isolate the FE polarization, avoiding the hole generating, and eventually leading to the MW loss [24, 26]. Notice that charge trapping is a common phenomenon in FeFETs. Here we only focus on the anomalous case caused by manufacturing imperfection. For example, the spacer spattering damages the SiO_2 layer, causing a large amount of electron injection [24].

A large V_g pulse may push injected electrons out of the gate stack, as presented in Fig. 2 (c). Thus, the MW is recovered and the defective FeFET is repaired. However, in theory, we cannot guarantee all electrons are pushed out. Besides, we must consider the risk of high V_g damaging the device.

4 DEVICE-AWARE DEFECT MODELING

To guarantee a high-quality test solution, dedicated defect models must be designed due to the intrinsic non-linear characteristics of ATC. In this section, we follow the device-aware defect modeling approach with three steps [16]: 1) physical defect analysis and modeling, 2) electrical defect modeling, and 3) model optimization.

4.1 Defect-free FeFET model

The defect-free FeFET model is designed by calculating the key parameters 'ferroelectric polarization P_{FE}', as follows [27]:

$$\begin{aligned} P_{\mathrm{FE}} &= P_S \cdot \tanh\left(V_{\mathrm{FE}} - \mathrm{dir} \cdot E_C \cdot t_{\mathrm{FE}}\right) \\ V_g &= V_{FE} + V_{MOS} \end{aligned} \tag{1}$$

P_{FE}	Ferroelectric polarization	P_S	FE layer maximum polarization
V_{FE}	Voltage across the FE layer	dir	Polarization direction
E_C	Coercive field	t_{FE}	FE layer thickness
V_g	Gate voltage	V_{MOS}	Voltage across MOS structure

The relationship between I_d and V_g follows the conventional MOSFET model [28].

4.2 Physical defect modeling

Considering the physical analysis of the ACT defect, the ACT defect model must incorporate three key aspects:

4.2.1 Impact on P_{FE}. Due to the isolation of the FE polarization by injected electrons, only a portion of the FE layer domain switching impacts the V_{th} shifting. Hence, P_{FE} in Eq. 1 is reduced in defective FeFETs.

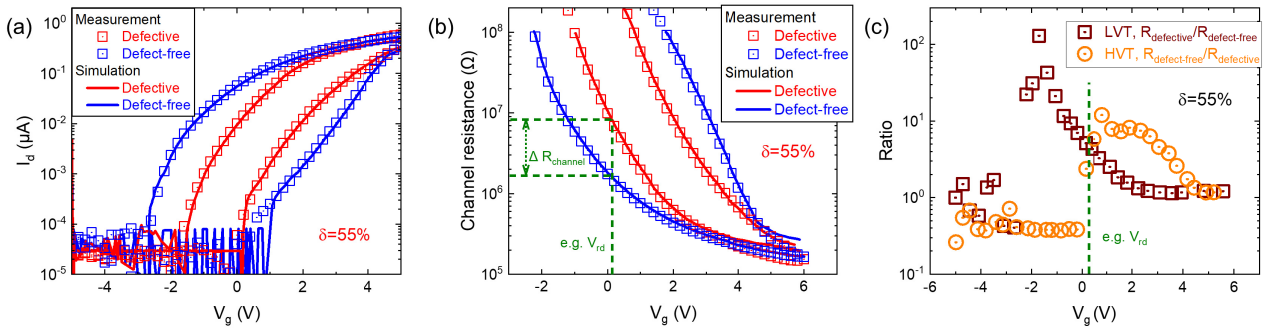

Figure 3: (a) $I_d - V_g$ measurement and fitting; (b) channel resistance measurement and fitting; (c) channel resistance ratio of defective and defect-free FeFETs.

4.2.2 Repairable. By applying a high V_g, electrons may be pushed out of the gate stack. Hence, the model must respond to a high V_g, and show the repairing process.

4.2.3 Reliability. Since regular write operations can inject electrons into the gate stack, the complete ACT model must address reliability issues caused by charge trapping. However, this work focuses on testing and only incorporates the first two aspects into the model.

In the next section, we will incorporate the physical impact of the ACT defect into the electrical parameters of the FeFET model.

4.3 Electrical defect modeling

To properly model the impact of injected electrons on the FE polarization, here we introduce a new parameter δ, which is negatively correlated with the total amount of injected electrons. We integrate δ into Eq. 1, presented as:

$$P_{\mathrm{FE}} = \delta \cdot P_S \cdot \tanh\left(V_{\mathrm{FE}} - \delta \cdot \mathrm{dir} \cdot E_C \cdot t_{\mathrm{FE}}\right) \tag{2}$$

where δ is presented a specific function of V_g:

$$\delta = 1 - \delta_0 \cdot g\left(V_g\right), \quad g\left(V_g\right) = \begin{cases} 1 & \left(V_g \geq V_{rp}\right) \\ 0 & \left(V_g < V_{rp}\right) \end{cases} \tag{3}$$

δ_0 represents the defect strength, with $\delta_0 \in [0, 1]$. When $\delta_0 = 0$, $\delta = 1$, indicates that the FeFET is defect-free. Conversely, when $\delta_0 = 1$, $\delta = 0$ and $P_{FE} = 0$, which means $MV = 0$ and the device has only one state, rendering it non-functional. $g(V_g)$ is a specific function of V_g that represents the repair mechanism. If the model detects that V_g is sufficiently larger than the repair voltage V_{rp} (i.e., $V_g > V_{rp}$), $V_g = 0$ and δ becomes '1' permanently (not considering reliability). Otherwise, $V_g = 1$ and δ remains $1 - \delta_0$. The V_{rp} can be designed by measurements of FeFETs. Besides, we assume the time for electrons to be pushed out of the gate stack is ignorable compared with the duration of write/read operations.

4.4 Model calibration

Eq. 2 and Eq. 3 are realized by Verilog-A and then integrated into the conventional FeFET model [27]. The defective FeFET model fitting consists of two steps: 1) fitting the defect-free FeFET (i.e., set $\delta_0 = 0$); 2) fitting the ACT-defective FeFET by selecting the appropriate defect strength (i.e., δ_0). The fitting results of both cases are shown in Fig. 3 (a). The excellent fit indicates that this model can be applied to subsequent fault modeling and test generation processes.

Next, we further extract the FeFET channel resistance under $V_d = 100\,\mathrm{mV}$, as presented in Fig. 3 (b). Notice that the channel resistance of FeFETs $R_{FeFET} = V_d/I_d$, and V_g is applied to WL to select the device. Fig. 3 (c) compares the channel resistance between defect-free and ACT-defective FeFETs. When V_g is either too small or too large, both defect-free and defective FeFETs work in the cutoff region or the saturation region [29], resulting in similar channel resistances. However, when FeFETs work in the linear region, the channel resistance changes significantly with V_g increasing, leading to a large gap in channel resistance.

Conventionally, we apply a small V_g in read operations to extract the FeFET channel resistance while avoiding unwanted state switching. If we keep both defective and defect-free FeFETs in LVT (i.e., high resistance) and apply $V_g = 0.1\,\mathrm{V}$ to read the FeFET state, the channel resistance of the defective FeFET is 10 times higher than that of the defect-free one, as presented in Fig. 3 (b). Hence, the ACT defect may cause read/write faults, or lead to FeFET falling into the 'U' state.

5 DEVICE-AWARE FAULT MODELING

In this section, device-aware fault modeling is conducted by examining the impact of the TVS defect at the circuit level.

5.1 Simulation set-up

This work has limited the analysis to single-cell faults. Fault primitive (FP) notations are applied to describe the memory faults [16] (as also in Tab. 1): <S/F/R>, S describes the sensitizing sequence, F describes the faulty effect, and R describes the readout value. For example, <0r0/0/1> denotes a r0 operation on a cell that holds '0' (S=0r0), where the cell remains in its correct state '0' (F=0) yet the read output returns to '1' (R=1) instead of the expected '0'. This FP clarifies how the memory faulty behaviors deviate from expectations. Cadence Spectre is adopted for circuit-level simulations. The simulation circuit consists of 3 x 3 FeFET and the peripheral circuits in Fig. 1 (b).

Table 1: Fault primitive notations

$\langle S/F/R \rangle$	Explanation	Value	
S	Sensitizing sequence	0, 1, $0w0$, $0w1$, $1w0$, $1w1$, $0r0$, $1r1$	
F	Faulty effect	L, 0, U, 1, H	
R	Readout value	0, 1, ?, -	
note in 'F':			
'L'	Extreme low resistance	'1'	Normal low resistance
'U'	Undefined resistance	'0'	Normal high resistance
'H'	Extreme high resistance		
note in 'R':			
'1'	Readout low state	'0'	Readout high state
'?'	Readout random state	'-'	Readout not applicable

5.2 Fault modeling

The fault modeling is performed following three steps: 1) simulation set-up, build the 3×3 FeFET array; 2) replace the central cell from the defect-free one to the ACT-defective one; 3) vary the defect strength (i.e. δ_0), perform all operations in Tab. 1 to the defective FeFET, and observe the related faulty behaviors. The obtained fault models are presented as follows:

Table 2: Fault models

δ_0	Fault	Fault type	δ_0	Fault	Fault type
[0, 0.3)	Fault-free	\	[0.56, 1]	$< 1r1/U/? >$	HtD
[0.3, 0.56)	$< 0w1/U/- >$	HtD		$< 1/U/- >$	
	$< 1w1/U/- >$			$< 1w0/U/- >$	
	$< 1r1/U/? >$			$< 0w0/U/- >$	
	$< 1/U/- >$			$< 0r0/U/- >$	
[0.56, 1]	$< 0w1/U/- >$	HtD		$< 0/U/- >$	
	$< 1w1/U/- >$				

The ACT increases the low channel resistance in logic '1' and decreases the high channel resistance in logic '0'. At the maximum defect strength (i.e., $\delta_0 = 1$), the FeFET state falls into the same 'U' state in both LVT and HVT, and no further changes will occur. Consequently, Hard-to-Detect (HtD) faults are sensitized [18].

5.3 Comparison with conventional fault modeling

Next, we compare the fault models obtained by two methods: 1) modeling defects with linear resistors and 2) applying the DAT method. For example, we model the ACT defect by introducing a resistor path between BL and SL, where the defect strength is represented by the resistance value, as illustrated in Fig. 4 (a) [9]. The fault modeling is performed following the same methodology in Sec. 5.2; all sensitized faults are depicted in the green circle in Fig. 4 (b). Faults obtained by the DAT method are presented in the purple circle. Upon comparison of these circles, no overlap is observed. Similar observations have been noted for faults resulting from other cases when resistors are injected into other positions in Fig. 4 (a), details of which will not be extended here [9]. Therefore, modeling ACT with linear resistors fails to yield accurate fault models, thereby preventing the generation of high-quality test generation.

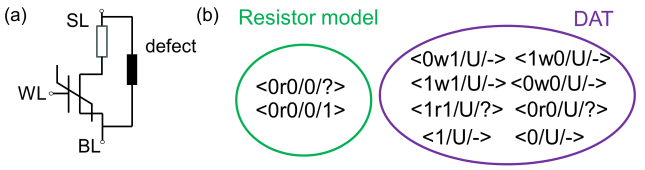

Figure 4: Fault comparison

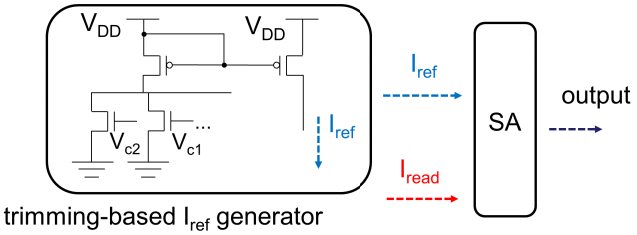

Figure 5: DFT method

6 TEST GENERATION

In this section, we generate test methods based on fault models obtained in the previous section. We first design regular write/read-based tests (i.e., march tests), then design the DfT method.

6.1 March test

We first select the targeted fault; the '$< 1r1/U/? >$' is selected since it sensitizes the largest defect strength range (from 0.3 to 1) (see Tab. 1), and it relates to read operations. Then, we generate the march algorithm to detect this fault:

$$\{\Updownarrow (w1); \Updownarrow (r1)\} \tag{4}$$

The first element initializes all devices to state '1. The second element applies the $r1$ operation and tries to sensitize the fault. Since the 'R' (Readout) of the fault is '?', the feedback of the second element can stochastically be either '0' or '1'. Hence, this march algorithm leads to escapes. By repeating the march algorithm, the detection rate will be increased; yet the escape rate will never reduce to 0, and repeating requires a longer test time.

6.2 DFT method

To improve the fault coverage, it is critical to detect the 'U' state (see Tab. 2). A common DfT structure to detect specific resistance states is the trimming-based circuit [13], as presented in Fig. 5. By selecting different V_{ci}, (i=1, 2, ...), different reference currents (I_{ref}) are generated. The read current (I_{read}) is compared with I_{ref} to evaluate the channel resistance of FeFETs.

The DfT is performed by three steps: 1) post-calibration, select the proper I_{ref}, which the read current when the FeFET channel resistance is at the border of 'U' and '1' state; 2) initialize the FeFETs to '1' state; 3) apply the read operation to compare I_{read} and I_{ref}. The ACT is detected when the FeFET state is in 'U'. This DfT method can guarantee 100% detection of the defect with a high time-efficiency, yet it requires additional chip area for trimming circuits.

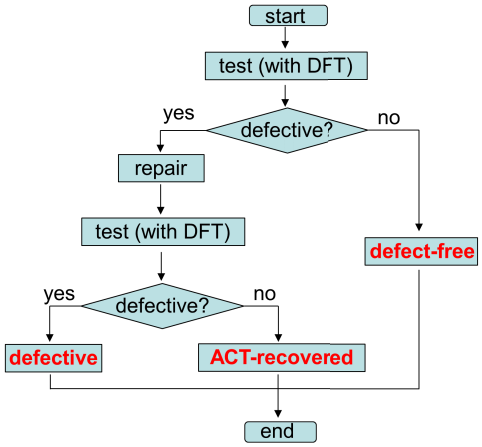

Figure 6: Flow chart of test and repair

6.3 Repair

Considering the nature of ACT defects that may be repaired by a high V_g, we design a complete test and repairing process, as presented in Fig. 6. We first apply the DfT to check if the device is initially defective. If no defects are detected, the device is classified as defect-free. On the other hand, if the device fails the first test process, a high V_g is applied to attempt to repair the device. Then, a second test process the same as the first one is carried out. If the device passes the second test, it is classified as repairable ACT-defective; otherwise, if the device fails, it is classified as defective. However, the actual defect type cannot be diagnosed.

7 DISCUSSION

7.1 Reliability

Charge trapping also affects the reliability of FeFETs [24], with the mechanism close to the hot carrier injection in MOSFETs [30]. For example, repeated write operations on defect-free FeFETs, or repaired ACT-defective FeFETs, can lead to charge trapping and a subsequent reduction in MW. Yet, the structure of the gate stack and the channel material may be different between MOSFETs and FeFETs, hence their charge-trapping-related reliability performance may also be different.

Fig. 7 presents the charge-trapping-related reliability performance of FeFET. The device is defect-free at cycle 0. Charges are injected into the gate stack by repeating write operations, and the MW is gradually reduced from 3 V to 0. Since ACT and the charge-trapping-related reliability issue originate from the same physical mechanism, the ACT defect model can be modified to represent the reliability performance, which will be our future work.

7.2 Comparison between ACT and Stuck-at-Polarization defect

The Stuck-at-Polarization (SaP) defect in FeFETs is described in [8]. It is observed that the SaP-defective and ACT-defective FeFETs show similar electrical performance; yet, the two defects have different physical mechanisms. In Table 3, the properties of the two defects are compared:

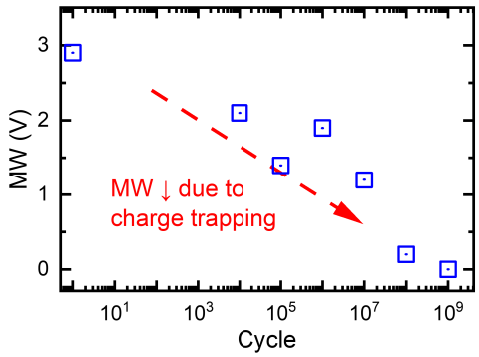

Figure 7: Charge trapping by repeating write operations

Table 3: Comparison of SaP and ACT

	SaP	ACT
Physical origin	Material crystallization imperfection	Electrons injected to SiO_2, spacer, or interface
Related fabrication process	FE layer deposition or Annealing	SiO_2 deposition, spacer deposition, or Annealing
Modeling	Adding parameters to the polarization	Adding parameters to represent the injected electrons
Electrical performance of defective FeFETs	Reduced MW	Reduced MW
If repairable	No	Possible

7.3 Testing of FeFETs in different fields.

This work focuses on the FeFETs operated as binary devices. However, FeFETs are potentially utilized in various applications, such as the CIM system, or operated as the Multi-Level-Cell devices (MLC, reference to MLC-FLASH) [2, 6]. In these scenarios, the ACT defect can have a more significant impact. For example, the outcome of the CIM system is the accumulation of the Analog-to-Digital (ADC) outputs, which relate to the read current of the FeFETs. As a result, even a slight difference in the FeFET channel resistance can accumulate, greatly affecting the outcome. When FeFETs are operated as MLC devices, the channel resistance gaps between different states are less distinct compared to when they are operated as binary devices, implying a small difference in the channel resistance has a larger impact. Hence, detecting the ACT defect in these fields becomes more critical, and test solutions in this work can be configured to these fields.

8 CONCLUSION

This paper applies the DAT method to develop test solutions for the ACT defect in FeFETs. We first introduce the physical mechanism of the ACT defect, and characterize the ACT-defective FeFETs. A specific ACT-defective FeFET model is designed by adjusting or introducing new parameters in the defect-free FeFET model; the model is then calibrated with measurement data. Thereafter, the fault modeling is performed based on circuit-level simulations with the ACT defect model. Test solutions of both the march test and the DfT are proposed to detect ACT.

REFERENCES

[1] J. Müller *et al.*, "Ferroelectric hafnium oxide: A cmos-compatible and highly scalable approach to future ferroelectric memories," in *IEDM*, 2013, pp. 10–8.

[2] H. Mulaosmanovic *et al.*, "Ferroelectric field-effect transistors based on HfO $_2$: A review," *Nanotechnology*, vol. 32, no. 50, p. 502 002, Dec. 2021.

[3] M. Trentzsch *et al.*, "A 28nm HKMG super low power embedded NVM technology based on ferroelectric FETs," San Francisco, CA, USA, Dec. 2016, pp. 11.5.1–11.5.4.

[4] H. Jiao *et al.*, "Ferroelectric field effect transistors for electronics and optoelectronics," *Appl. Phys. Rev.*, vol. 10, no. 1, 2023.

[5] T. Cui *et al.*, "Can interface layer be really free for hf x zr 1-x o 2 based ferroelectric field-effect transistors with oxide semiconductor channel?" *IEEE Electron Device Lett.*, 2024.

[6] S. Sakai *et al.*, "Recent progress of ferroelectric-gate field-effect transistors and applications to nonvolatile logic and FeNAND flash memory," *Materials*, vol. 3, no. 11, pp. 4950–4964, 2010.

[7] D. Chen *et al.*, "Antiferroelectric Phase Evolution in Hf x Zr 1-x O 2 Thin Film Toward High Endurance of Non-Volatile Memory Devices," *IEEE Electr. Device. L.*, vol. 43, no. 12, pp. 2065–2068, 2022.

[8] D. Thapar *et al.*, "Analysis and characterization of defects in fefets," in *ITC*, IEEE, 2023, pp. 256–265.

[9] S. Hamdioui *et al.*, "An experimental analysis of spot defects in srams: Realistic fault models and tests," in *ATS*, 2000, pp. 131–138.

[10] A. Pavlov *et al.*, *CMOS SRAM circuit design and parametric test in nano-scaled technologies: process-aware SRAM design and test*. Springer Science & Business Media, 2008, vol. 40.

[11] A. J. van de Goor *et al.*, "Disturb neighborhood pattern sensitive fault," in *VTS*, 1997, pp. 37–45.

[12] J. Azevedo *et al.*, "A complete resistive-open defect analysis for thermally assisted switching MRAMs," in *IEEE T. VLSI Syst.*, vol. 22, IEEE, 2014, pp. 2326–2335.

[13] C. Münch *et al.*, "MBIST-based Trim-Search Test Time Reduction for STT-MRAM," in *VTS*, 2022, pp. 1–7.

[14] S. Kannan *et al.*, "Sneak-Path Testing of Crossbar-Based Nonvolatile Random Access Memories," *IEEE TN*, vol. 12, no. 3, 2013.

[15] X. Chen *et al.*, "Effect of pinholes in magnetic tunnel junctions," *Appl. Phys. Lett.*, vol. 91, no. 21, 2007.

[16] L. Wu *et al.*, "Electrical Modeling of STT-MRAM Defects," in *ITC*, Phoenix, AZ, USA, Oct. 2018, pp. 1–10.

[17] S. Hamdioui *et al.*, "Device aware test for memory units," 2021.

[18] M. Fieback *et al.*, "Defects, Fault Modeling, and Test Development Framework for RRAMs," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 18, no. 3, pp. 1–26, 2022.

[19] H. Xun *et al.*, "Device-Aware Test for Ion Depletion Defects in RRAMs," in *ITC*, Anaheim, CA, USA, Oct. 2023, pp. 246–255.

[20] S. Yuan *et al.*, "Device-Aware Test for Back-Hopping Defects in STT-MRAMs," in *DATE*, Antwerp, Belgium, Apr. 2023, pp. 1–6.

[21] M. Sachdev *et al.*, *Defect-oriented testing for nano-metric CMOS VLSI circuits*. Springer Science & Business Media, 2007, vol. 34.

[22] T. Soliman *et al.*, "Ultra-Low Power Flexible Precision FeFET Based Analog In-Memory Computing," San Francisco, CA, USA, Dec. 2020, pp. 29.2.1–29.2.4.

[23] M. Ullmann *et al.*, "Disturb free programming scheme for single transistor ferroelectric memory arrays," *Integrated Ferroelectrics*, vol. 34, no. 1-4, pp. 155–164, 2001.

[24] E. Yurchuk *et al.*, "Charge-trapping phenomena in HfO2-based FeFET-type nonvolatile memories," *IEEE T. Electron. Dev.*, vol. 63, no. 9, pp. 3501–3507, 2016.

[25] H. Mulaosmanovic *et al.*, "Ferroelectric FETs With 20-nm-Thick HfO $_2$ Layer for Large Memory Window and High Performance," *IEEE T. Electron. Dev.*, vol. 66, no. 9, pp. 3828–3833, Sep. 2019.

[26] S. Deng *et al.*, "Examination of the interplay between polarization switching and charge trapping in ferroelectric fet," in *IEDM*, IEEE, 2020, pp. 4–4.

[27] K. Ni *et al.*, "A Circuit Compatible Accurate Compact Model for Ferroelectric-FETs," in *VLSI*, 2158-9682, Jun. 2018, pp. 131–132.

[28] B. J. Sheu *et al.*, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE J. Solid-State Circuits*, vol. 22, no. 4, pp. 558–566, 1987.

[29] Y. Taur *et al.*, *Fundamentals of modern VLSI devices*. Cambridge university press, 2021.

[30] E. Takeda *et al.*, "An empirical model for device degradation due to hot-carrier injection," *IEEE Electron Device Lett.*, vol. 4, no. 4, pp. 111–113, 1983.

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