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# Investigation of Dead Time Losses in Inverter Switching Leg Operation: GaN FET vs. MOSFET Comparison

**Vincenzo Barba [1], Salvatore Musumeci [1,*], Fausto Stella [1], Fabio Mandrile [1] and Marco Palma [2,*]**

[1] Energy Department DENERG, Power Electronics Innovation Center PEIC, Politecnico Torino, 10129 Torino, Italy; vincenzo.barba@studenti.polito.it (V.B.); fausto.stella@polito.it (F.S.); fabio.mandrile@polito.it (F.M.)
[2] Efficient Power Conversion Corporation, 10121 Torino, Italy
* Correspondence: salvatore.musumeci@polito.it (S.M.); marco.palma@epc-co.com (M.P.)

**Abstract:** This paper investigates the commutation transients of MOSFET and GaN FET devices in motor drive applications during hard-switching and soft-switching commutations at dead time operation. This study compares the switching behaviors of MOSFETs and GaN FETs, focusing on their performance during dead time in inverter legs for voltage source inverters. Experimental tests at various phase current levels reveal distinct switching characteristics and energy dissipation patterns. A validated simulation model estimates the experimental energy exchanged and dissipated during switching transients. The results demonstrate that GaN FETs exhibit lower overall losses at shorter dead times compared to MOSFETs, despite higher reverse conduction voltage drops. The study provides a quantitative framework for selecting optimal dead times to minimize energy losses, enhancing the efficiency of GaN FET-based inverters in low-voltage motor drive applications. Finally, a dead time optimization strategy is proposed and described.

**Keywords:** motor drive; inverter leg; dead time; switching losses; reverse conduction; GaN FET; MOSFET



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## 1. Introduction

The performance limitations of silicon-based power devices are increasingly evident, moving the semiconductor industry towards alternative materials like silicon carbide (SiC) and gallium nitride (GaN). GaN, in particular, has gained significant traction due to its superior switching speed capabilities [1,2]. Traditional silicon power MOSFETs have faced challenges in balancing conduction and switching losses, as efforts to reduce on-resistance often result in increased parasitic capacitances, leading to higher switching losses [3].

In Pulse-Width Modulation (PWM) motor drive applications, the adoption of GaN technology offers the potential to achieve higher switching frequencies, which in turn reduces torque ripple and improves the waveform quality of the motor current [4]. In a motor drive powered by a voltage source inverter, the dead time is necessary to avoid cross-conduction [5]. Unfortunately, dead time always causes the waveform distortion phenomenon in a motor drive, and dead time compensation strategies are required [6]. Moreover, voltage source inverters used in these applications require dead time to prevent cross-conduction, introducing waveform distortion. This distortion originates from the inherent delays in switching devices and the characteristics of the devices themselves, such as turn-on and turn-off delays and reverse conduction voltage drop [7].

GaN FETs are particularly attractive in power electronics due to their low on-resistance and ability to operate at very high frequencies [8]. For low-voltage (V < 100 V) motor drives, GaN FET-based inverters have demonstrated advantages in reducing the size of passive components and minimizing motor current distortion and torque ripple. On the other hand, an advanced motor insulation layout and a deep investigation of the commutation transient in the inverter leg are required due to the dV/dt increase [9].

Properly setting the dead time is crucial to minimize both reverse conduction [10]. Numerous studies have aimed to optimize dead time settings, exploring solutions like gate driver ICs with adjustable or adaptive dead time capabilities. While some methods, such as programmable dead time settings, lack adaptability in real-world applications [11], others have shown promise but often lack generality or theoretical underpinning [12,13]. Recent research has highlighted the importance of theoretically derived optimal dead time values, which have demonstrated improvements in efficiency [14]. These research studies require a deep knowledge of the considered device behavior, depending on the operative conditions and the technology features [15,16].

This paper investigates the commutation transients of MOSFET and GaN FET devices during dead time for motor drive applications. Experimental tests are conducted in an inverter leg board controlling the phase current. Results reveal different switching behaviors depending on the working conditions. The energy exchanged between the high-side and low-side devices during commutations and the energy losses are estimated through a validated model of the system. The contribution to switching losses during hard-switching and soft-switching commutations and the differences between GaN FET and MOSFET results are distinguished and deeply investigated. Findings aim to provide insights and guidelines for optimizing dead time based on the specific technology for different operating conditions. Furthermore, an optimization strategy for the dead time related to the GaN FET in inverter leg application is presented and described.

## 2. GaN FET and MOSFET Commutation Transients in Motor Drive Application

The motor drive system used consists of a GaN FET-based inverter powering a 3-phase permanent magnet (PM) motor. Figure 1 shows the system composed of the inverter and the electrical machine. The inverter is composed of three legs, one for each motor phase. The stator phase currents $I_a$, $I_b$, $I_c$ are controlled by the high-side $Q_{HS}$ and the low-side $Q_{LS}$ using a Pulse-Width Modulation (PWM). The modulation works at the switching frequency $f_{sw}$, significantly higher than the AC stator phase current frequency of the motor in order to ensure control stability. A dead time ($t_{dt}$) is introduced between the devices' commutation in which both driving signals are off-state. This $t_{dt}$ is set by the user to avoid shoot-through in the inverter leg [17]. Nevertheless, the introduction of $t_{dt}$ creates voltage harmonic distortion affecting the phase current waveform [18,19].

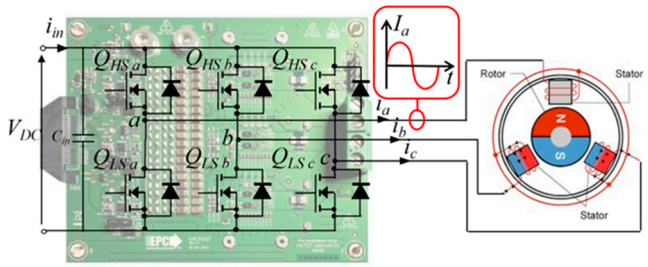


**Figure 1.** A 2-Level inverter using GaN FETs powering a 3-phase AC permanent magnetic motor.

In AC motor drive systems, each inverter leg operates with a sinusoidal phase current of various amplitudes. These currents are directed either from the inverter leg's switching node to the motor phase or in the reverse direction. Figure 1 shows that a current entering the stator phase is considered positive.

To study commutation transients in switching legs with MOSFET and GaN FET devices, we used two half-bridge experimental board PCBs. These boards only differed in device technology. This setup ensured consistent parasitic effects from the PCB, allowing a fair comparison. Nevertheless, the different packages of GaN FET and MOSFET cannot be removed. However, the choice of the technology leads to the use of the corresponding parasitic elements introduced by the case of the selected device [20,21]. Moreover, tests are

carried out using equal operating conditions for both the GaN FET-based board and the MOSFET-based one.

The GaN FET board featured EPC2065 GaN FET, while the MOSFET one featured Onsemi FDMS2D5N08C. The device features are reported in Table 1.

**Table 1.** MOSFET Onsemi FDMS2D5N08C and GaN FET EPC2065 features.

| Parameter | Symbol | MOSFET | GaN FET |
|---|---|---|---|
| Breakdown voltage | $BV_{DSS}$ | 80 V | 80 V |
| Conduction resistance | $R_{Ds,on}$ | 2.7 mΩ | 3.6 mΩ |
| Driving gate voltage | $V_q$ | 10 V | 5 V |

Figure 2a depicts the schematic of the inverter leg. Figure 2b,c show the pictures of the GaN FET board and the MOSFET one, respectively.

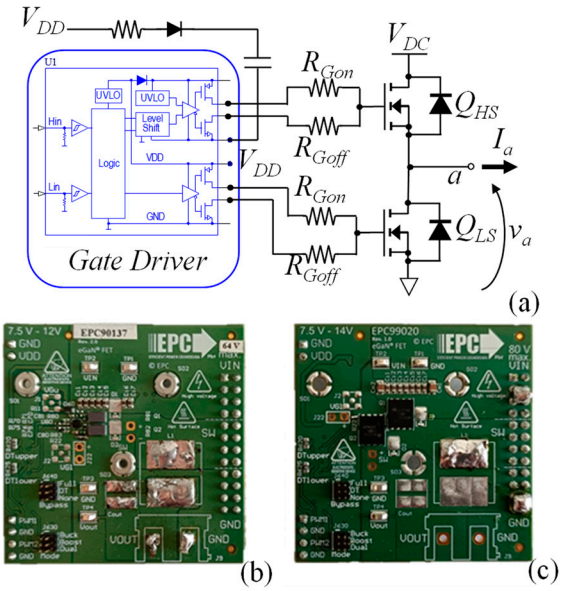


**Figure 2.** (**a**) Electric schematic of the half-bridge boards used for testing the devices. (**b**) GaN FET-based board. (**c**) MOSFET-based board.

Precise measurement results are particularly challenging to obtain, especially when they aim to distinguish different events that happen in a short time (e.g., during the switching transient of WBG devices). Therefore, a dedicated experimental setup controlling the system variables is required [22].

Testing occurred at an ambient temperature of 25 °C with a DC input voltage of $V_{DC} = 48$ V. A second inverter board is used to control the phase current $I_a$ connecting an LCL filter to the half-bridge switching node (point a of Figure 2a). An STM32H7 microcontroller generated PWM signals and controlled the phase current. The PWM operated at a $f_{sw} = 20$ kHz, switching frequency with a duty cycle of 0.1 to reduce current ripple. This $f_{sw}$ is sufficient to ensure that the switching transient has been completed before a new switching. Despite the fact that WBG devices can operate at a higher switching frequency, the $f_{sw}$ selection does not affect the switching transient's investigation [23]. Additionally, $f_{sw} = 20$ kHz is a reasonable settlement for the MOSFET, which operates at a lower $f_{sw}$ than the GaN FET; $t_{dt}$ duration needs to be chosen long enough to prevent shoot-through and obtain hard-switching for commutations with low phase current [24]. Furthermore, significant distortion effects due to the duration of the dead time need to be avoided [25]. In the experimental test, both GaN FET and MOSFET boards have a dead time of $t_{dt} = 150$ ns, which is a good trade-off between the GaN FET and MOSFET

requirements. During $t_{dt}$, transitioning from high-side ($Q_{HS}$) turn-off to low-side ($Q_{LS}$) turn-on can cause zero-voltage transients at different current levels [26].

Experimental tests carried out with $t_{dt} = 150$ ns reveal that the MOSFET switching leg achieves zero voltage switching (ZVS) [27] for currents $I_a \geq 1.5$ A. The GaN FET achieves ZVS at lower $I_a$.

The voltage waveforms are measured using a digital scope featuring a bandwidth of 500 MHz, an output resistance of 10 MΩ, and an output capacitance of 10 pF.

The experimental setup of the controlled current-level system is shown in Figure 3. It includes the half-bridge board under test, the power converter regulating $I_a$, and the STM32H7 microcontroller.

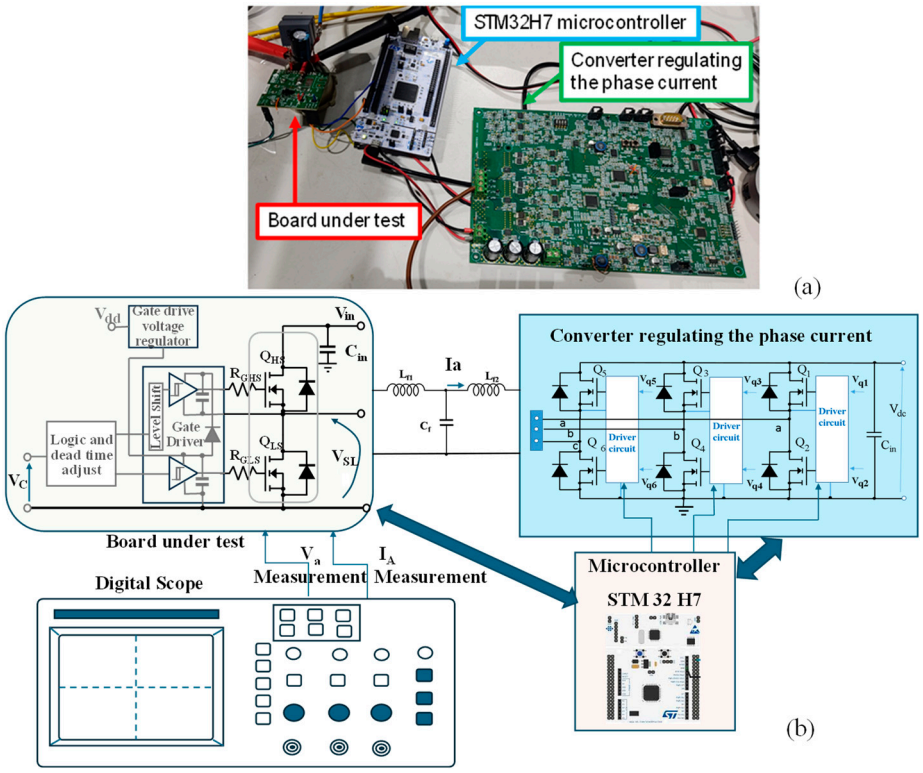


**Figure 3.** Experimental setup made of the half-bridge board under test (GaN FET and MOSFET), the converter imposing the phase current, and the STM32H7 microcontroller. (**a**) Picture of the testing bench, (**b**) block diagram of the experimental setup.

Tests are conducted for positive $I_a$ current values (exiting from the switching node and entering the converter regulating current) at $I_a = 0.5$ A, 1 A, 1.5 A, 2 A, 5 A, 7.5 A, 10 A. Two commutation characteristics for two transitions are analyzed:

- **High-Side Turn-Off, Low-Side Turn-On:** This commutation features a negative voltage slew rate ($dV_a/dt < 0$) as the switching node voltage ($V_a$) decreases;
- **Low-Side Turn-Off, High-Side Turn-On:** This had a positive voltage slew rate ($dV_a/dt > 0$) as the switching node voltage ($V_a$) increased to $V_{DC}$.

The experimental test result achieved in these two commutations for various $I_a$ amplitudes are each reported separately.

### *2.1. Commutation with $dv_a/dt < 0$ and Positive $I_a$*

Figure 4 shows the voltage waveforms measured on the half-bridge boards using GaN FETs and MOSFETs. Figure 4a displays the switching node voltage $V_a$, while Figure 4b illustrates the gate-source voltages for the high-side device ($V_{GS,HS}$) and the low-side device ($V_{GS,LS}$). The $V_a$ waveforms correspond to the current amplitudes $I_a$ indicated by the arrows.

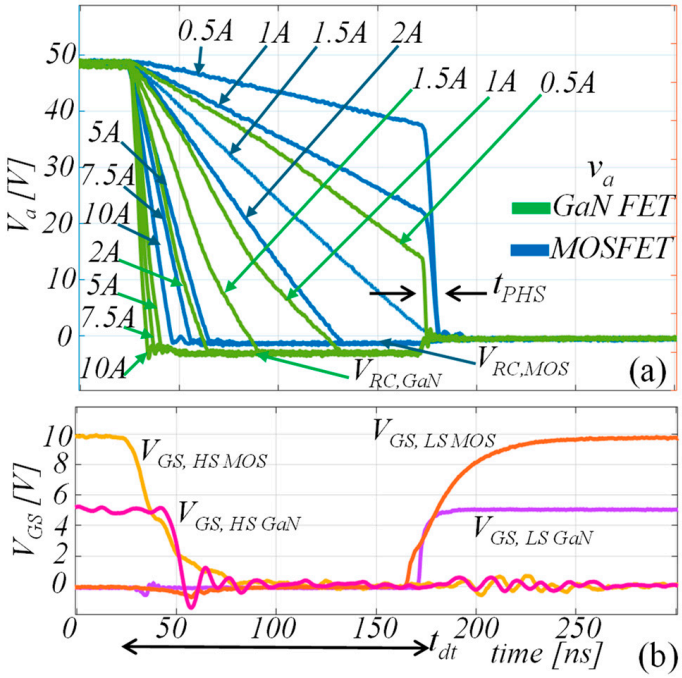


**Figure 4.** Voltages measured on GaN FET and MOSFET during the $Q_{HS}$ turn-off and $Q_{LS}$ turn-on commutation with $I_a > 0$ A ($t_{dt} = 150$ ns). (**a**) Switching node voltage $V_a$. (**b**) Gate-source voltages $V_{GS}$. $V_a = 10$ V/div; $V_{GS} = 2$ V/div; $timestep = 50$ ns/div.

Depending on the $t_{dt}$ length and the $I_a$, three different switching events can happen for the switching node voltage:

- Zero voltage switching (ZVS);
- Voltage variation and partial hard switching (PHS);
- Voltage fall transient and reverse conduction (RC).

When the high-side switch ($Q_{HS}$) turns off, $V_a$ starts to fall. The rate of $V_a$ decline is steeper with higher $I_a$ due to the parasitic output capacitances of the devices ($C_{OSS} = C_{GD} + C_{DS}$) and the load [28]. Since $C_{OSS}$ is not constant with voltage, the dynamics of $V_a$ can be described using an equivalent capacitance $C_{eq}$. This $C_{eq}$ is derived as the average value resulting from the $V_a$ slew rate ($dV_a/dt$) measured at different $I_a$ amplitudes and considering the time ($t_{Vfall}$) taken for $V_a$ to fall to 0 V when $Q_{HS}$ turns off. Integrating the constitutive equation of a capacitance ($I = C \cdot dV/dt$), it is possible to calculate $C_{eq}$ as

$$C_{eq} = \frac{V_{DC}}{t_{Vfall} \cdot I_a} \tag{1}$$

ZVS occurs when the low-side switch ($Q_{LS}$) turns on exactly as $V_a$ reaches 0 V. This is the condition in which $t_{Vfall} = t_{dt}$. As shown in Figure 4, ZVS for MOSFET happens at a phase current amplitude of $I_a = 1.5$ A, while for GaN FET, it occurs between $I_a = 0.5$ A and $I_a = 1$ A. The GaN FET has a lower $C_{OSS} = 750$ pF, compared to the MOSFET's $C_{OSS} = 1800$ pF. The lower $C_{OSS}$ of the GaN FET results in a shorter $t_{Vfall}$, enabling ZVS at lower $I_a$ compared to the MOSFET.

When $I_a$ is lower than the ZVS threshold, a PHS event follows the $V_a$ transient. In this case, $Q_{LS}$ turns on before $V_a$ has fully dropped to 0 V. After $t_{dt}$, $V_a$ falls to $Q_{LS}$'s conduction value within the partial hard switching duration time ($t_{PHS}$), causing PHS losses. Figure 4 shows MOSFET experiencing PHS at $I_a = 0.5$ A and $I_a = 1$ A, while the GaN FET exhibits PHS only at $I_a = 0.5$ A.

In the cases of higher $I_a$ values than those required for ZVS, $V_a$ drops to 0 V before $t_{dt}$ ends $t_{Vfall} < t_{dt}$. Subsequently, $Q_{LS}$ operates in RC mode until $Q_{HS}$ turns on. The reverse

conduction duration is $t_{RC} = t_{dt} - t_{Vfall}$. $V_a$ is negative at $V_a = -V_{RC}$ due to the activation of the body-diode in the MOSFET or the equivalent diode behavior in the GaN FET. The reverse conduction voltage $V_{RC}$ is higher for GaN FET ($V_{RC} = 1.4$ V) than for MOSFET ($V_{RC} = 0.8$ V), causing higher RC losses in the GaN FET than in the MOSFET. No losses follow $t_{dt}$ as $Q_{HS}$ turns on.

In Figure 5a are highlighted $t_{dt}$ and $t_{PHS}$ in the example of the PHS event achieved with the GaN FET with $I_a = 0.5$ A. Figure 5b indicates the time intervals of $t_{Vfall}$ and $t_{RC}$ relative to the $V_a$ curves achieved with $I_a = 2$ A for the GaN FET.

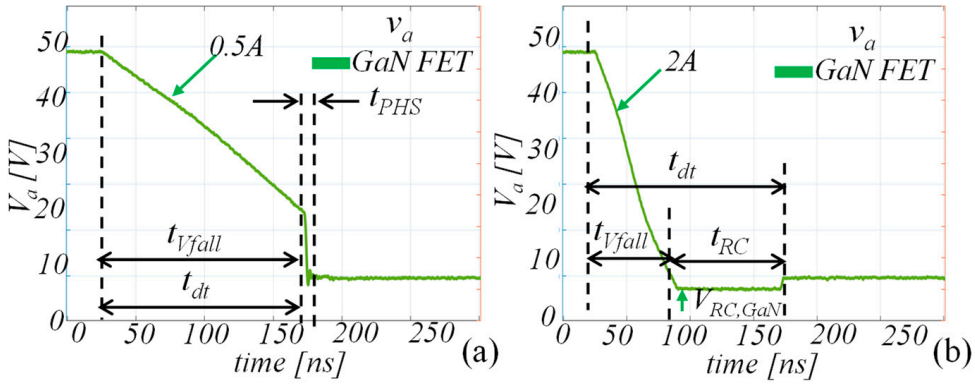


**Figure 5.** Switching node voltages measure on GaN FET during the $Q_{HS}$ turn-off and $Q_{HS}$ turn-on commutation: (**a**) PHS event at $I_a = 0.5$ A; (**b**) RC event at $I_a = 2$ A. $V_a = 10$ V/div; *timestep* $= 50$ ns/div.

### 2.2. Commutation with $dV_a/dt > 0$ and Positive $I_a$

Figure 6 shows voltage waveforms with $dV_a/dt > 0$ for both the half-bridge board using GaN FETs and the one using MOSFETs at the same current variations as in Figure 4. Figure 6a presents the switching node voltage $V_a$, while Figure 6b illustrates the gate-source voltages ($V_{GS,LS}$ for the low-side device and $V_{GS,HS}$ for the high-side device).

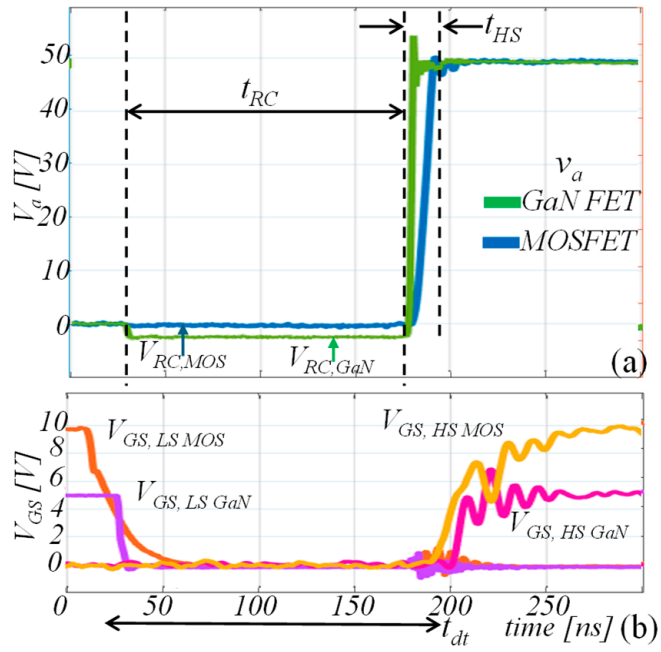


**Figure 6.** Voltages measured on GaN FET and MOSFET during the $Q_{LS}$ turn-off and $Q_{HS}$ turn-on commutation with $I_a > 0$ A ($t_{dt} = 150$ ns). (**a**) Switching node voltage $V_a$. (**b**) Gate-source voltages at the bottom side. $V_a = 10$ V/div; $V_{GS} = 2$ V/div; *timestep* $= 50$ ns/div.

The phase voltage $V_a$ waveforms rise with no differences for all $I_a$ amplitudes used in the tests. The difference in $dV_a/dt$ is determined by the device technology. The parasitic capacitance $C_{OSS}$ of the device affects the voltage rise time $t_{HS}$. The reverse conduction (RC) phase begins when $Q_{LS}$ turns off and ends when $Q_{HS}$ turns on. During RC, $V_a = -V_{RC}$ due to the body-diode of the MOSFET or the equivalent diode in the GaN FET. A hard switching (HS) event follows the dead time, lasting a few nanoseconds, and is a dissipative process because $V_{DS}$ of $Q_{HS}$ equals $V_a = V_{RC} + V_{DC}$.

### 2.3. Commutation with $dV_a/dt < 0$ and Negative $I_a$

The results for negative current are dual to those with positive current. The switching event of $I_a < 0$ A and $dV_a/dt < 0$ is characterized by an RC phenomenon lasting $t_{RC} = t_{dt}$. During RC, $V_a$ reaches the value of $V_a = V_{RC} + V_{DC}$. Consequently, an HS event with a rapid $V_a$ rising happens, and it elapses in lasting a few nanoseconds ($t_{HS}$). All considerations made for $V_a/dt > 0$ and $I_a > 0$ (Section 2.2) are valid.

Figure 7 illustrates $V_a$ measured on the boards with GaN FETs and MOSFET during the commutation with $dV_a/dt < 0$ when testing with $I_a < 0$ A. Figure 7a depicts the falling $V_a$ waveforms, while Figure 7b shows the gate-source voltages for $Q_{LS}$ and $Q_{HS}$ ($V_{GS,LS}$ for the low-side device and $V_{GS,HS}$ for the high-side device).

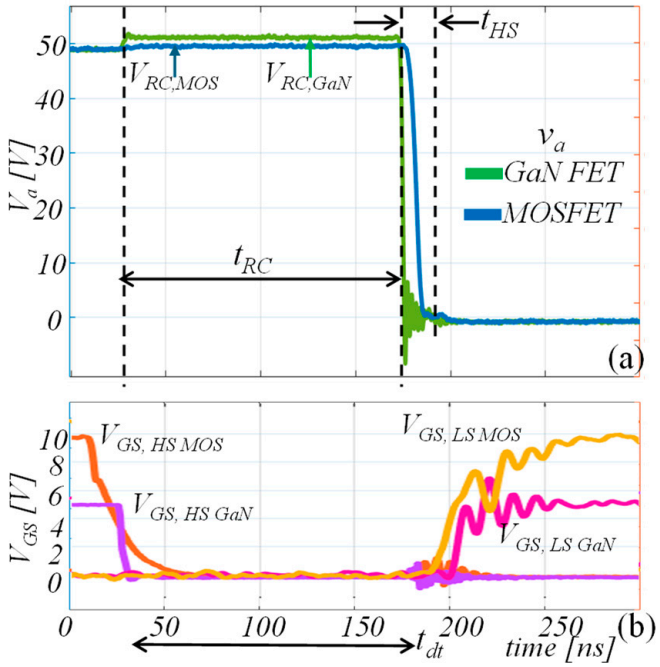


**Figure 7.** Voltages measured on GaN FET and MOSFET during the $Q_{HS}$ turn-off and $Q_{LS}$ turn-on commutation with $I_a < 0$ A ($t_{dt} = 150$ ns). (**a**) Switching node voltage $V_a$. (**b**) Gate-source voltages. $V_a = 10$ V/div; $V_{GS} = 2$ V/div; $timestep = 50$ ns/div.

### 2.4. Commutation with $dV_a/dt > 0$ and Negative $I_a$

For $dV_a/dt > 0$ and $I_a < 0$ A, the commutation dynamics are influenced by the parasitic capacitance. Depending on the amplitude of $I_a$, Zero Voltage Switching (ZVS), Partial Hard Switching (PHS), and Reverse Conduction (RC) events can occur. The same considerations discussed for $dV_a/dt < 0$ and $I_a > 0$ A apply here. At higher $I_a$ amplitudes, the voltage rise time ($t_{Vrise}$) is shorter. Figure 8 shows the voltages measured on GaN FET and MOSFET boards with $I_a = -1.5$ A, $-2$ A, $-5$ A, $-7.5$ A, $-10$ A during commutation with $dV_a/dt > 0$. Figure 8a illustrates the rising $V_a$ waveforms, while Figure 8b presents the gate-source voltages for $Q_{LS}$ and $Q_{HS}$ ($V_{GS,LS}$ and $V_{GS,HS}$, respectively).

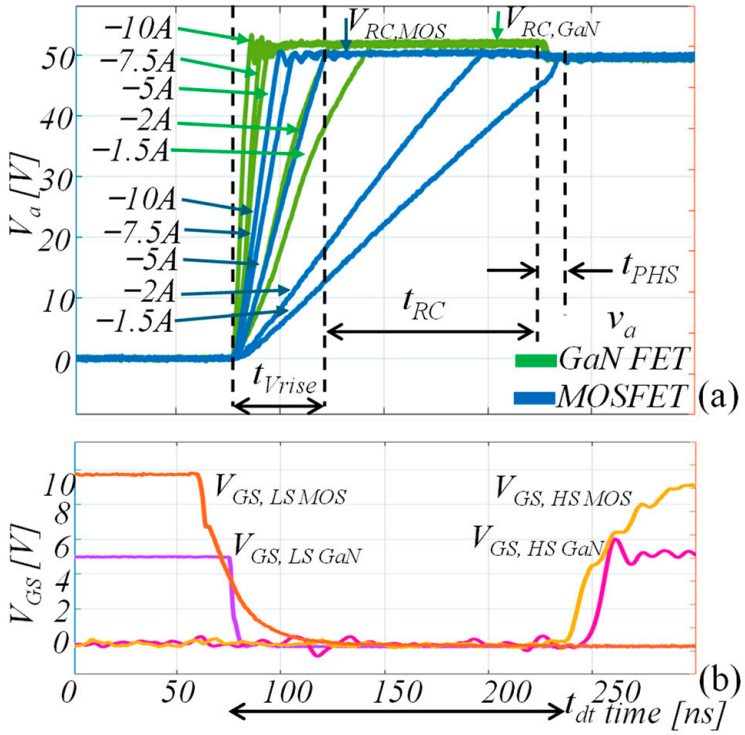


**Figure 8.** Voltages measured on GaN FET and MOSFET during the $Q_{LS}$ turn-off and $Q_{HS}$ turn-on commutation with $I_a < 0$ A ($t_{dt} = 150$ ns). (**a**) Switching node voltage $V_a$. (**b**) Gate-source voltages $V_{GS}$. $V_a = 10$ V/div; $V_{GS} = 2$ V/div; $timestep = 50$ ns/div.

## 3. GaN FET vs. MOSFET Commutation Energy Evaluation

The board used for experimental tests does not incorporate current sensing to measure the current of transistors in a half-bridge configuration. This is intentionally designed to prevent any impact on the switching board's performance. Nevertheless, measuring transistor current is crucial for evaluating power trends and energy during commutations. To achieve the current waveform of devices, LTSpice simulations are used. The simulation models for MOSFET and GaN FET are sourced from the manufacturer's official websites.

The simulated electrical circuit replicates the experimental setup (see Figure 2a) and maintains the same operating conditions: $V_{DC} = 48$ V; $f_{sw} = 20$ kHz and duty-cycle 0.1. The half-bridge circuit model is validated by ensuring it produces waveforms consistent with those obtained in the experimental tests, as depicted in Figures 4 and 6 [29]. The phase currents exiting the switching node (positive $I_a$) in the simulations are $I_a = 0.5$ A, 1 A, 1.5 A, 2 A, 5 A, 7.5 A, 10 A, emulating the experimental conditions.

Simulations are performed twice with dead times $t_{dt} = 20$ ns and $t_{dt} = 150$ ns. These $t_{dt}$ values are typical for the respective devices (20 ns for GaN FETs and 150 ns for MOSFETs) and are relevant for motor drive applications. The energy values computed from the simulations pertain to the low-side device ($Q_{LS}$).

Figures 9 and 10 show the $Q_{LS}$ waveforms of the current $I_{LS}$, the phase voltage $V_a$, and the power $P_{LS}$ during the commutation with $dV_a/dt < 0$, load current of $I_a = 2$ A, and a dead time of $t_{dt} = 20$ ns and with $t_{dt} = 150$ ns, respectively. Figures 9a and 10a refer to the GaN FET, while Figures 9b and 10b refer to the MOSFET.

Comparing the GaN FET waveforms of Figures 9a and 10a with the MOSFET ones in Figures 9b and 10b shows that the $V_a$ and current variations last longer in the MOSFET than in the GaN FET. As a result, during the $V_a$ fall the GaN FET power $P_{GAN}$ has a peak comparable with those of the MOSFET $P_{MOS}$, but $P_{GAN}$ lasts shorter. In the case of soft switching following the $V_a$ fall in Figure 9a,b, GaN FET features a higher reverse conduction voltage drop ($V_{RC}$). The current flowing through the device operating in reverse conduction is $I_a$ and it is equal for both the GaN FET or the MOSFET. Therefore, the higher $V_{RC}$ of

the GaN FET leads to higher reverse conduction losses than the MOSFET [30]. Due to the higher voltage drop of the GaN transistor during reverse conduction operation, the device in the third quadrant must work with reduced timing to optimize performance and losses. In the hard-switching event with $I_a = 2$ A and $t_{dt} = 20$ ns shown in Figure 10a,b, the overall GaN FET hard switching losses are much lower than the MOSFET ones.

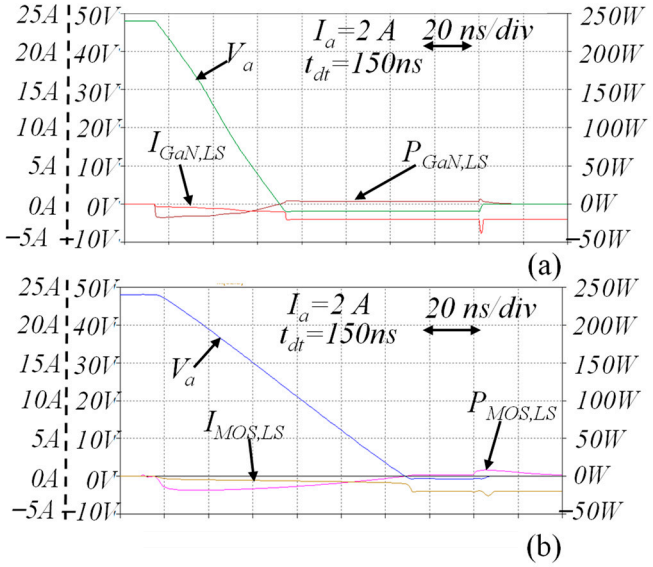


**Figure 9.** Waveforms of the commutation with $I_a = 2$ A, $t_{dt} = 150$ ns, and $dV_a/dt < 0$. (**a**) GaN FET $I_{GaN} = 10$ A/div; $V_a = 10$ V/div; power $P_{GaN}$ = 25 W/div. (**b**) MOSFET $I_{MOS} = 10$ A/div; $V_a = 10$ V/div; power $P_{MOS}$ = 25 W/div. *timestep* = 20 ns/div.

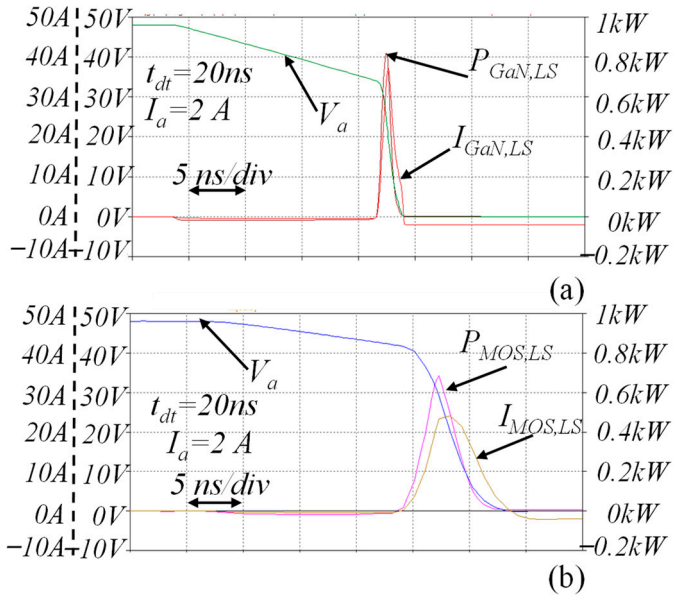


**Figure 10.** Waveforms of the commutation with $I_a = 2$ A, $t_{dt} = 20$ ns, and $dV_a/dt < 0$. (**a**) GaN FET $I_{GaN} = 10$ A/div; $V_a = 10$ V/div; power $P_{GaN}$ = 200 W/div. (**b**) MOSFET $I_{MOS} = 10$ A/div; $V_a = 10$ V/div; power $P_{MOS}$ = 200 W/div. *timestep* = 5 ns/div.

During the commutation exhibiting $dV_a/dt < 0$ ($Q_{HS}$ turning off and $Q_{LS}$ turning on) with a positive $I_a$, it is possible to distinguish between the $I_a$ amplitudes that result in ZVS

or RC and those that cause PHS. The energy of $Q_{LS}$ during the voltage variation, $E_{VV}$, is determined by the equation:

$$E_{VV} = \int_0^{t_{Vfall}} |V_a \cdot I_{LS}| \cdot dt \quad (2)$$

where $I_{LS}$ is the current through $Q_{LS}$ and $t_{Vfall}$ is the time taken for the switching node variation $V_a$. The time $t_{Vfall}$ varies according to the $V_a$ falling slew rate. If $V_a$ drops to 0 V before the end of $t_{dt}$, RC conditions appear. ZVS condition appears when $t_{Vfall}$ equals the maximum value of $t_{dt}$ if $V_a$ reaches 0 V at the end of $t_{dt}$. The PHS conditions occur if the theoretical voltage fall time $t_{Vfall}$ exceeds $t_{dt}$. When $t_{Vfall}$ is followed by RC conditions lasting $t_{RC}$, the energy losses during $t_{dt}$ are denoted as $E_{RC}$ and calculated as

$$E_{RC} = \int_{t_{Vfall}}^{t_{Vfall}+t_{RC}} |V_{RC} \cdot I_{LS}| \cdot dt \quad (3)$$

where $t_{RC}$ is the RC time interval when $V_a$ is negative and equal to $V_a = -V_{RC}$ for the GaN FET or MOSFET. The upper integral limit at $t = t_{Vfall} + t_{RC}$ is close to $t_{dt}$ and includes turn-on delays of $Q_{LS}$ and the driving circuit's propagation delay uncertainty.

If $V_a$ does not drop to 0 V within $t_{dt}$, the voltage variation during $t_{Vfall} = t_{dt}$ is followed by PHS. The energy losses due to the PHS $E_{PHS}$ are calculated as

$$E_{PHS} = \int_{t_{dt}}^{t_{dt}+t_{PHS}} |V_a \cdot I_{LS}| \cdot dt \quad (4)$$

where $t_{PHS}$ is the duration of the PHS phenomenon, starting at the end of $t_{dt}$ and ending as $I_{LS} = 0$ A.

In the ZVS condition, $E_{RC} = 0$ J and $E_{PHS} = 0$ J. $E_{VV}$ is the only energy involved in the switching event.

Figures 11 and 12 illustrate the energies involved during the $Q_{HS}$ turn-off and $Q_{LS}$ turn-on with positive $I_a$ from 0.5 A to 10 A. Figure 11 refers to results with $t_{dt} = 20$ ns, while Figure 12 refers to those achieved with $t_{dt} = 150$ ns. In particular, Figures 11a and 12a depict the energy $E_{VV}$ as a function of $I_a$. On the other hand, Figures 11b and 12b show the energy losses due to RC ($E_{RC}$) and PHS ($E_{PHS}$) as a function of $I_a$. ZVS is marked with a dashed line, while PHS and RC are marked with dotted lines. MOSFET curves are blue, and GaN FET curves are green.

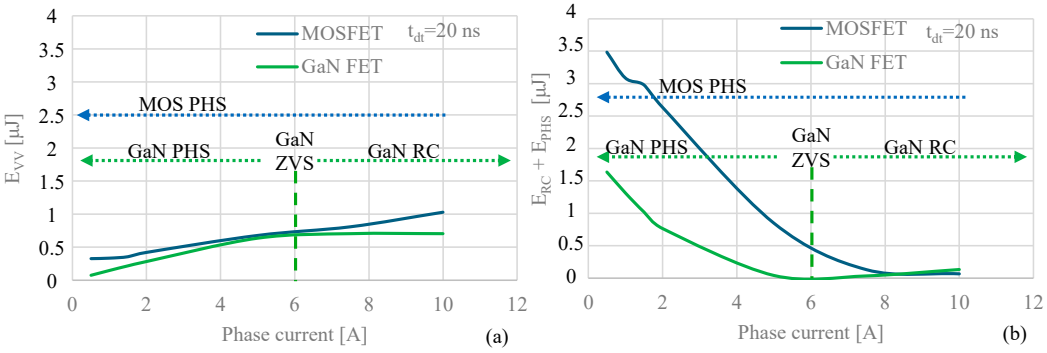


**Figure 11.** Energies of $Q_{LS}$ (MOSFET in blue and GaN FET in green) versus phase current during the commutation with $I_a > 0$ A and $dV_a/dt < 0$ using $t_{dt} = 20$ ns. (**a**) Energy of voltage variation; (**b**) PHS and RC energies. ZVS event is highlighted with a dashed line. PHS and RC are highlighted with dotted lines. $E = 0.5$ µJ/div; $I_a = 2$ A/div.

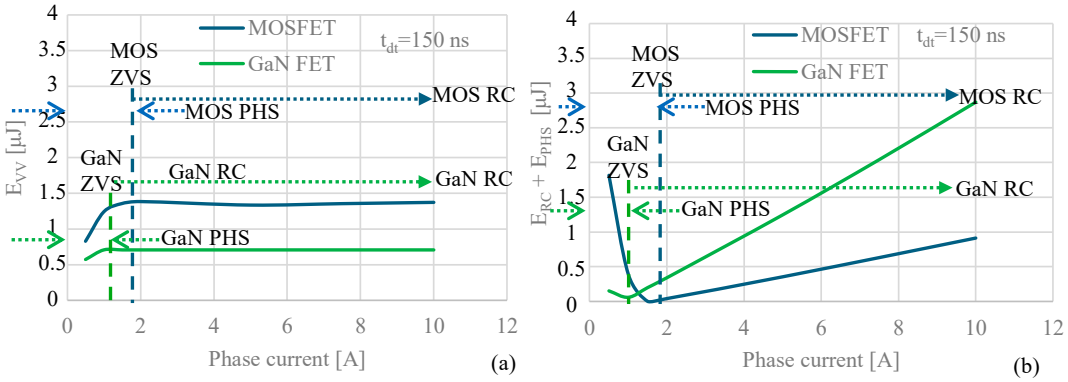


**Figure 12.** Energies of $Q_{LS}$ (MOSFET in blue and GaN FET in green) versus phase current during the commutation with $I_a > 0$ A A and $dV_a/dt < 0$ using $t_{dt} = 150$ ns. (**a**) Energy of voltage variation; (**b**) PHS and RC energies. ZVS event is highlighted with a dashed line. PHS and RC are highlighted with dotted lines. $E = 0.5$ µJ/div; $I_a = 2$ A/div.

GaN FET achieves ZVS at $I_a = 6$ A with $t_{dt} = 20$ ns and at $I_a = 0.8$ A with $t_{dt} = 150$ ns. Differently, the MOSFET achieves ZVS at $I_a = 1.5$ A with $t_{dt} = 150$ ns, while it does not achieve ZVS with $t_{dt} = 20$ ns for currents up to $I_a = 10$ A. RC losses occur for $I_a$ higher than the one causing ZVS, while PHS occurs for $I_a$ lower than the ZVS.

Commutation with $dV_a/dt < 0$ starts with the initial conditions of $C_{OSS,LS}$ of $Q_{LS}$ charged to $V_{DC}$ and $C_{OSS,HS}$ of $Q_{HS}$ discharged to nearly 0 V. Immediately after turning off $Q_{HS}$, $C_{OSS,LS}$ of $Q_{LS}$ discharges to 0 V and $C_{OSS,HS}$ of $Q_{HS}$ charges to $V_{DC}$. During this, both devices are in the off-state, but the variation of $V_a$ causes an exchange of energy $E_{VV}$ between them. The amount of $E_{VV}$ exchanged varies depending on the switching event:

- ZVS or RC: $C_{OSS,LS}$ of $Q_{LS}$ discharges of $E_{VV}$ until $V_a$ stabilizes at 0 V, while $C_{OSS,HS}$ of $Q_{HS}$ charges of $E_{VV}$ up to $V_{DC}$. $E_{VV}$ is maximum ($E_{VVmax}$) since $C_{OSS,LS}$ of $Q_{LS}$ fully discharges using the charging energy of $C_{OSS,HS}$ of $Q_{HS}$. $E_{VVmax}$ is calculated as

$$E_{VV\ max} = \frac{1}{2} \cdot C_{eq} \cdot V_{DC}^2 \tag{5}$$

and looking at Figures 11a and 12a, $E_{VVmax} \approx 0.75$ µJ for GaN FET and $E_{VVmax} \approx 1.5$ µJ for MOSFET.

- PHS: $C_{OSS,LS}$ of $Q_{LS}$ does not discharge completely because after $t_{dt}$ the phase voltage is not null, $V_a > 0$ V. $C_{OSS,HS}$ of $Q_{HS}$ charges of $E_{VV} < E_{VV\ max}$, and $C_{OSS,LS}$ of $Q_{LS}$ does not fully charge to $V_a = V_{DC}$. GaN FET's smaller $C_{OSS}$ results in a steeper $V_a$ fall and a shorter $t_{Vfall}$ for exchanging $E_{VV}$. As a result, MOSFET features a greater quantity of $E_{PHS}$ losses than the GaN FET when using the same $t_{dt}$.

ZVS condition features zero energy losses $E_{RC} + E_{PHS} = 0$ J. Only $E_{VV}$ is involved due to the energy exchange between the switching leg devices' output capacitances ($C_{OSS,HS}$ and $C_{OSS,LS}$). Differently, PHS and RC are dissipative phenomena following $t_{Vfall}$ (Figures 11b and 12b).

Considering the same $I_a$, PHS energy losses $E_{PHS}$ is lower with long $t_{dt}$ because $Q_{LS}$ turns on with a lower $V_{DS} = V_a > 0$ V (closer to ZVS). Additionally, elapsed $t_{dt}$, GaN FET's smaller $C_{OSS}$ results in a steeper $V_a$ fall than MOSFET, leading to lower $E_{PHS}$ for GaN FET. On the other hand, MOSFET features a lower voltage drop $V_{RC}$ and corresponding losses $E_{RC}$ than the GaN FET. $E_{RC}$ increase proportionally with $t_{dt}$ and $I_a$ whatever the technology is considered.

Figures 13 and 14 show the GaN FET and MOSFET waveforms of the $Q_{LS}$ current $I_{LS}$, the phase voltage $V_a$ and the device power $P_{LS}$ during the commutation with $dV_a/dt > 0$. Additionally, Figures 13a and 14a show the GaN FET power $P_{GaN}$, while Figures 13b and 14b depict the MOSFET reverse recovery current and the body-diode

power, respectively. In particular, Figure 13 refers to the case with $I_a = 2$ A and Figure 14 to $I_a = 7.5$ A.

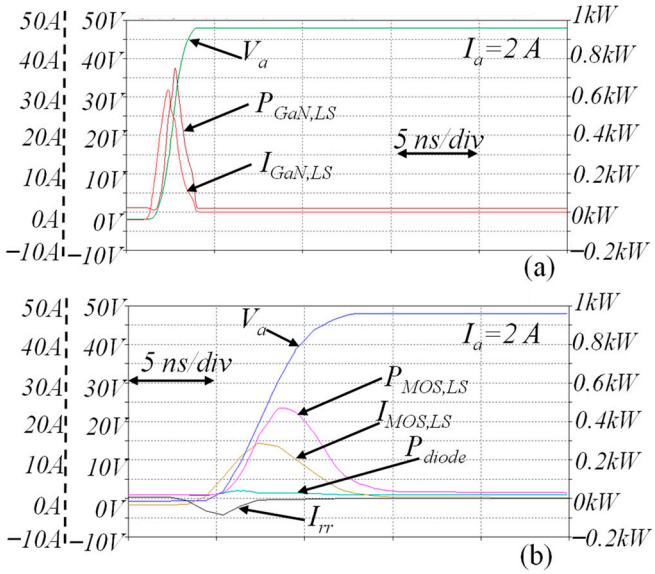


**Figure 13.** Waveforms of the commutation with $I_a = 2$ A and $dV_a/dt > 0$. (**a**) GaN FET $I_{GaN} = 5$ A/div; $V_a = 5$ V/div; power $P_{GaN} = 100$ W/div. (**b**) MOSFET $I_{MOS} = 5$ A/div; $V_a = 5$ V/div; power $P_{MOS} = 100$ W/div; reverse recovery current $I_{rr} = 5$ A/div; body-diode power $P_{diode} = 100$ W/div. *timestep* = 5 ns/div.

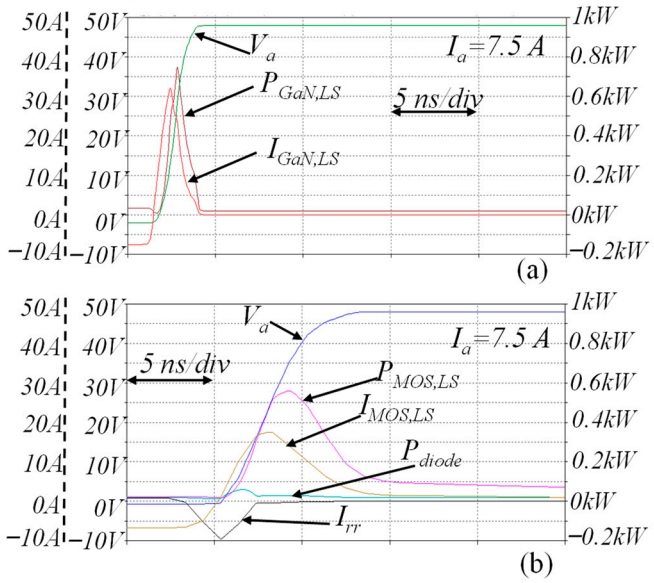


**Figure 14.** Waveforms of the commutation with $I_a = 7.5$ A and $dV_a/dt > 0$. (**a**) GaN FET $I_{GaN} = 5$ A/div; $V_a = 5$ V/div; power $P_{GaN} = 100$ W/div. (**b**) MOSFET $I_{MOS} = 5$ A/div; $V_a = 5$ V/div; power $P_{MOS} = 100$ W/div; reverse recovery current $I_{rr} = 5$ A/div; body-diode power $P_{diode} = 100$ W/div. *timestep* = 5 ns/div.

During commutation with $dV_a/dt > 0$ ($Q_{LS}$ turn off and $Q_{HS}$ turn on), the transient event starts with the $C_{OSS,LS}$ of $Q_{LS}$ being discharged, and $C_{OSS,HS}$ of $Q_{HS}$ being charged to $V_{DC}$. With positive $I_a$, $Q_{LS}$ works in reverse conduction for all $t_{dt}$. At the end of $t_{dt}$, $Q_{HS}$ turns on with a drain-source voltage of $V_a = V_{DC}$, causing hard switching (HS). The device $Q_{LS}$ has a current peak and an almost instantaneous $C_{OSS,LS}$ charge.

GaN FET waveforms in Figures 13a and 14a exhibit negligible differences with the $I_a$ level. Furthermore, GaN FET shows a faster dynamic than the MOSFET one of

Figures 13b and 14b because of the low GaN FET $C_{OSS}$. Additionally, MOSFET features a reverse recovery current $I_{rr}$ due to the body-diode which causes an increase of $P_{diode}$ in switching losses $P_{MOS}$. A higher $I_a$ leads to a higher $I_{rr}$ peak and higher $P_{diode}$, as shown comparing Figures 13b and 14b. GaN FET does not feature reverse recovery current and corresponding losses. The $I_{GaN}$ peak is due only to the charging $C_{OSS}$.

The reverse conduction energy $E_{RC}$ achieved by $Q_{LS}$ both for GaN FET and MOSFET is illustrated in Figures 15a and 16a as a function of $I_a$. Figures 15b and 16b depict the hard switching energy losses ($E_{HS}$) as a function of $I_a$. Figure 15 refers to the case with $t_{dt} = 20$ ns, while Figure 16 refers to the one with $t_{dt} = 150$ ns. GaN FET curves are depicted in green, while MOSFET curves are shown in blue.

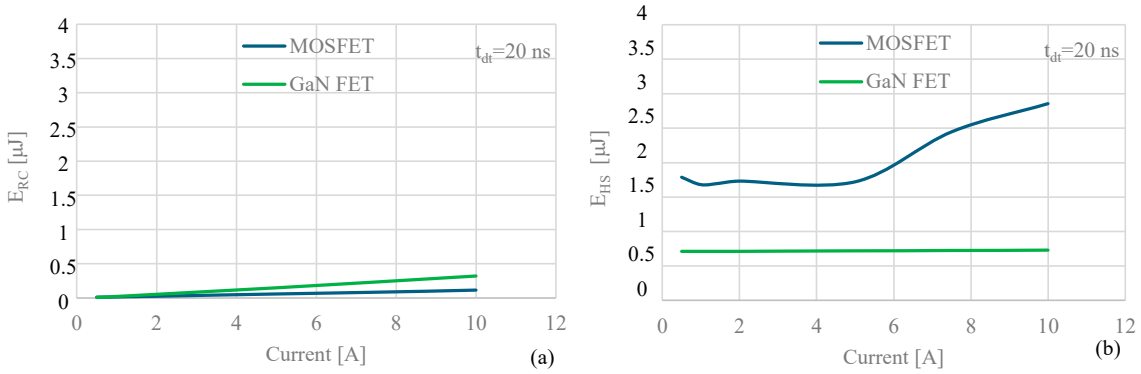


**Figure 15.** Energies of $Q_{LS}$ (MOSFET in blue and GaN FET in green) versus phase current $I_a$ during the commutation with $I_a > 0$ A and $dV_a/dt < 0$ using $t_{dt} = 20$ ns. (**a**) Energy dissipation for reverse conduction $E_{RC}$; (**b**) Energy dissipation for hard switching $E_{HS}$. $E = 0.5$ µJ/div; $I_a = 2$ A/div.

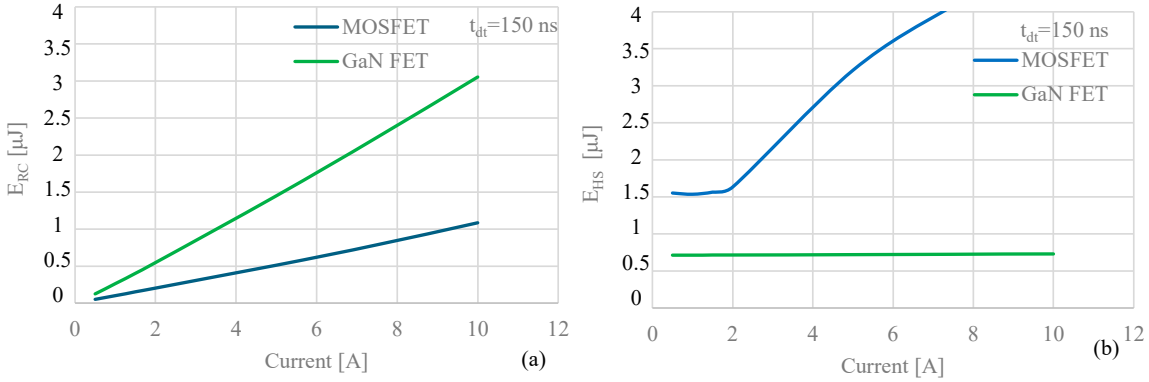


**Figure 16.** Energies of $Q_{LS}$ (MOSFET in blue and GaN FET in green) versus phase current $I_a$ during the commutation with $I_a > 0$ A and $dV_a/dt < 0$ using $t_{dt} = 150$ ns. (**a**) Energy dissipation for reverse conduction $E_{RC}$; (**b**) Energy dissipation for hard switching $E_{HS}$. $E = 0.5$ µJ/div; $I_a = 2$ A/div.

The comparison of the GaN FET and MOSFET $E_{RC}$ curves in Figures 15a and 16a demonstrates that GaN FET losses are higher than MOSFET during $t_{RC}$ due to higher $V_{RC}$ [30]. Despite this, $E_{RC}$ losses are significantly low (up to 0.3 µJ for GaN FET and 0.1 µJ for MOSFET) considering $t_{dt} = 20$ ns. $E_{RC}$ increases linearly with $t_{dt}$ and the level of $I_a$.

Figures 15b and 16b show that HS energy losses $E_{HS}$ of GaN FET are significantly lower than the MOSFET ones. GaN FET features a $E_{HS} = 0.75$ µJ regardless of $t_{dt}$ and $I_a$. Differently, MOSFET, and $E_{HS}$ has a minimum $E_{HSmin} = 1.5$ µJ for low $I_a$ levels which persist according to $t_{dt}$ duration: $I_a < 6$ A for $t_{dt} = 20$ ns and $I_a < 2$ A for $t_{dt} = 150$ ns.

$E_{HSmin}$ corresponds to the energy required to charge the $C_{OSS,LS}$ of $Q_{LS}$ to $V_{DC}$ (no energy comes from $C_{OSS,HS}$ of $Q_{HS}$) and it is calculated as

$$E_{HS\ min} = \frac{1}{2} \cdot C_{eq} \cdot V_{DC}^2 \tag{6}$$

where $C_{eq}$ is the constant equivalent value of $C_{OSS}$ (which is a non-linear parameter with the voltage). $E_{HSmin}$ is not affected by $t_{dt}$ and closely matches the maximum energy capacity of $C_{OSS}$ ($E_{VVmax}$), as arises comparing in Figures 12a and 16b.

When $I_a$ level is higher, $E_{HS}$ of the MOSFET grows with the $I_a$ amplitude, while the GaN FET one remains constant. The MOSFET $E_{HS}$ increase is due to the additional reverse recovery charge $Q_{rr}$ in the MOSFET's P-N junction, which grows with longer $t_{dt}$ and higher reverse recovery current $I_{rr}$ [31,32]. Conversely, the GaN FET maintains a constant $E_{HS} = E_{HSmin}$ due to the absence of a P-N junction, thereby featuring $Q_{rr} = 0$ nC [33]. In general, $E_{HS}$ significantly exceeds $E_{RC}$, particularly at $t_{dt} = 20$ ns. When considering both energy dissipation components, the GaN FET exhibits reduced energy losses during the switching transient, especially with a shorter dead time ($t_{dt} = 20$ ns).

## 4. Dead Time Reduction Strategy

A reduction switching losses strategy can be developed acting on the dead time length. In particular, it is aimed to set the dead time differently for the switching events of $dV_a/dt < 0$ ($Q_{HS}$ turn off and $Q_{LS}$ turn on) and $V_a/dt > 0$ ($Q_{LS}$ turn off and $Q_{HS}$ turn on), according to the load current sign:

1. $I_a > 0$ A
   a. $dV_a/dt > 0$: set $t_{dt} = t_{dt,min}$
   b. $dV_a/dt < 0$: set $t_{dt} = t_{dt,opt}$
2. $I_a < 0$ A
   c. $dV_a/dt > 0$: set $t_{dt} = t_{dt,opt}$
   d. $dV_a/dt < 0$: set $t_{dt} = t_{dt,min}$

Where $t_{dt,min}$ is the minimum dead time which ensures a safe switching event according to the gate propagation delay uncertainty; $t_{dt,opt}$ is the optimum dead time minimizing the reverse conduction duration. Furthermore, in motor drive applications, it may be useful to maintain $t_{dt,opt}$ between a maximum value $t_{dt,max}$ and the minimum $t_{dt,min}$. The dead time $t_{dt,max}$ is chosen according to the maximum admissible hard-switching losses and avoids increasing the total harmonic distortion (THD) in the phase motor current [33,34].

### *4.1. Operation with Constant Minimum Dead Time Conditions*

When turning on GaN FET HS with a $I_a > 0$ A, case a, (see Figure 6) and GaN FET LS with $I_a < 0$ A, case d, (see Figure 7), reverse conduction phenomenon persists for all the dead time duration, regardless of the $I_a$ amplitude. Reverse conduction is minimized by simply setting the minimum $t_{dt}$ duration ($t_{dt,min}$). The $t_{dt} = t_{dt,min}$ condition can be enabled after having monitored the $I_a$ sign and applied only for the turn-on transient of the corresponding GaN FET: HS turns on when $I_a > 0$ A; LS turns on when $I_a < 0$ A.

### *4.2. Operation with Reduced Dead Time Conditions*

The control strategy for turning on GaN FET LS when $I_a > 0$ A, case b, (see Figure 4), or GaN FET HS when $I_a < 0$ A, case c, (see Figure 8) requires a preliminary estimation of the optimum dead time $t_{dt,opt}$. A comparator is used to monitor the drain-source voltage $V_{DS}$ of the GaN FET to turn on, as depicted in the circuit schematic of Figure 17a. A constant reference voltage $V_{refON}$ is set as a threshold. The comparator compares $V_{DS}$ with a threshold reference value $V_{refON}$. The dead time control block in Figure 17a generates the driving signal $V_q$ when $V_{DS}$ falls below $V_{refON}$, as shown in Figure 17b. Additionally, a maximum dead time value $t_{dt,max}$ in the dead time control block is considered [35].

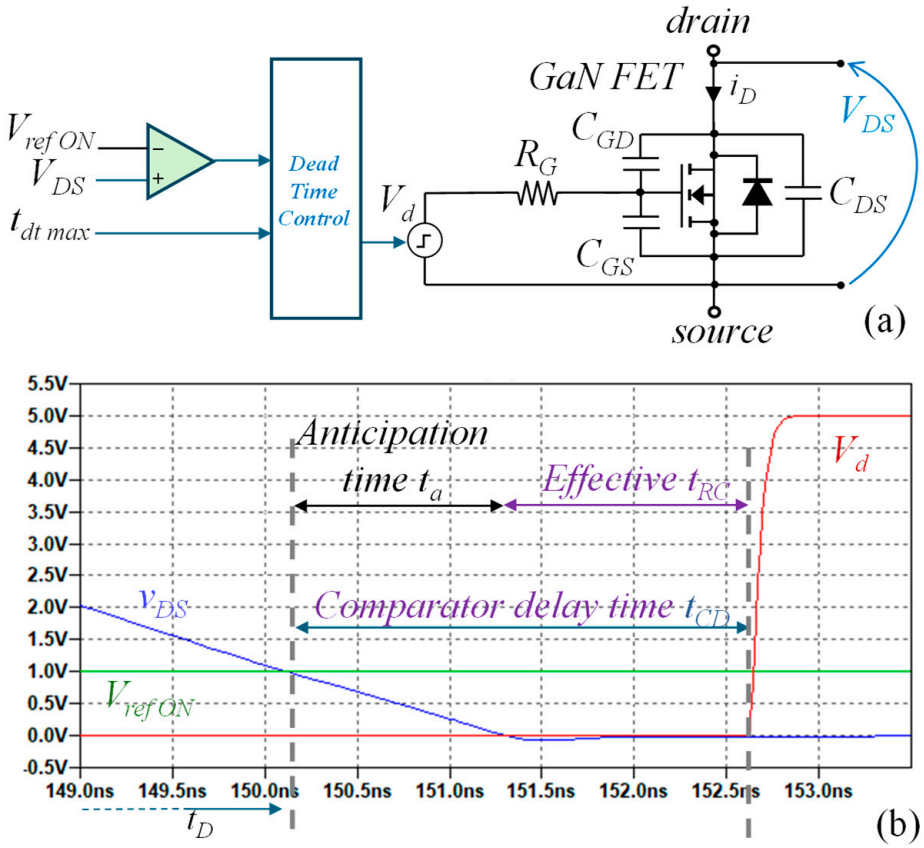


**Figure 17.** (**a**) $v_{DS}$ comparison and $t_{dt,max}$ entering the dead time control strategy for dead time reduction. (**b**) Choice of $V_{refON}$ for $v_{DS}$ comparison. $V = 0.5$ V/div. $timestep = 5$ ns/div.

If $V_{DS} < V_{refON}$ is not triggered within the maximum dead time $t_{dt,max}$, the turn-on signal is generated regardless of the comparator output (the dead time is fixed and equal to $t_{dt,max}$).

In Figure 17b, $t_d$ represents the turn-on driving time which corresponds to the time when the condition $V_{DS} = V_{refON}$ is triggered. The threshold $V_{refON}$ is chosen according to the highest $I_a$ amplitude that does not cause reverse conduction within $t_{dt,max}$. This condition is equivalent to ZVS with $t_{dt} = t_{dt,max}$. $V_q$ generation can be anticipated by the comparator delay time $t_{cd}$. $V_{refON}$ is set equal to the value of $V_{DS}$ when $t_D = t_{dt,max} - t_{cd}$.

This approach ensures that the turn-on signal is sent only when the voltage variation has been completed, thereby minimizing reverse conduction. The commutation behavior is thus adapted to the current amplitude, differing from constant dead time methods.

### *4.3. Validation in Motor Drive Setup*

For instance, the presented dead time reduction strategy is developed in a GaN FET-based inverter board supplying a BLDC motor (nominal voltage of 36 V, nominal power of 250 W, and 26 pole pairs). A maximum dead time of $t_{dt,max} = 100$ ns and a minimum of $t_{dt,min} = 20$ ns are selected. At the time $t_{dt,max} = 100$ ns the $I_a$ current in ZVS is 1.2 A. For the phase current below 1.2 A, the PHS condition appears. This $t_{d,mx}$ value choice is a trade-off between the quality of the sinusoidal output current and reduced energy losses during the partial hard switching conditions ($E_{PHS}$ contribute).

The $V_a$ waveforms measured for $I_a = 1.2$ A, 1.6 A, 2.5 A, 4 A, 6 A utilizing the dead time reduction strategy are shown in Figure 18a for commutations with $dV_a/dt < 0$ and in Figure 18b for commutations with $dV_a/dt > 0$.

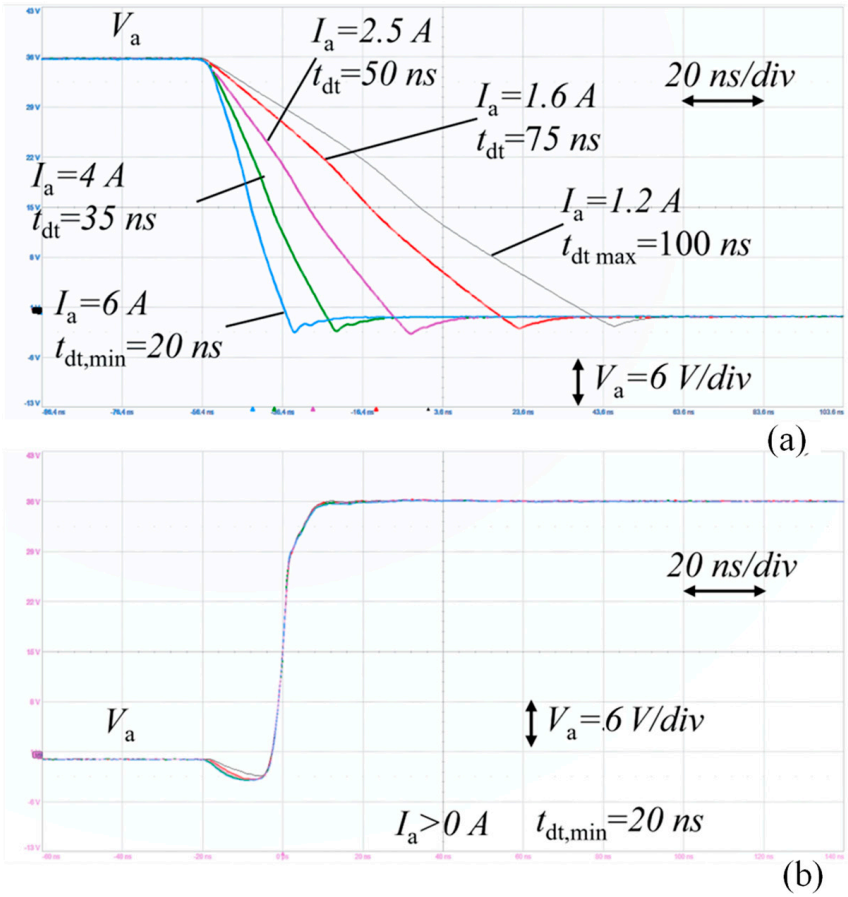


**Figure 18.** $V_a$ waveforms measured for $I_a$ = 1.2 A, 1.6 A, 2.5 A, 4 A, 6 A utilizing the dead time reduction strategy. (**a**) $dV_a/dt < 0$; (**b**) $dV_a/dt > 0$; $V_a$ = 5 V/div. $timestep$ = 20 ns/div.

The $V_a$ voltage fall in Figure 18a shows that with higher $I_a$ it is possible to minimize the reverse conduction phenomenon shortening the dead time. Moreover, for $I_a < 1.2$ A the dead time is maximum $t_{dt,max} = 100$ ns, while for $I_a > 6$ A the dead time is minimum $t_{dt,min} = 20$ ns. On the other hand, in Figure 18b, when $V_a$ rises with $I_a > 0$ A, the dead time is minimum $t_{dt,min} = 20$ ns independently from the $I_a$ amplitude.

## 5. Conclusions

This paper presents a comprehensive investigation into the commutation transients of MOSFET and GaN FET devices in motor drive applications, with a focus on hard-switching and soft-switching commutations. Through experimental tests and validated simulations, the study reveals distinct differences in switching behaviors and energy dissipation patterns between MOSFETs and GaN FETs. The key findings highlight that GaN FETs exhibit significantly lower overall losses at shorter dead times compared to MOSFETs, despite a higher reverse conduction voltage drop. Additionally, the lower output parasitic capacitance of GaN FETs contributes to faster commutations and reduced energy losses.

These insights provide a quantitative framework for optimizing dead time duration to minimize energy losses in GaN FET-based low-voltage inverters for motor drive applications. Furthermore, a strategy to optimize the dead time choice for the different operative conditions in the inverter leg is presented and described. The proposed strategy for dynamically adjusting dead time based on load conditions shows potential for further reducing commutation losses and enhancing inverter efficiency. Future research will focus on developing algorithms to adapt dead time duration in real-time, thereby optimizing performance and reducing energy consumption in motor drive systems.

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**Data Availability Statement:** Data are contained within the article.

**Conflicts of Interest:** Author Marco Palma was employed by the Efficient Power Conversion Corporation. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationship that could be construed as a potential conflict of interest.

## References

1. Meneghini, M.; De Santi, C.; Abid, I.; Buffolo, M.; Cioni, M.; Khadar, R.A.; Nela, L.; Zagni, N.; Chini, A.; Medjdoub, F.; et al. GaNbased power devices: Physics, reliability, and perspectives. *J. Appl. Phys.* **2021**, *130*, 181101. [CrossRef]
2. Udabe, A.; Baraia-Etxaburu, I.; Diez, D.G. Gallium Nitride Power Devices: A State of the Art Review. *IEEE Access* **2023**, *11*, 48628–48650. [CrossRef]
3. Baliga, J. Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Lett.* **1989**, *10*, 455–457. [CrossRef]
4. Musumeci, S.; Mandrile, F.; Barba, V.; Palma, M. Low-Voltage GaN FETs in Motor Control Application; Issues and Advantages: A Review. *Energies* **2020**, *14*, 6378. [CrossRef]
5. Chierchie, F.; Paolini, E.E.; Stefanazzi, L. Deadtime distortion shaping. *IEEE Trans. Power Electron.* **2019**, *34*, 53–63. [CrossRef]
6. Li, Y.-S.; Wu, P.-Y.; Ho, M.-T. Dead-Time Compensation for Permanent Magnet Synchronous Motor Drives. In Proceedings of the 2020 International Automatic Control Conference (CACS), Hsinchu, Taiwan, 4–7 November 2020. [CrossRef]
7. Liu, G.; Wang, D.; Jin, Y.; Wang, M.; Zhang, P. Current-Detection-Independent Dead-Time Compensation Method Based on Terminal Voltage A/D Conversion for PWM VSI. *IEEE Trans. Ind. Electron.* **2017**, *64*, 7689–7699. [CrossRef]
8. Lidow, A.; Strydom, J.; De Rooij, M.; Reusch, D. *GaN Transistors for Efficient Power Conversion*; Wiley: Hoboken, NJ, USA, 2020. [CrossRef]
9. Musumeci, S.; Palma, M.; Mandrile, F.; Barba, V. Low-Voltage GaN Based Inverter for Power Steering Application. In Proceedings of the 2021 AEIT International Conference on Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE), Torino, Italy, 17–19 November 2021; pp. 1–6. [CrossRef]
10. Ren, R.; Gui, H.; Zhang, Z.; Chen, R.; Niu, J.; Wang, F.; Tolbert, L.M.; Blalock, B.J.; Costinett, D.J.; Choi, B.B. Characterization of 650 V Enhancement-mode GaN HEMT at Cryogenic Temperatures. In Proceedings of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 23–27 September 2018; pp. 891–897.
11. TI: UCC21222 4A, 6A, 3.0kVRMS Isolated Dual-Channel Gate Driver with Dead Time Datasheet [EB/OL]. Available online: https://www.ti.com/product/UCC21222?keyMatch=UCC21222%204A&tisearch=search-everything&bm-verify (accessed on 2 July 2024).
12. Chiu, P.K.; Wang, P.Y.; Li, S.T.; Chen, C.J.; Chen, Y.T. A GaN driver IC with novel highly digitally adaptive dead-time control for Synchronous Rectifier Buck Converter. In Proceedings of the 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 11–15 October 2020; pp. 3788–3792.
13. Thuc, G.H.; Chen, C.-J. A Gate Driver IC for GaN-Based Synchronous Buck Converter with A Double-Sided Adaptive Dead-Time Generator. In Proceedings of the 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 19–23 March 2023; pp. 283–289.
14. Han, D.; Sarlioglu, B. Deadtime Effect on GaN-Based Synchronous Boost Converter and Analytical Model for Optimal Deadtime Selection. *IEEE Trans. Power Electron.* **2016**, *31*, 601–612. [CrossRef]
15. Zhang, Y.; Chen, C.; Xie, Y.; Liu, T.; Kang, Y.; Peng, H. A High- Efficiency Dynamic Inverter Dead-Time Adjustment Method Based on an Improved GaN HEMTs Switching Model. *IEEE Trans. Power Electron.* **2022**, *37*, 2667–2683. [CrossRef]
16. Teng, J.H.; Liu, B.-H. Three-Stage Dead-Time Adjustment Scheme for Conversion Efficiency Enhancement of Phase-Shift Full-Bridge Converters at Light Loads. *IEEE Trans. Ind. Electron.* **2021**, *68*, 1210–1219. [CrossRef]
17. Abe, S.; Hasegawa, K.; Tsukuda, M.; Wada, K.; Omura, I.; Ninomiya, T. Modelling of the shoot-through phenomenon introduced by the next generation IGBT in inverter applications. *Microelectron. Reliab.* **2017**, *76–77*, 465–469. [CrossRef]
18. Lee, J.-H.; Sul, S.-K. Inverter Nonlinearity Compensation of Discontinuous PWM Considering Voltage Drop of Power Semiconductor and Dead Time Effect. In Proceedings of the 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 11–15 October 2020; pp. 5677–5682. [CrossRef]

19. Mandrile, F.; Musumeci, S.; Palma, M. Dead Time Management in GaN Based Three-Phase Motor Drives. In Proceedings of the 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, 6–10 September 2021; pp. P.1–P.10. [CrossRef]
20. Gurpinar, E.; Iannuzzo, F.; Yang, Y.; Castellazzi, A.; Blaabjerg, F. Design of low-inductance switching power cell for gan hemt based inverter. *IEEE Trans. Ind. Appl.* **2018**, *54*, 1592–1601. [CrossRef]
21. Górecki, P.; Górecki, K. Thermal limits of the maximum operating frequency of SiC MOSFETs. In Proceedings of the 2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG), Birmingham, UK, 29 June–1 July 2022; pp. 1–4. [CrossRef]
22. Alemanno, A.; Angelotti, A.M.; Gibiino, G.P.; Santarelli, A.; Sangiorgi, E.; Florian, C. A Reconfigurable Setup for the On-Wafer Characterization of the Dynamic $R_{ON}$ of 600 V GaN Switches at Variable Operating Regimes. *Electronics* **2023**, *12*, 1063. [CrossRef]
23. Górecki, P.; Górecki, K.; Detka, K.; D'Alessandro, V. Influence of parasitics of components and circuit on switching losses of power SiC and GaN transistors in power converter applications. In Proceedings of the 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 4–8 September 2023; pp. 1–7. [CrossRef]
24. Dyer, J.; Zhang, Z.; Wang, F.; Costinett, D.; Tolbert, L.M.; Blalock, B.J. Dead-time optimization for SiC based voltage source converters using online condition monitoring. In Proceedings of the 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, USA, 30 October–1 November 2017; pp. 15–19. [CrossRef]
25. Scrimizzi, F.; Cammarata, F.; D'agata, G.; Nicolosi, G.; Musumeci, S.; Rizzo, S.A. The GaN Breakthrough for Sustainable and Cost-Effective Mobility Electrification and Digitalization. *Electronics* **2022**, *12*, 1436. [CrossRef]
26. Joo, D.M.; Lee, B.K.; Kim, J.S. Dead-time optimisation for a phase-shifted dc–dc full bridge converter with GaN HEMT. *Electron. Lett.* **2016**, *52*, 769–770. [CrossRef]
27. Kasper, M.; Burkart, R.M.; Deboy, G.; Kolar, J.W. ZVS of Power MOSFETs Revisited. *IEEE Trans. Power Electron.* **2016**, *31*, 8063–8067. [CrossRef]
28. Cittanti, D.; Iannuzzo, F.; Hoene, E.; Klein, K. Role of parasitic capacitances in power mosfet turn-on switching speed limits: A sic case study. In Proceedings of the 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017; pp. 1387–1394.
29. Barba, V.; Solimene, L.; Palma, M.; Musumeci, S.; Ragusa, C.S.; Bojoi, R. Modelling and Experimental Validation of GaN Based Power Converter for LED Driver. In Proceedings of the 2022 IEEE International Conference on Environment and Electrical Engineering and 2022 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe), Prague, Czech Republic, 28 June–1 July 2022; pp. 1–6. [CrossRef]
30. Park, S.; Rivas-Davila, J. Power loss of GaN transistor reverse diodes in a high-frequency high voltage resonant rectifier. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 1942–1945. [CrossRef]
31. Musumeci, S.; Barba, V.; Mandrile, F.; Palma, M.; Bojoi, R.I. Dead Time Reverse Conduction Investigation in GaN-Based Inverter for Motor Drives. In Proceedings of the IECON 2022—48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 17–20 October 2022; pp. 1–6. [CrossRef]
32. Pennisi, G.; Pulvirenti, M.; Salvo, L.; Sciacca, A.G.; Cascino, S.; Laudani, A.; Salerno, N.; Rizzo, S.A. Investigation of SiC MOSFET Body Diode Reverse Recovery and Snappy Recovery Conditions. *Energies* **2023**, *17*, 2651. [CrossRef]
33. Sorensen, C.; Fogsgaard, M.L.; Christiansen, M.N.; Graungaard, M.K.; Norgaard, J.B.; Uhrenfeldt, C.; Trintis, I. Conduction, reverse conduction and switching characteristics of GaN E-HEMT. In Proceedings of the 2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Aachen, Germany, 22–25 June 2015; pp. 1–7. [CrossRef]
34. PatWheeler, W.; Clare, J.C.; Apap, M.; Bradley, K.J. Harmonic loss due to operation of induction machines from matrix converters. *IEEE Trans. Ind. Electron.* **2008**, *55*, 809–816.
35. Barba, V.; Musumeci, S.; Palma, M.; Bojoi, R. Dead Time Reduction Strategy for GaN-Based Low-Voltage Inverter in Motor Drive System. In Proceedings of the 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 19–23 March 2023; pp. 2385–2390. [CrossRef]