Abstract

Power electronics is a well-established field that has developed many proven technologies, particularly in Switch-mode Power Supplies (SMPS) that use discrete components and analog control strategies. However, recent advancements in large bandgap semiconductor devices such as silicon carbide (SiC), gallium arsenide (GaAs), and gallium nitride (GaN) offer new opportunities for high-frequency power conversion up to multi-MHz. These advancements have the potential to significantly increase achievable power densities, driving innovation in power electronics. They have also spurred research into integrating control circuits and power devices on the same semiconductor chip. This concept is known as digital control in power electronics, and it has several benefits such as flexibility, reliability, cost-effectiveness, and reduced susceptibility to aging.

Although digital controllers have many advantages, they encounter a specific problem called low-frequency steady-state Limit-cycle Oscillations (LCOs). These LCOs are caused by quantization effects from the Analog-to-Digital Converter (ADC) and the Digital Pulse Width Modulator (DPWM). While high-resolution ADCs and DPWMs can alleviate these problems, they also introduce higher costs and more complexity, particularly for SMPS operating at high switching frequencies using emerging semiconductor technology like GaN and SiC power transistors.

Several high-resolution DPWM techniques have been proposed to address these challenges and enhance DPWM resolution. This has motivated further research into high-resolution DPWM in digitally controlled SMPS and DPWM-based Digital-to-Analog Converters (DACs) design.

In this regard, the thesis presents an in-depth theoretical analysis of LCOs in digitally controlled power converters. The discussion outlines quantization effects, techniques for determining steady-state DC solutions, and guidelines for preventing LCOs. This analysis explores state-of-the-art DPWM techniques, including Sigma-Delta (ΣΔ) modulation, delay line modulation, Digital Thermometric Dithering Pulse Width Modulation (DTDPWM) modulation, and the recently proposed Dyadic Digital Pulse Width Modulation (DDPWM), aimed at enhancing resolution and mitigating LCO onset.

Also, the thesis presents an approach to implement the digitally controlled Boost converter based on DDPWM. Through Simulink/Modelsim co-simulations and experimental testing on a voltage-mode, 7-10 V input, 13.8 V output Boost converter operated at a 1.17 MHz switching frequency under different operating conditions and ADC/DPWM resolutions, the

effectiveness of DDPWM in suppressing the onset of LCOs, increasing DC accuracy, and reducing output ripple has been verified. The accuracy in DC has been increased by more than 6X compared to plain DPWM, while the output ripple has been reduced by approximately 3X compared to DTDPWM.

Additionally, the thesis presents a theoretical evaluation of Dyadic Digital Pulse Modulation (DDPM) and its spectral characteristics, followed by a comparison of DDPM modulators' existing hardware (HW) implementations. The thesis introduces a newly developed optimized DDPM modulator architecture designed explicitly for software (SW) implementation and compares it with an SW architecture derived from directly transferring the HW implementation. To evaluate the proposed SW DDPM modulator's effectiveness and efficiency, an 8-bit DDPM DAC has been implemented using software on a commercially available Texas Instruments c2000 microcontroller platform, showcasing its practical application.

The proposed SW DDPM DAC performs better than the simple iterative SW implementation in all aspects. Its maximum sample rate is 7.812 kS/s, which is 6X higher than the iterative SW DDPM DAC implementation, significantly expanding its potential applications. The static characteristics demonstrate that the peak INL error of the proposed converter is only 1.64 LSBs, compared to 2.8 LSBs for the iterative converter. Additionally, the superiority of the proposed DAC is evident through the measured DNL of 1.79 LSBs, which is much lower than the 3.53 LSBs for the iterative implementation. Finally, the proposed DAC shows considerable improvements regarding dynamic characterization metrics such as SNDR, SFDR, and ENOB.

The proposed DDPM DAC achieves sample rates similar to those of FPGA implementations of DDPM DACs and non-DDPM DACs, such as the DPWM FPGA DAC and the FPGA $\Sigma\Delta$ DAC. However, it has a marginally lower effective resolution, with 2.0-4.8 effective bits less. Unlike these alternatives, it does not require dedicated FPGA hardware, making it a more cost-effective solution.