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(*XXXVI* cycle)

Innovative GaN Multilevel Inverter for Motorsport Applications

By

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Enrico Vico
2024

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Abstract

At the present time, the climate changes represent the most relevant issues that compromise the planet and human future. As the acknowledgement and the interest of the public opinion are raised, the governments have started to promote clean energy production and sustainability to reduce the human activity pollutions. One of the most significative and participated example of this effort is the Paris Agreement. The electrification of the automotive sector represents an important step in this energy transition to reduce the greenhouse gasses produced by the fossil fuel combustion for the transportation sector. As a consequence, the electric vehicles are subject to a great pressure to improve the overall performances to fulfill the gap with traditional cars. In this context, the thesis focuses on the development and the optimization of an innovative automotive traction inverter. In order to achieve the stringent efficiency and power density requirements, the future inverter must adopt non-standard architectures and new technologies. In particular, GaN devices, PLZT ceramic capacitors and multilevel structure are selected as innovative elements. Firstly, they are compared with the respective state-of-the-art counterparts in order to outline the effective advantages. Then, they are combined in a single inverter prototype that exploits the complementary benefits. The presented research activity illustrate lots of contributions that focus on the semiconductor and capacitors technologies comparison, on the converter structure analysis and modelling and on the inverter design and prototype experimental validation.

Contents

Chapter 1

Introduction

Climates changes have become more and more relevant in the last decade. As a consequence, the public opinion and thus the governments have started to become more careful to sustainability and clean energies. This changed mind-set is proved by the Paris Agreement, which represents one of the most participated and important document that states the will to achieve a significant pollutants reduction emitted by human activities. The decrement of the greenhouse gasses produced by the fossil fuel combustion in the automotive sector plays an important role in this energy transition. Under the strong pressure of improvement, electric vehicle (EV) starts to become an interesting solution to reach the more stringent required standards. Indeed, their combination to the usage of energies produced from renewable sources could drastically breaks down the pollutant emissions. In additions, EVs offer high efficient conversion process, reduced maintenance, low noise emissions and excellent acceleration dynamics. However, some gaps compared to the more mature gasoline vehicles must be still addressed. For example, it is registered a not negligible consumer anxiety about the autonomy range and related charging battery process.

1.1 Goal of the Thesis

The main components of the EV power-train are the battery, the inverter and the electric motor. In this context, the thesis goal is to address the design and realization challenges related to the development of a traction inverter for motor-sport application. It is responsible of the energy conversion and regulation from the battery to the

motor. It is clear that its optimization enables to push forward the performances of the power-train and favour the adoption of EV vehicles. Thus, its main requirements and challenges can be summarized in:

- high efficiency to reduce the losses and maximise the battery autonomy range;
- high power density to optimize the volume and weight required;
- low cost to make EV more competitive compared to the traditional gasoline vehicles;
- high reliability to reduce the maintenance intervention;
- high voltage DC-Link rating standard to reduce the charging times and cables sizes;
- high quality synthesized output voltage to reduce the PWM losses and the voltage derivatives stresses on the load motor.

The current architecture traction inverter standard is the two-level voltage source inverter employing 1200V rated Si IGBT or SiC MOSFET. As a matter of fact, the great pressure of improvement has required a change in the standard in the DC-Link voltage rating (i.e. from 400V to 800V) to enable higher charging power rating and cable size reduction. Thus, the achievement of all the targets stated above requires the usage of innovative technologies combined with non-standard topologies, such as:

- *GaN devices*, which are recently entered in the semiconductor market. Even if they are still a not mature technology, they feature higher performances in terms of lower specific resistance and higher switching frequency capabilities compared to the Si/SiC counterpart;
- *multilevel architectures*, which enable the usage of lower voltage rating devices with enhanced performances (i.e. better figure of merit) and synthesize a better output waveform that reduces the stresses on the load motor compared to the standard two-level architecture;
- *PLZT ceramic technology*, which features better specific capacitance and RMS capabilities compared to film capacitors and thus allows to reduce the capacitance requirements optimizing the power density.

The aim of this thesis is to analyse, design and realized an inverter that combines all these innovative elements which present complementary features. The target application is motor-sport, which features high speed low inductance electric motors (i.e. it is then fundamental the inverter output voltage quality waveforms). Due to the extreme complexity and multiple challenges of the project, it has been decided to realize a 800V 100kVA prototype with a target efficiency greater than 98%. Firstly, all these innovative elements are analysed separately to identify all the related strengths and drawbacks. The realized inverter represents a fundamental step to study the architecture integration with the other innovative technologies and the overall behaviour. Due to its prototype nature, it is clear that many aspects such as the control architecture, the measurements and the cooling system can be redesigned and optimized to achieve better overall integration and performances (i.e. both efficiencies and power densities) in the converter future versions.

1.2 Research Contributions

The main research contributions are:

- *innovative elements selection and analysis*: new technologies that can enable a performance improvement in the future inverters have been selected, analysed separately and compared to the state-of-the-art counterpart. A clear estimation of the advantages have been reported and exploited in the final converter design;
- *converter analysis and modelling*: the stresses of all the main inverter components (i.e. both active and passive) have been studied and simple analytical expressions useful in the converter design have been calculated;
- *converter design*: a complete design procedure featuring the selection of all inverter components is provided. Particular attention has been given to the benefit integration of the selected new technologies (i.e. GaN devices and PLZT ceramic capacitors) into the multilevel architecture.

1.3 Outline of the Thesis

- **Chapter 2: Wide Band-Gap Power Devices**
  The chapter introduces the GaN technology comparing the physical properties with the Si/SiC semiconductors. Then, the main GaN architectures are analysed pointing out the benefits and drawbacks of each structure. Some unusual behaviours that must be addressed in the converter design are underlined. From the presented literature review, the main future research trends are identified. Then, a new technology performance comparison method based on the Figure-Of-Merit is presented. Finally, a clear comparison of the advantages of the GaN adoption over SiC devices is presented taking into consideration the target converter operating conditions (i.e. the commutated voltage, the switching frequency and the junction temperature).

- **Chapter 3: Multilevel Converter Topology**
  The history and current application of the multilevel structures are briefly presented. Then, the advantages and the operational basics compared to the traditional two-level inverter standard structure are analysed. Finally, the main adopted architectures are compared with particular attention on the typology and number of the needed devices, on the power loop inductance, on the mid-point low frequency oscillations.

- **Chapter 4: Capacitor Technology**
  The chapter starts with the description of the film and PLZT ceramic capacitors. A first comparison between the two technologies is performed in relative parameters showing the higher performances of PLZT ceramic technology. Then, an experimental characterization is made on a single PLZT capacitor device to verify its thermal and electric characteristics. In particular, a large-signal equivalent capacitance curve not provided by the manufacture is extracted (i.e. it is useful for a precise DC-Link sizing). Finally, a 800V 550kVA 2-level SiC inverter prototype is build featuring a full ceramic DC-Link. The proposed DC-Link sizing procedure is experimentally verified. Weight and volume are compared to a standard film-based DC-Link capacitors solution, showing PLZT ceramic capacitors performance superiority.

- **Chapter 5: Three-Phase Three-Level Flying Capacitor Converter**
  A detailed design procedure for the target innovative inverter featuring three-

level flying capacitor architecture and employing GaN devices and PLZT ceramic capacitors is presented. The stresses for all the main component are presented. In particular, the RMS flux ripple is identified as a practical performance index related to the output voltage quality waveform and to the PWM losses on the load motor. A comparison with the 2-level inverter is presented showing the superiority of the selected topology in this field particularly important for the target motor-sport application. Finally, the component selection and the realized prototype are described. Key aspects such as the power loop commutation and the mechanical assembly are outlined.

- **Chapter 6: Experimental Validation**
  Firstly, the experimental validation of a single-phase three-level flying capacitor converter is presented. It represents an intermediate step before the final converter realization. Then, the gate driver stage is experimentally testes on a separate board. In the end, the experimental set-up for the three-phase converter is presented. The performed tests focus mainly on the flying capacitor balance mechanism and the measured loss curves.

- **Chapter 7: Fast Over-current Protection foe VisIC Devices**
  Here, a fast over-current protection is deepen on a less complex structure compared to the flying capacitor architecture. In particular, the proposed circuit scheme is simulated with LTSPICE and experimentally verified.

- **Chapter 8: Conclusion**
  The main research contribution and achievements are here summarized. Moreover, possible improvements and future research fields related to the presented work are prospected.

1.4 List of Publications

1.4.1 Journal Articles

- D. Cittanti, **E. Vico** and I. R. Bojoi, "New FOM-Based Performance Evaluation of 600/650 V SiC and GaN Semiconductors for Next-Generation EV Drives," in IEEE Access, vol. 10, pp. 51693-51707, 2022, doi: 10.1109/ACCESS.2022.3174777.

- D. Cittanti, F. Stella, **E. Vico**, C. Liu, J. Shen, G. Xiu and R. Bojoi, "Analysis, Design, and Experimental Assessment of a High Power Density Ceramic DC-Link Capacitor for a 800 V 550 kVA Electric Vehicle Drive Inverter," in IEEE Transactions on Industry Applications, vol. 59, no. 6, pp. 7078-7091, Nov.-Dec. 2023, doi: 10.1109/TIA.2023.3307101.

- D. Cittanti, M. Gregorio, **E. Vico**, F. Mandrile, E. Armando and R. Bojoi, "High-Performance Digital Multiloop Control of LLC Resonant Converters for EV Fast Charging With LUT-Based Feedforward and Adaptive Gain," in IEEE Transactions on Industry Applications, vol. 58, no. 5, pp. 6266-6285, Sept.-Oct. 2022, doi: 10.1109/TIA.2022.3178394.

1.4.2 Conference Papers

- D. Cittanti, **E. Vico**, M. Gregorio, F. Mandrile and R. Bojoi, "Iterative Design of a 60 kW All-Si Modular LLC Converter for Electric Vehicle Ultra-Fast Charging," 2020 AEIT International Conference of Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE), Turin, Italy, 2020, pp. 1-6, doi: 10.23919/AEITAUTOMOTIVE50086.2020.9307381.

- D. Cittanti, **E. Vico**, M. Gregorio and R. Bojoi, "Design and Experimental Assessment of a 60 kW All-Si Three-Phase Six-Leg T-Type Rectifier for Electric Vehicle Ultra-Fast Charging," 2021 International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME), Mauritius, Mauritius, 2021, pp. 01-08, doi: 10.1109/ICECCME52200.2021.9590926.

- D. Cittanti, F. Stella, **E. Vico**, C. Liu, J. Shen, G. Xiu and R. Bojoi, "Analysis and Design of a High Power Density Full-Ceramic 900 V DC-Link Capacitor for a 550 kVA Electric Vehicle Drive Inverter," 2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia), Himeji, Japan, 2022, pp. 1144-1151, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807220.

- D. Cittanti, **E. Vico**, E. Armando and R. Bojoi, "Analysis and Conceptualization of a 800 V 100 kVA Full-GaN Three-Level Flying Capacitor Inverter for Next-Generation Electric Vehicle Drives," 2022 International Power Electron-

ics Conference (IPEC-Himeji 2022- ECCE Asia), Himeji, Japan, 2022, pp. 2320-2327, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807091.

- D. Cittanti, **E. Vico**, E. Armando and R. Bojoi, "Analysis and Conceptualization of a 400V 100 kVA Full-GaN Double Bridge Inverter for Next-Generation Electric Vehicle Drives," 2022 IEEE Transportation Electrification Conference and Expo (ITEC), Anaheim, CA, USA, 2022, pp. 740-747, doi: 10.1109/ITEC53557.2022.9813847.

- F. Stella, **E. Vico**, D. Cittanti, C. Liu, J. Shen and R. Bojoi, "Design and Testing of an Automotive Compliant 800V 550 kVA SiC Traction Inverter with Full-Ceramic DC-Link and EMI Filter," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1-8, doi: 10.1109/ECCE50734.2022.9948096.

- D. Cittanti, **E. Vico**, F. Mandrile, E. Armando and R. Bojoi, "Analysis and Conceptualization of a Single-Phase Buck-Boost Integrated EV On-Board Charger Based on a Double Bridge Inverter Drive System," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1-8, doi: 10.1109/ECCE50734.2022.9947444.

- **E. Vico**, F. Stella, S. Giuffrida, R. Bojoi, "Fast Overcurrent Protection for Direct Drive Cascode GaN HEMT Semiconductors Based on Industrial Gate Drivers" (application in process to APEC 2024).

- F. Stella, S. Savio, **E. Vico**, R. Bojoi and E. Armando, "Cost Effective 3D Printed Heatsink for Fast Prototyping of WBG Power Converters" (application in process to APEC 2024).

1.4.3 Patents

- D. Cittanti, F. Mandrile, **E. Vico**, E. Armando, and R. Bojoi, “Caricabatterie Integrato per Veicoli Elettrici basato su Topologia a Doppio Ponte Trifase e Metodo di Controllo”, IT Patent, 2022

- F. Stella, S. Savio, **E. Vico**, R. Bojoi, E. Armando, "Dissipatore a Liquido Stampato in 3D in Multimateriale", IT Patent, 2024 (application in process)

Chapter 2

Wide Band-Gap Power Devices

2.1 Introduction

At the present time, there are a lot of reasons that push toward the energy transition. The Paris Agreement is one of first and most important documents which aims to coordinate a global action against the climate changes [1]. Many governments among which the European Union have started agreements and policies which aim to produce clean energy and reduce the dependence from fossil fuel [2–5]. The key word is sustainability, which means to reduce pollutants in human activities to not further compromise the planet future.
The automotive sector plays a strategic role in the energy transition. Indeed, transport is identified as one of the five biggest greenhouse gas producers in the European Commission 2022 Strategic Foresight Report [3]. In order to become a climate-neutral economy by the 2050, many countries have introduced more restrictive emission laws [6]. Following this trend, electric vehicles (EV) have became more and more attractive respect to traditional petrol vehicles. Indeed, if this technology is combined to the usage of energy produced from renewable sources, the city pollution and in general the greenhouse gasses emissions could be drastically reduced.
Connectivity, Advanced Driver Assistance System (ADAS), shared and electrification are considered as the main driver in the modernization of tomorrow vehicles [7]. According to Yole automotive market forecast [7] in terms of Compound Annual Growth Rate (CAGR), the car electrification will have one of the fastest growths in the next years, as shown in Fig. 2.1.

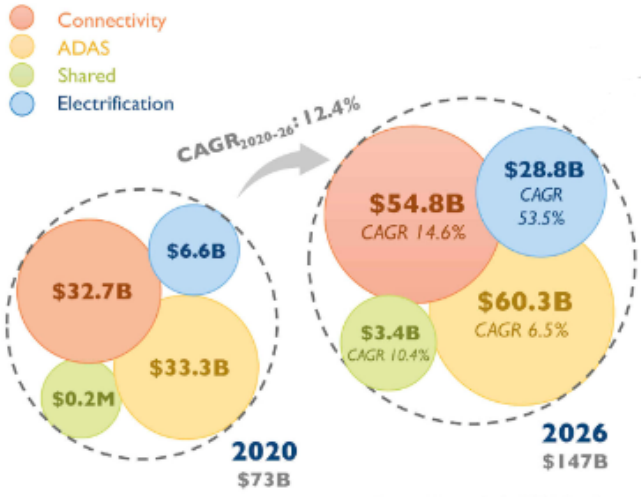


Fig. 2.1 Yole group automotive market analysis and forecast [7]. CAGR=Compound Annual Growth Rate (mean annual growth rate over one year)

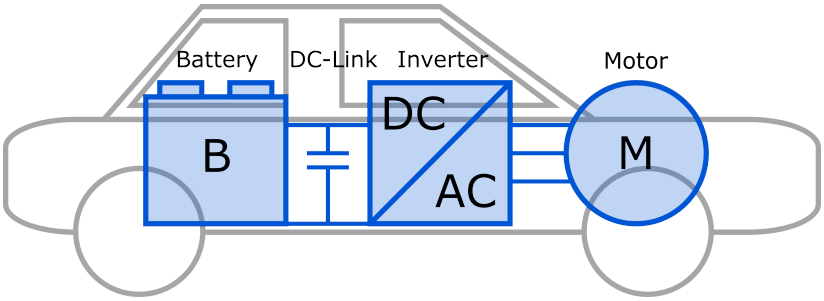


Fig. 2.2 Functional schematic of a electric vehicle powertrain including: battery, capacitive DC-Link, traction inverter and electric motor.

As a consequence, the electric vehicles will triple by 2027 (i.e. passing from 16 million to 50 million EV [8]) and the power electronics market will achieve 26 US $ billion by 2026 [9]. The EV main research and development focus on traction inverter, on-board chargers (OBC) and auxiliary DC/DC converters.
The simplest EV powertain structure consist of the battery system supplying a two-level inverter whose load is the electrical motor, as shown Fig. 2.2.

This work is focused on the traction inverter, whose main required features include high efficiency and power density. Indeed, converter low losses, low weight and volume translate into a reduction of energy battery requirements or in other terms smaller and lighter batteries or extended autonomy range of the vehicle. Taking into account that the battery system is one of the most expensive and heavy component of the electric vehicle, there is a lot of research to optimize the overall system.

The battery voltage architecture and so the DC-Link voltage of the inverter is standardized at 400V. In the last decade, the growing need of high power is shifting this standard to 800V to limit the phase current in cables and connectors. Therefore, the power switch voltage ratings of interest for a two-level inverter are 650V/750V and 1200V, respectively.
The technology of the power switches employed for the inverter design is fundamental to reach high efficiency and power density. The next section will provide an overview on the characteristics of Si devices that are compared with the new WBG materials (SiC and GaN).

2.2 Si versus Wide Band-Gap (WBG) materials

Since the introduction of silicon MOSFET in the 1970s, many efforts have been performed to reduce the device conduction resistance $R_{ds,on}$ which is considered an important performance indicator as directly influences the device conduction losses. The classical planar MOSFET has lots of advantages such as isolated gate (i.e. easy gate controllability) and the fast commutation speed.
The MOSFET symbol is shown in Fig. 2.3 (a), while its planar vertical structure is shown in Fig. 2.3 (b). When this structure is applied to a 650 voltage rated device, the resistance of the drift layer (n^- layer) increases a lot the $R_{ds,on}$ [10], making this solution not convenient for high voltage power converters due to the excessive conduction losses. The drift resistance is proportional to the doping charge and to the width of the drift region. Between 1980s and 1990s, the super-junction silicon MOSFET (SJ-MOSFET) has been introduced on the market. The super-junction principle aims to reduce the channel resistance by modifying the MOSFET structure. As depicted in Fig.2.3 (c), a tighter and highly doped drift column decreases significantly the drift resistance compared to a traditional MOSFET and overcomes its theoretical limit [10], [11].
At the present day, planar MOSFET is still utilized in low voltage power converter while the SJ concept is mainly applied to 650V devices.

As mentioned before, the SJ on resistance is proportional to the breakdown voltage [12]. This limits the super-junction market to the 500V-800V voltage rating class [10]. From 1980s, the insulated gate bipolar transistors (IGBTs) has been used for high current and high voltage applications. The IGBT devices represent today

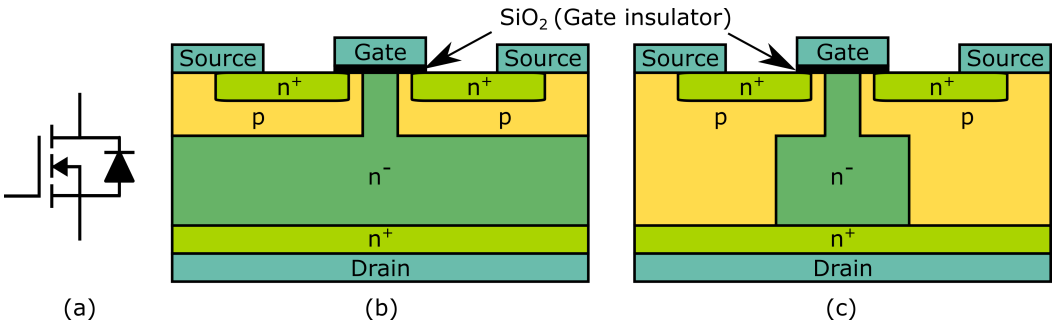


Fig. 2.3 (a) MOSFET circuital symbol (it represents both planar and SJ structure), semiconductor layer structure of (b) planar MOSFET (c) superjunction MOSFET.

the state-of-the-art in both industrial and automotive sector for power devices with voltage rating higher or equal to 650V [13].

The IGBT, whose symbol is shown in Fig. 2.4 (a), combines the features of MOSFET (i.e. simple gate driving) and the bipolar junction transistor (BJT) (i.e. high current density). Fig. 2.4 (b) shows the standard NPT (non-punch through) internal vertical structure of the IGBT. The qualitative asymptotic IGBT and MOSFET conduction characteristics $i_D(v_{ds}), i_C(v_{CE})$ are compared in Fig. 2.4 (c) for devices with rated voltage > 650V. Clearly the IGBT has a lower on resistance at higher current and therefore the IGBT dominates the high voltage applications (commutated voltage higher than 600V).

The Si IGBT has represented the high voltage power switch standard for many years. It is well known that this technology presents some limitations which make difficult for power converters to satisfy the rising demand of power density and efficiency. One example is the low efficiency in traction inverter at low load due to the forward voltage drop V_J.

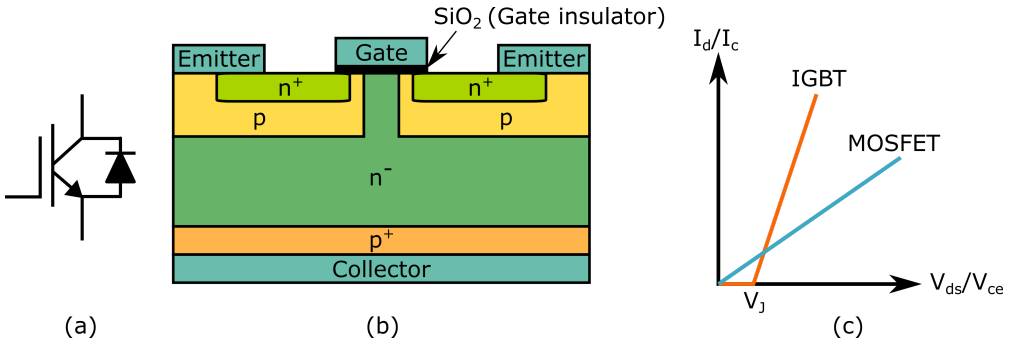


Fig. 2.4 IGBT circuital symbol (a) and semiconductor layer structure (b). MOSFET and IGBT qualitative conduction characteristics comparison (c).

Moreover, the limited switching frequency limits the maximum inverter output frequency.

In the last decade, Si power devices have reached their theoretical limits with the SJ-MOSFET and IGBT [10], [14]. With the aim of further reducing the devices on-resistance, the semiconductor technology must be replaced with a more performing one.
Silicon carbide (SiC) and gallium nitride (GaN) are now considered the most promising materials for the next generation of power switch [15], [16]. Table 2.1 illustrates the key material properties of Si, SiC and GaN.

Table 2.1 SI, 4H-SIC AND GAN MATERIAL PROPERTIES (25°C AND ATMOSPHERIC PRESSURE).

Parameter	**Description**	**Si**	**SiC**	**GaN**
$E_g[eV]$	Energy Gap	1.12	3.26	3.39
$E_c[MV/cm]$	Breakdown Electric Field	0.3	3.0	3.3
$\mu_n[cm^2/Vs]$	Electron Mobility	1400	900	2000
$\upsilon_n[Mcm/s]$	Electron Saturation Velocity	10	20	25
$\lambda_{th}[W/cmK]$	Thermal Conductivity	1.5	3.7	1.3
$T_m[^oC]$	Melting Point	1420	2730	2500

SiC and GaN materials are also commonly known as wide band-gap (WBG) semiconductor due to their higher energy gap compared to Si. While the energy gap and the critical electric field are related to voltage breakdown, the electron mobility and saturation velocity are more connected to the switching frequency capability of the device. The comparison between the different materials has shown that WBG semiconductors present better properties that Si [17]. In particular, SiC seems more suitable for high operation temperature while GaN excels for high switching frequency operation.
It is also important to quantify the influence of these material properties on the power switch performance. Indeed, assuming a fixed breakdown voltage and device structure (i.e. vertical structure), the $R_{ds,on}$ is inversely proportional to the electron mobility and to the third power of the breakdown electric field as shown in the following relation [18]:

$$R_{ds,on} \alpha \frac{1}{\mu_n E_c^3} \tag{2.1}$$

The equation 2.1 is also known as Baliga's figure-of-merit, it shows the technological limit of each semiconductor material that is directly limited by the material properties. This explain why a semiconductor change can enhance the device power handling capability [19] [20]. The new WBG materials (i.e. SiC and GaN) show key properties to further reduce the switch $R_{ds,on}$ enabling power converters with higher efficiency and power density. The theoretical limit improvements are shown in Fig. 2.5, demonstrating the superior performance of GaN that may outperform SiC in terms of specific on-state resistance.

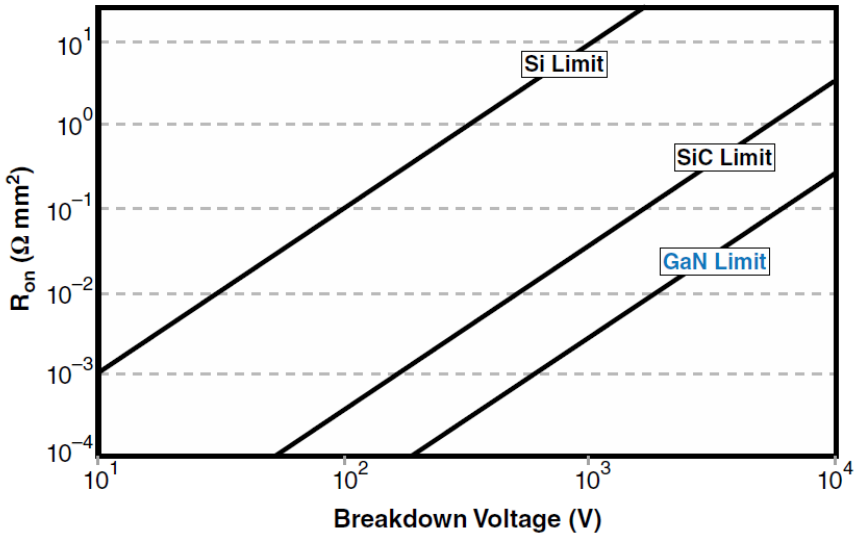


Fig. 2.5 Baliga's figure-of-merit of Si,SiC and GaN material showing the specific $R_{ds,on}$ limit related to the device breakdown voltage [21].

To sum up, WBG devices are now becoming the future standard in power electronics because they can achieve lower on resistance per unit area and better switching performances [15], [22]. This directly translate in a higher inverter efficiency and power density, which will improve the overall EV power train performances [23].

2.3 GaN Power Devices

In recent years, GaN technology has been rapidly penetrating the semiconductor market. Yole Group foreseen that the GaN market will achieve 2 billion US $ by 2027 [24]. At the beginning, GaN devices established as radio frequency (RF) devices [25]. As depicted in Fig. 2.6, consumer and telecom/datacom are now the main application. In particular, GaN devices are rapidly penetrating in the consumer power supply market that will worth more than US $ 900 million in 2027 as reported in the Yole Group GaN market analysis [24]. Two of the main players in this field are GanSystem and Navitas, which have already announced several products designed in collaboration with the leading mobile phone and laptop manufacturer such as Lenovo, Dell, Xiaomi, Samsung, OnePlus and Motorola [26–39]. Lots of prototypes have been also presented for data center application [40–42].

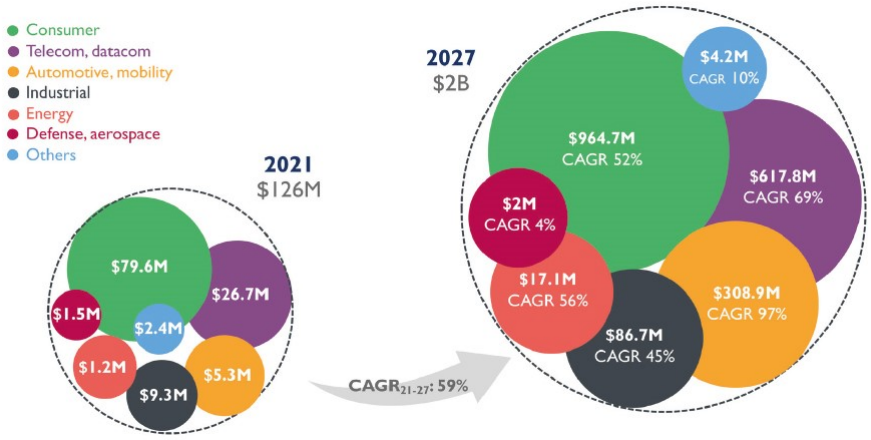


Fig. 2.6 Yole group GaN market analysis and forecast[24]. CAGR=Compound Annual Growth Rate (mean annual growth rate over one year)

Generally, in low power application GaN devices have already achieved an high penetration level [24], [43]. To encourage the adoption of this devices many GaN manufacturers have realised several converter prototype designs [44–50]. As shown in Fig. 2.6, one the most important of GaN market (CAGR 97%) is related to the automotive applications, with focus on auxiliary DC-DC converter [51–53] and on-board charger (OBC) [54–59]. The automotive industry interest on GaN technology is demonstrated by the different collaborations between OEMs/TIER1 and GaN manufacturers, such as Navitas and Brusa [60], GaN System and Toyota [61], VisIC and Marelli [62], Neaxperia and Ricardo [63] and many others [64–66]. In addition, the GaN market has become very dynamic and competitive. An example is the recent

acquisition of GeneSiC semiconductor announced by Navitas Semiconductor [67]. The adoption of GaN devices to automotive is boosted if the GaN manufacturers provide AEC qualified products, such as Transphorm, EPC, TI, Nexperia, and Gan Systems. The straightforward development will be the penetration in automotive high power rated application (i.e. traction inverter and off board charger) as shown in Fig. 2.7. Many collaborations have been announced to realize traction inverter [61, 63, 66, 68]. Clearly this passage will be easier when GaN modules will be commercially available.

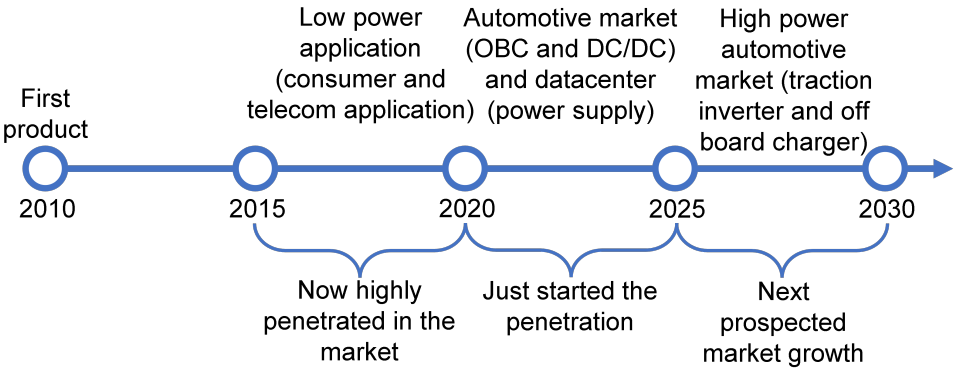


Fig. 2.7 GaN timeline according to the presented literature review.

As explained before, GaN material has lots of potential but the state-of-the-art device manufacturing is still far away to reach the theoretical material limits [69]. The technology achievements in the actual commercially available devices are shown in Fig. 2.8. These are compared to the theoretical $R_{ds,on}$ limit achievable by the material physical properties in relation to the breakdown voltage expressed in the Baliga figure of merit [18] defined by 2.1. It is clear that Si and SiC devices are a more mature technology as they approach their theoretical limit, while GaN still has margin of improvement.

The next subsection will review the GaN structure of the devices available on the market. Starting form the normally-on depletion devices, the HEMT, GIT, cascode and direct drive normally-off power switch will be analysed to emphasize the pros and cons of each technology.

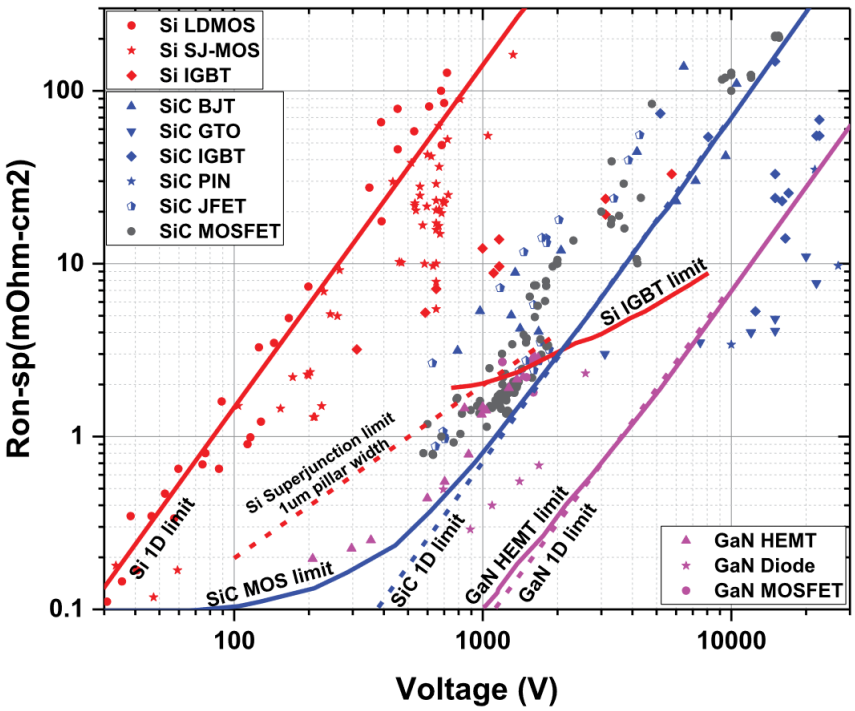


Fig. 2.8 Theoretical $R_{ds,on}$ limit related to the breakdown voltage compared to the commercially available devices for Si, SiC and GaN material [70].

2.3.1 Lateral Devices

As mentioned before, the Si IGBT and SiC MOSFET present a vertical structure. As it is quite difficult to fabricate GaN substrates [71], all GaN devices that are commercially available exhibit a lateral structure. For this reason, the *GaN* layer is typically grown by metalorganic chemical vapour deposition (MOCVD)[72] or molecular-beam epitaxy (MBE) [73] on a Si substrate. This substrate material is clearly cheaper than GaN. Moreover, all the manufacturer process, the know-how and the instruments already employed for Si MOSFET can be utilized (i.e. leading to a considerable manufacturing cost reduction). GaN-on-Si is now the standard technology structure for GaN power devices [24], [74].
The fundamental switch structure is the normally-on depletion mode device that is shown in Fig. 2.9.

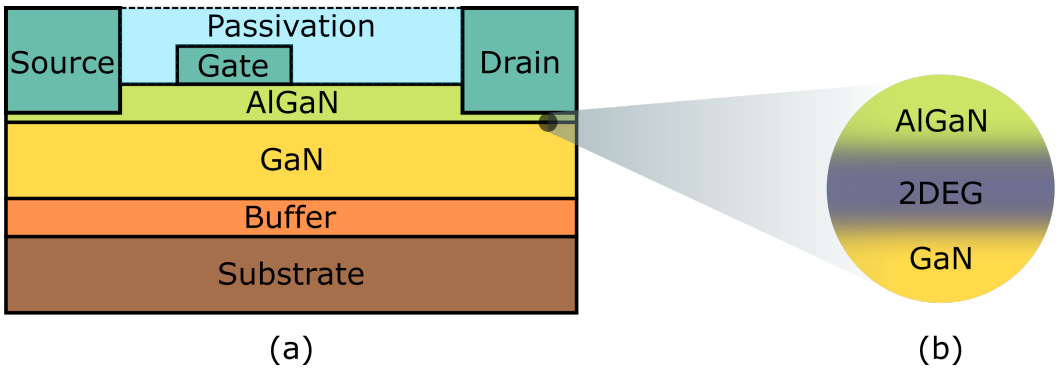


Fig. 2.9 (a) Depletion *GaN* layer structure including substrate (brown), buffer (orange), undoped *GaN* (yellow), *AlGaN* (green), passivation (light blue), source gate and drain pads(aqua green). (b) enlarged detail of the heterojunction between the *GaN* and *AlGaN* layer where the two-dimension electron gas 2DEG (violet) originates.

As shown in Fig. 2.9, the layer disposition of the depletion-mode lateral GaN device includes:

- **Two-dimension electron gas (2DEG) (violet)**: it is the highly conductive channel of the power devices. It is spontaneously originated at the boundary of the GaN and AlGaN layers. Unlikely to conventional MOSFET, the GaN layer is intentionally left undoubted. So the 2DEG formation is due to the spontaneous and piezoelectric polarization which originate at the GaN/AlGaN heterojunction. The first is caused by the electronegativity of the materials. The latter is raised by the strain of the materials thermal expansion coefficient (CTE) mismatch at the interface [75], [76]. A theoretical calculation of the sheet carrier concentration is presented in [77].
- **Passivation layer (light blue)**: it is the ultimate shield layer that protect the semiconductor from the external environmental.
- **Source gate and drain pads (aqua green)**: they represent the physical output contacts of the power switch.
- **AlGaN layer (green)**: it is one of the heterostructure components that is fundamental in the formation of 2DEG channel. There is a critical thickness under which the 2DEG does not originates. Both thickness and Al% in the composition influence the two-dimension electron gas properties [75].
- **GaN layer (yellow)**: one of the main issues of the epitaxially growth of GaN layer is the thermal expansion coefficient mismatch with the non native

substrate [78]. The resulting threading dislocation (TD) affects the crystalline quality of the *GaN* and *AlGaN* layers. Consequently, this will worse the conduction properties of the 2DEG [75].

- **Buffer layer (orange)**: it is inserted to mitigate the CTE mismatch between the substrate and the *GaN* layer. It is often made of different Al layer [72].
- **Substrate layer (brown)**: it can be made of different materials such as Si, sapphire or SiC [78]. GaN substrate is difficult to manufacture and cost-prohibitive. As a consequence, lateral switch structure is now dominant on the market.

To sum up, the 2DEG layer is spontaneously originated at the heterojunction between the undoped GaN and and AlGaN layers. The 2DEG layer represents the conductive channel (i.e. the device current path), so it is one of the most important part of the power devices. As a consequence, 2DEG is subject of many studies which aim to both explain its formation and optimize its features [79–81]. In order to generate a continuous and stable electron gas layer, it is fundamental to create an AlGaN film with a stable stoichiometry [75]. This is achieved with a minimal film thickness value which also depends on the Al percentage. Indeed, too thin AlGaN films are more prone to oxidation phenomena, which cause imperfections and composition variations in the material thus leading to discontinuities in the conduction characteristic of the two dimension electron gas. The optimal AlGaN thickness and Al percentage in composition result from a compromise between electron density (proportional the thickness and Al%) and the mobility (inversely proportional with the thickness and Al%) [75, 76, 82]. The 2DEG formation is not a unique property of the GaN/AlGaN interface, a similar potential surface distribution phenomenon has been observed for the $LaAlO_3/SrTiO_3$ in [83].
The main problem of this depletion mode lateral device is that it is a normally-on device, which means that a negative gate-to-source voltage is needed to go in the OFF state [71]. This correspond to an unsafe operating mode. Indeed, in power electronics it is preferable a normally-OFF devices when the auxiliary power supply is disabled (i.e. at the converter start-up or in a fail event). To overcome this problem, several structures have been implemented to manufacture normally-off devices, as described in the following subsections.

E-mode High Electron Mobility Transistor (HEMT)

The enhanced mode (e-mode) HEMT is a normally OFF device, i.e. the OFF state is obtained when no voltage is applied between gate and source. When a positive voltage is applied on its gate, the switch goes to the ON state. Since this feature is particularly appreciate in power electronics, there have been lots of research to transform the depletion mode structure in enhances mode device. Each manufacturer has its own process, but generally this transformation is obtained through a gate structure modification or putting a low voltage Si MOSFET in series with d-mode GaN to get a cascode configuration. It will be investigated separately in a dedicated subsection. The main adopted gate structures to get a normally-OFF device are:

- **Recessed gate**: as mentioned before, under a certain AlGaN film thickness value, the 2DEG highly conductive channel does not originate. The recessed gate structure (shown in Fig. 2.10) aims to make a thinner AlGaN film under the gate pad in such a way that there is no 2DEG formation under it [84]. As a consequence, the conductive channel is generated only if a positive gate voltage is applied on the gate above a certain threshold value, otherwise the device is normally OFF.

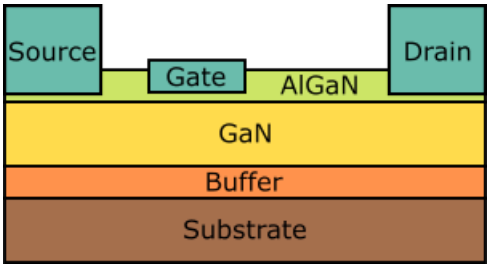


Fig. 2.10 Recessed gate GaN layer structure.

- **Plasma treatment gate structure**: in this case, the AlGaN barrier is undergoing to a fluorine treatment under the gate pad as shown in Fig. 2.11. In this area, the implanted negative fluorine charges prevent the 2DEG formation and normally OFF e-mode device is created. It is mandatory that no fluorine atoms reach the GaN layer, otherwise conduction channel mobility decreases [85].
- **P-doped GaN structure**: here a positively charged GaN layer (i.e. p-GaN) is positioned between the AlGaN film and the gate pad, as shown in Fig. 2.12.

As in the previous structures, the 2DEG does not originates under the gate and the e-mode device is obtained [25].

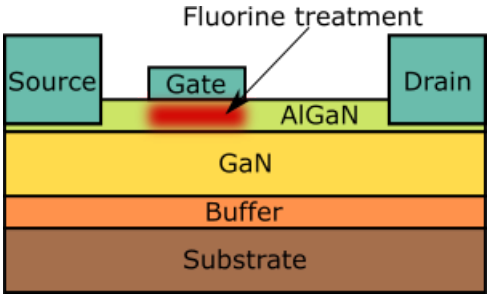


Fig. 2.11 Plasma treatment gate GaN layer structure.

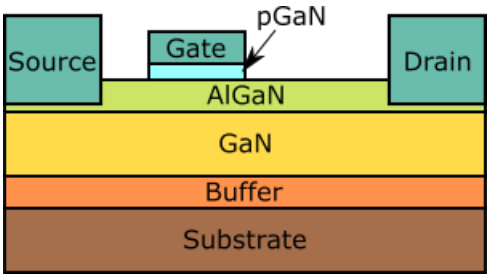


Fig. 2.12 P-doped gate GaN layer structure.

The main drawback of this technology is the gate driving stage. Indeed HEMT devices have a very low voltage threshold (i.e. few volts), which makes the gate spikes very dangerous in the OFF state (i.e. they can turn the switch ON causing shot-through events). Moreover, also the maximum peak gate voltage sustained by the device is typically close to its static value. With this reduced safety margin, a very precise gate PCB design and voltage control are required to avoid dysfunctions related to the parasitic ringing or voltage spikes. As a consequence, the turn OFF and the turn ON damping requirements are different. Fig. 2.13 (b) shows a qualitative example of gate voltage waveform.

While a faster transition is allowed at the turn-OFF, a critically damped transient is desired at the turn-ON to respect the strict requirement [21]. These aspects make the gate driving of these switches very fragile and susceptible to external noise. The typical gate voltage levels of the commercially available e-mode GaN devices are between 5V and 7V. Except this facts, the gate driver structure results similar to the Si MOSFET one as shown in Fig. 2.13 (a). Generally, in all GaN HEMT devices

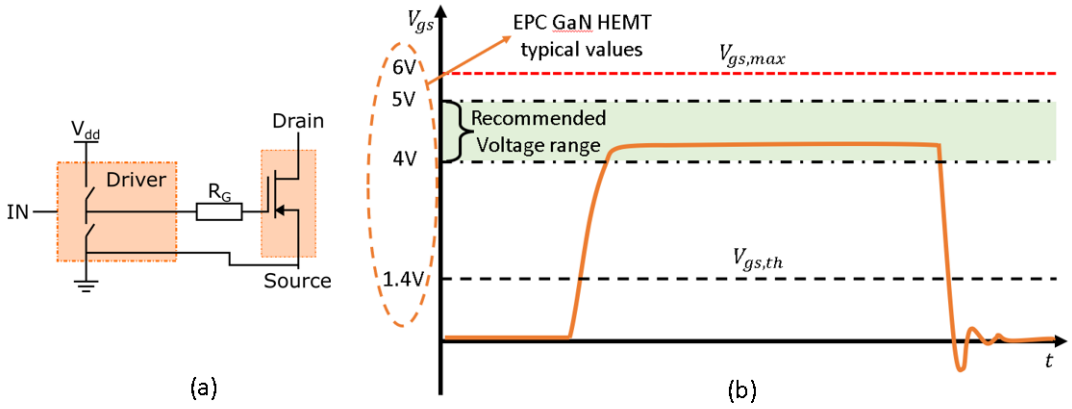


Fig. 2.13 (a) GaN HEMT gate driver scheme and (b) qualitative gate voltage waveform with usual voltage values referred to EPC devices.

the voltage precision and the noise rejection requirement (i.e. dv/dt immunity) are more severe. The selection of the appropriate gate driver is an important task in the converter design. On the other hand, the gate charge result very limited. Thus, the low driving loss enables high switching frequency converter (hundreds kHZ).
The main GaN HEMT manufactures are EPC, GaN System, Texas Instruments and Navitas.

Gate Injection Transistor (GIT)

The main GIT device manufacturer is Infineon that commercializes the *CoolGaN* devices in collaboration with Panasonic. Their gate structure is the p-doped gate shown in Fig. 2.12 and described in the previous subsection [86]. The contact between the p-GaN and the AlGaN layers generates a pin diode [87]. On the other hand, the gate metallization material type combined with p-GaN doping level and the manufacturing process produce different metal/p-GaN interfaces that lead to different gate behaviours [88–90]. The gate injection transistor features an ohmic gate structure shown in Fig. 2.14 (a), while the standard HEMT described before presents a Schottky gate structure depicted in Fig. 2.14 (b). The GIT is an enhanced mode switch and thus it is normally OFF devices.

The GIT turns ON when a gate voltage grater of its threshold value is applied to the gate. The main difference form standard HEMT switch is in the driver circuit at

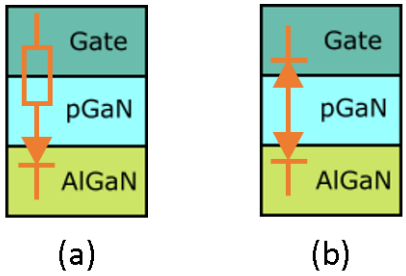


Fig. 2.14 GaN gate structure equivalent circuit schematic comparison (a) ohmic structure, (b) Schottky structure.

steady state operation. In the ON state, the GaN gate structure can be schematically represented like a diode as shown in Fig. 2.15 (a). Taking into account that the device is symmetrical, there are two equivalent diodes which are formed between the gate and the source and between the gate and the drain [91].
In the case of EPC GaN HEMT, the diode knee is around 5/6V (i.e. it depends by the device). As stated before, the manufacturer strictly recommends to not overcome this limit. On the other hand, GIT from Infineon has the diode knee around 3V as shown in datasheet of IGOT60R070D1 reported in Fig. 2.15 (b).

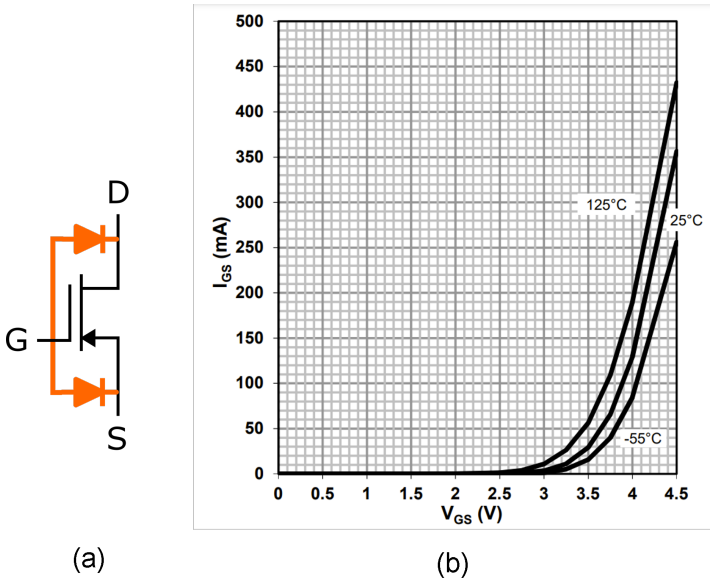


Fig. 2.15 (a)Equivalent diode gate behaviour scheme. Due to device symmetry one is formed between the gate and the source and the other between the gate and the drain, (b) forward gate characteristic form for IGOT60R070D1 [92].

The GIT device is driven with an higher knee voltage of the GaN gate equivalent diode behaviour. As a consequence, the gate driver must supply a steady state current in the gate loop in the range of tens of mA during the ON state of the switch. When the gate voltage is removed, the device is then turned OFF. Fig. 2.16 shows the qualitative gate charge characteristic of GaN GIT (i.e. continuous line) compared with the Si and SiC devices (i.e. dashed line).

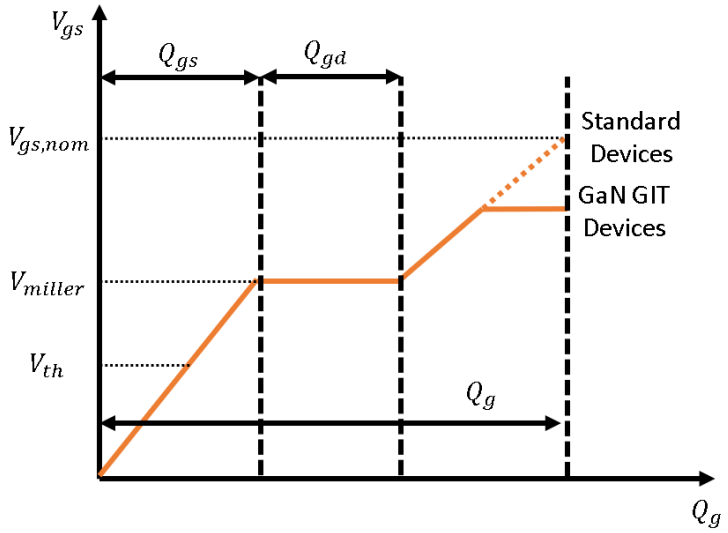


Fig. 2.16 Asymptotic qualitative gate charge characteristic of a GaN GIT (continuous line) compared to the one of standard Si and SiC devices (dashed line).

Initially, the gate-to-source voltage V_{gs} rises above the threshold value and start turning ON the device. After the power switch is completely ON (i.e. the miller plateau has been overcome), the gate voltage of standard devices achieve the nominal value. By contrast, the V_{gs} of the GIT devices is clamped. This is caused by the fact that the equivalent diode is turned ON and the driver stage is injecting a small current quantity in the driver loop as shown in Fig. 2.17 (b).
The driver stage of GIT power switch is then slightly more complicated [93]. As an example, it can be used a normal gate driver with separate output as shown in Fig. 2.17 (a). As soon as the device turn ON the on resistance $R_{g,ON}$ gives the required dynamic power. On the other hand, the resistance $R_{g,st}$ sets the steady state current needed to completely turn ON the device. The OFF stage is similar to standard devices. The GIT devices have the same problem of the standard HEMT. Their threshold voltage is very low. As a consequence, the power switch is susceptible to

noises. To prevent an unwanted turn ON, a negative gate voltage, a strong pull-down OFF resistance or an miller clamp circuit can be designed in the driver circuit.

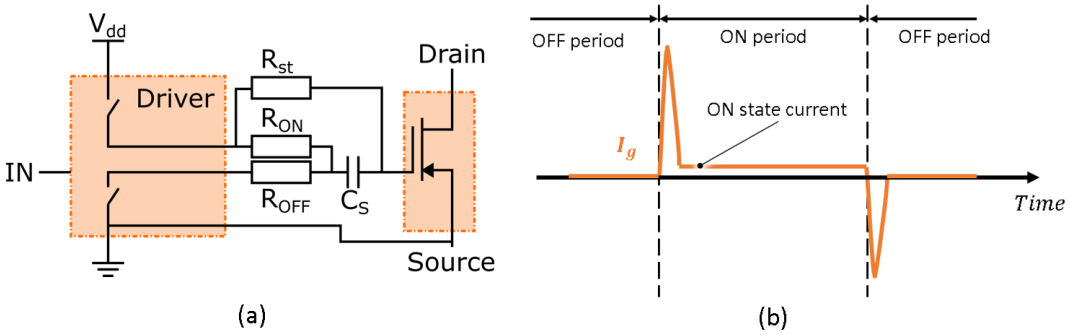


Fig. 2.17 (a) GaN GIT gate driver scheme and (b) qualitative gate current waveform.

Cascode Devices

The cascode configuration represents an easy manufacturing solution to implement normally-off GaN devices. It is composed of a depletion mode GaN switch and a low voltage Si MOSFET (i.e. 30V voltage ratings) connected in series. As shown in Fig. 2.18, the devices share the same current path while the voltage is split between the two in the OFF state. The GaN gate-source voltage is commanded by the drain-source of the Si MOSFET. The main drawback of this configuration is an increase in packaging complexity. Indeed, the two devices are connected in the same package typically with wire-bond. This introduces a rise in the overall parasitic package inductance, which leads to an increase in commutation overvoltage and switching losses. The source and the gate of the GaN switch are not directly accessible from the outside.

Fig. 2.19 shows the GaN cascode forward and reverse conduction characteristics and the related current path in the device for different ON/OFF states. As a matter of fact, in the picture three different device operations are illustrated. Beside the forward conduction, there are two types of reverse conduction. The first type (number two in Fig. 2.19) occurs when the Si MOSFET is left OFF (i.e. occurring during dead time). Hence, the voltage drop due to the low voltage MOSFET body diode can be observed. The other reverse conduction happens when the Si MOSFET it turned ON (number three in Fig. 2.19). Generally, when an high voltage is applied to the overall device in the OFF state, the drain-to-source voltage of the low voltage Si MOSFET starts rising. Simultaneously, a gate-to-source voltage $V_{gs,GaN}$ of the same absolute

value but opposite sign is applied to d-mode GaN device, since the GaN gate pin is connected to the Si MOSFET source pin. When the $V_{gs,GaN}$ overcomes the threshold value, the GaN device is turned OFF.

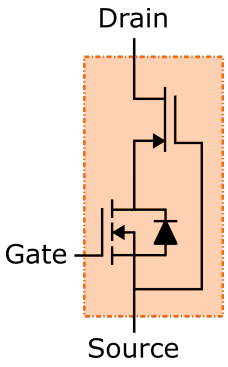


Fig. 2.18 GaN cascode functional scheme. Both the low voltage Si MOSFET and the GaN semiconductor die are integrated in the same package represented by the orange rectangle.

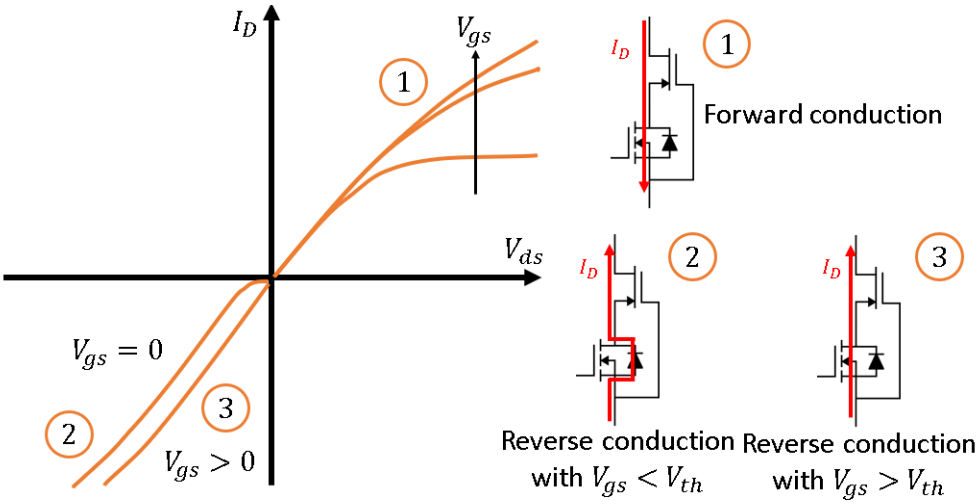


Fig. 2.19 GaN cascode forward and reverse conduction characteristics. On the right it is outlined the related current path in the device for different on/off states

Looking at the structure illustrated in Fig. 2.20, it is clear that the input capacitance C_{iss} of the GaN cascode device is the one of the Si MOSFET. On the other hand, the output capacitance C_{oss} is the combination of the low voltage MOSFET and the GaN switch. This can be notice in the discontinuity of the C_{oss} characteristic as shown in Fig. 2.20. Indeed, in the low voltage area the main contribution of the output capacitance is related to the Si MOSFET, while at high voltage GaN switch pinch-off and it shows its trend [94].

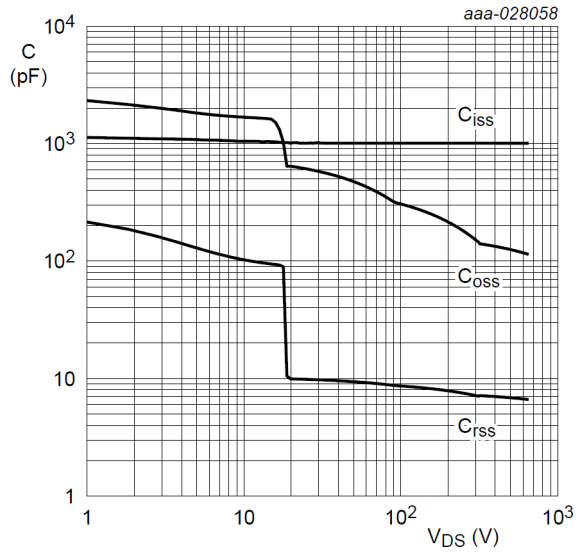


Fig. 2.20 Input, output and reverse transfer capacitances expressed as a function of drain-source voltage [95]

While the low voltage MOSFET on resistance is negligible for high voltage cascode [21], [96], its body diode contributes to the overall device losses. Indeed, the depletion mode GaN is a unipolar device, thus it does not present the reverse recovery phenomenon. On the other hand, a small reverse recovery due to the Si MOSFET body diode is observed in the commutation of the cascode switch. Fig. 2.21 shows the experimental measurement of the reverse recovery for a GaN cascode device and for a SJ Si MOSFET considering the same switching condition. Due the low voltage rating of the Si MOSFET in the cascode, the reverse recovery charge Q_{rr} results drastically reduced compared to the SJ counterpart.

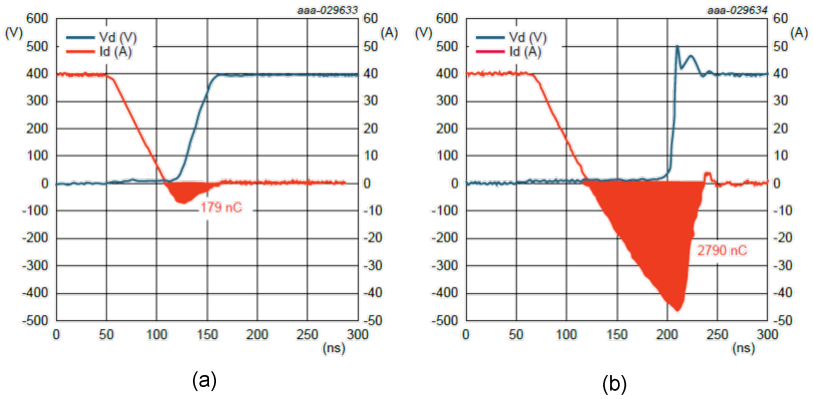


Fig. 2.21 Reverse recovery comparison at the same switching condition (400V,40A and 800 $A/\mu s$) of (a) GaN Cascode and (b) SJ Si MOSFET [94].

The main GaN cascode manufacturers are Transphorm and Nexperia. The products on the market are available in both low inductive surface mounted and standard TO packages [97]. They are usually rated until 175^oC. Cascode devices have a standard driving stage. Indeed it is similar to the driving approach adopted for Si MOSFET (i.e. no negative gate voltage is required). It has thus an high gate voltage threshold (i.e. giving noise robustness to the device) and simple structure as shown in the schematic of Fig. 2.22. Therefore, existing commercial Si MOSFET standard and robust gate driver solution can be employed. The simplicity of the gate driver stage is a great advantage in the practical converter realization (i.e. both in cost reduction and robustness aspect) compared to HEMT and GIT power switches.

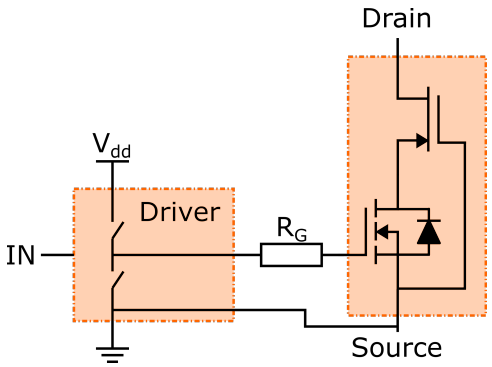


Fig. 2.22 GaN cascode simple drive scheme.

Direct Drive Devices

As explained in the previous subsection, one of the GaN cascode configuration advantage is the simple and robust gate driver stage. As a matter of fact, these devices are commanded by piloting the low voltage Si series MOSFET. While direct drive devices have the same cascode structure (i.e. a depletion mode GaN put in series with a low voltage Si MOSFET), the gate driver approach is different. First of all, the Si MOSFET does not commutate with the GaN transistor. It is only turned on by an enabling signal. Its main purpose is preventing a short-circuit at the converter start-up or auxiliary supply failure. Another great difference is that the gate driver stage pilots directly the GaN gate, which is accessible from the outside [96]. The standard GaN cascode functional scheme and the direct drive architecture are illustrated respectively in Fig. 2.23 (a) and (b). Compared to a traditional cascode structure, the direct drive approach substantially eliminates the reverse recovery losses due to the low voltage Si MOSFET and reduces the overall switching losses

(i.e. classical cascode has to charge and discharge both the GaN gate-to-source and Si MOSFET output capacitance each switching cycle).

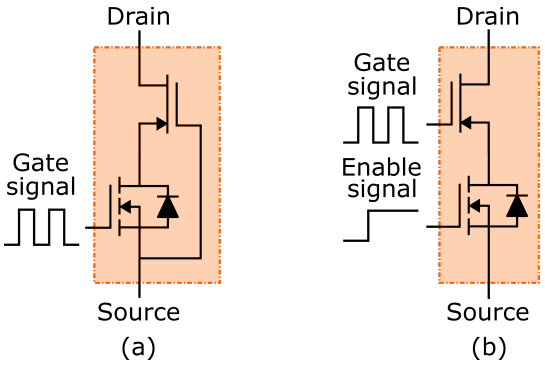


Fig. 2.23 GaN and low voltage Si MOSFET semiconductor die connection in the same package (represented by the orange rectangle) and gate driver principle scheme for cascode (a) and direct drive cascode (b) architectures.

There are two main manufacturers of GaN direct drive cascode. The first one is VisIC technologies. In this case, the enabling circuitry is more complicated than a single Si MOSFET as shown in Fig. 2.23 (b). To ensure a safe normally off state, the diode D_1 and switches Q_1 and Q_2 are integrated in the same package of the GaN devices as shown in Fig. 2.24. Moreover, an external circuit providing the under voltage lock out (UVLO) function is added. Q_1 and Q_2 are p-channel Si MOSFET, the pull-up resistance R_1 ensure to keep them in the OFF state [98].

To fully understand the operation mechanism, the following cases are described:

1. **High voltage bias applied in OFF state (auxiliary supply working)**: when the high voltage bias is applied to the the entire power switch, the source-to-drain voltage V_{sd,Q_2} on the p-MOS Q_2 starts to rise. The fast Schottky diode D_1 clamps the Q_2 drain terminal to the GaN gate, the GaN gate-to-source voltage $V_{gs,GaN}$ is equal to V_{sd,Q_2} but with an opposite polarity. Therefore, as V_{sd,Q_2} rises a gate voltage with same absolute value but opposite sign is applied on the GaN switch. As soon as it reaches the GaN gate threshold voltage $V_{th,GaN}$, the d-mode GaN is turned OFF and stands the high voltage bias. This mechanism is very similar to the one described for standard cascode devices.

2. **High voltage bias applied in OFF state (auxiliary supply NOT working)**: the device operates as described in the previous case. Moreover, the driver circuit is sectioned since Q_1 is in the OFF state.

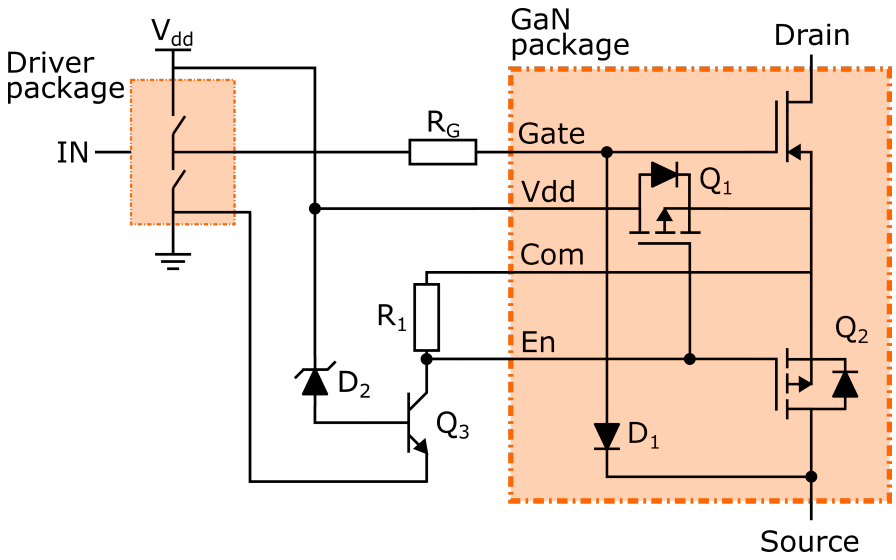


Fig. 2.24 VisIC direct drive GaN devices schematic. The gate driver and the GaN device package are represented by the orange rectangle. D_1, Q_1 and Q_2 are integrated in the GaN package. R_1, D_2 and Q_3 represent the external UVLO circuit.

3. **ON state**: both Q_1 and Q_2 are kept permanently ON and thus they have no influence in the device switching performance (i.e. no reverse recovery phenomena). Q_2 adds only a small conduction resistance. The gate driver commands directly the GaN gate.

The ULVO external circuit further ensures a normally OFF operation especially at the auxiliary power supply shut-down/start-up. Indeed, when the auxiliary power supply voltage is under a fixed value (i.e. it is setted by the zener diode D_2), the pre-biased BJT Q_3 turns OFF Q_1 and Q_2 and the power switch operates as the case 2 described before. In [99] an example of robustness device evaluation and static and dynamic parameter characterization are presented for the VisIC V22TC65S1A power switch.

The second main GaN direct drive cascode manufacturer is Texas Instruments (TI). In this case, the device philosophy is slightly different, inasmuch the complete gate driver stage is integrated in the power device. The first advantage is the overall reduction of the gate loop parasitic inductance. Fig. 2.25 shows the parasitic inductances introduced by a discrete packages solution.

While the inductances due to bonding wire of the gate driver ($L_{dr,out}$ and $L_{dr,gnd}$) are usually limited to few nanohenries (i.e. the gate driver usually has a compact surface-mount package), the ones introduced by the power switch package ($L_{sw,g}$

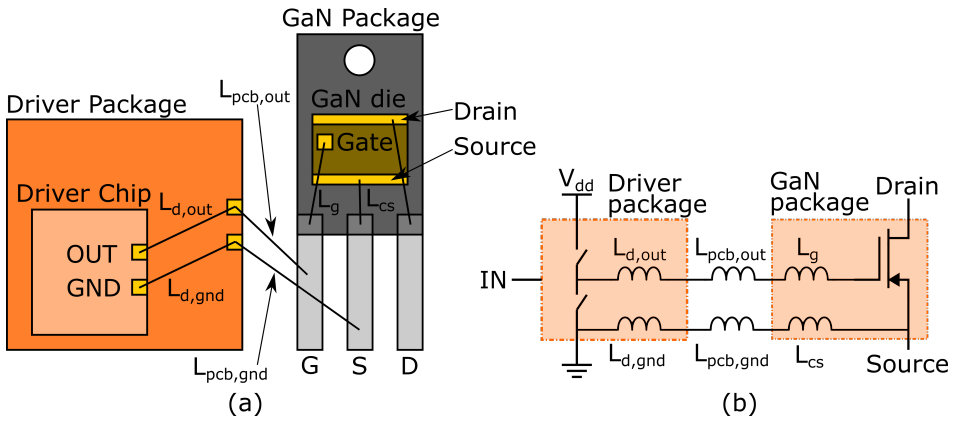


Fig. 2.25 Traditional gate driver accomplished with discrete components: (a) discrete packages illustration, (b) schematic block representation

and L_{cs}) are more relevant. Indeed it can achieve 10 nH for TO-220 or 15 nH for TO-247 through hole devices [100]. For this reason, even if these packages have a better thermal management, a low inductive surface-mounted switch package is often preferred. The inductances contribution of the PCB connection ($L_{pcb,out}$ and $L_{pcb,gnd}$) can be minimized by a proper layout design. Among all the components, the common source inductance (L_{cs}) is the most important parameter. Indeed, when high current derivative (di/dt) occurs, disturbances and oscillations can be generated in the gate circuit.
To sum up, the gate driver integration reduces the gate loop inductance (i.e. eliminating the inductance contribution due to the bonding wires and lead in the driver and switch discrete packages) thus improving the switching performances. As a matter of fact, the minimization of the common mode inductance decreases the gate oscillation (i.e. reducing the stress on the gate) and improves the hold-off capability [100]. Fig. 2.26 shows the system (a) and schematic (b) integrated gate direct drive GaN cascode produced by Texas Instruments.

Moreover, the gate driver integration allows to implement additional features such as switching slew rate control, over-temperature and over-current (i.e. measuring the Si MOSFET on resistance) protections [96]. Since the inductances connections are minimized by the system integration, these protections have optimal intervention response [100]. This integration contributes to reduce the gate driver components on PCB and thus enhancing the design compactness and reliability [101]. Fig. 2.27 shows an example of block diagram which illustrates all the TI LMG341 product family integrated functionalities.

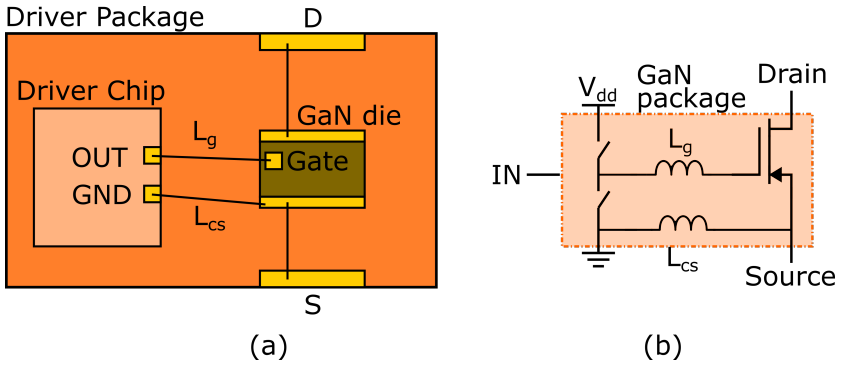


Fig. 2.26 Texas Instruments integrated drive direct drive solution: (a) package illustration, (b) schematic block representation

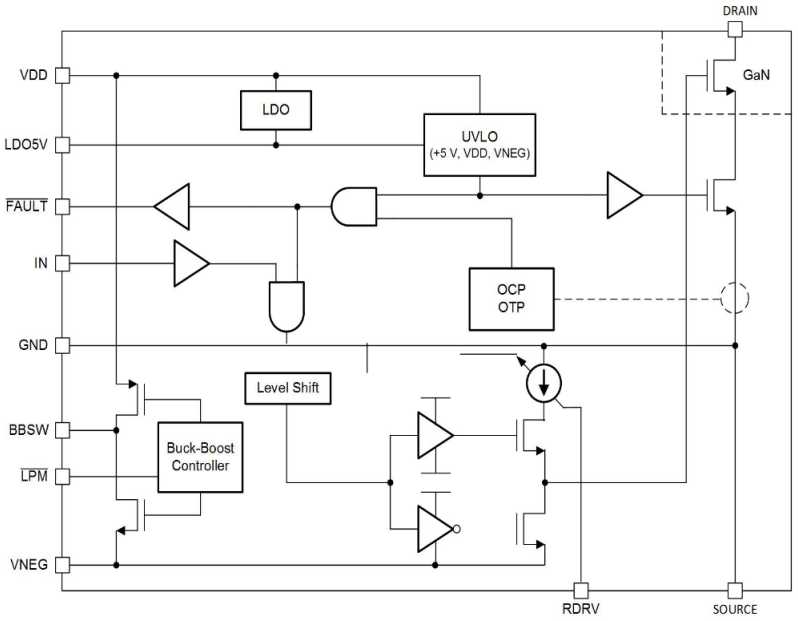


Fig. 2.27 GaN driect drive functional block diagram of TI LMG341 family [102].

2.3.2 Additional Issues of GaN Devices

Despite GaN devices have different structures, they present some issues that are not encountered for Si counterparts. This subsection aims to analyse and explain these issues. As example, the GaN devices do not have a parasitic body diode such as in Si and SiC MOSFETs. Consequently, the reverse conduction originates with a different mechanism. However, the overall effect looks similar to the other devices but with an increased threshold voltage. It is important to know and manage this aspect in order to limit the dead time losses. The current collapse phenomenon is also known as dynamic ON resistance. Although the manufacturer has mitigated this problem, it can

be responsible of an increment in conduction losses. Lastly, the breakdown behaviour is analysed. As said before, at the time of writing, all commercially available GaN devices adopt a lateral structure, so they present a dielectric breakdown mechanism. As a consequence, some devices have a transient voltage capability specified in the datasheet. All the covered aspects help to understand how to better integrate and how to fully exploit the GaN device in the power converter.

Reverse Conduction Behaviour

The body diode provides the reverse conduction path in a standard Si MOSFET. In GaN devices, there is no pn junction and therefore no parasitic body diode exists. Therefore, the reverse conduction mechanism originates differently. Indeed, the reverse current flows directly in the conduction channel. The GaN switch has a symmetrical gate structure as shown in Fig. 2.15. As a consequence, the device is turned ON also if the gate-to-drain voltage V_{gd} overcomes its own threshold value $V_{gd,th}$ (i.e. $V_{gd} = V_{gs} - V_{ds}$). In reverse conduction, the GaN switch behaves like a resistor put in series with a diode whose threshold voltage depends also on the OFF gate voltage as shown in Fig. 2.28.

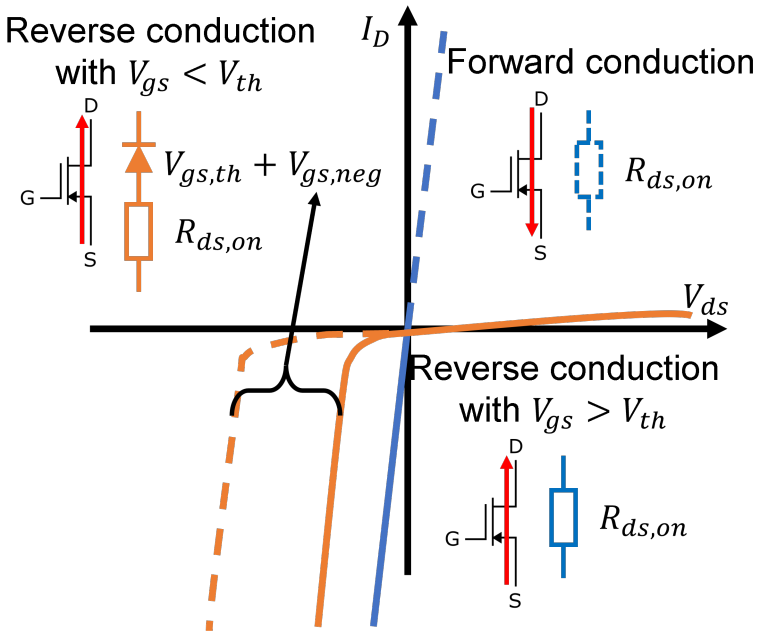


Fig. 2.28 GaN device forward and reverse conduction characteristics.

When a negative driver voltage is used to pilot the device in the OFF state, this negative drive voltage increases the reverse conduction offset voltage and thus worsen the reverse conduction losses. As in Si MOSFET, these losses occur only in the dead-time event. This threshold phenomenon is then avoided turning ON the device. Compared to standard device, the dead-time losses can be more relevant in the converter efficiency. The negative gate voltage is often utilized to prevent the device false turn ON. Hence, it must be carefully considered the trade-off between dead-time loss and gate driver noise immunity in the OFF state.

Current Collapse Phenomenon

The current collapse phenomenon is the temporary increase of the conduction resistance immediately after the turn ON event. It is also known as dynamic $R_{ds,on}$. This is mainly caused by the conduction of the electron trapped in unwanted crystalline defects of the various materials. In order to maintain the charge neutrality, the 2DEG electron density is reduced causing a temporary on resistance increment. As soon as these electrons are all de-trapped, the dynamic $R_{ds,on}$ returns to its static value. It requires a finite time which depends on the trap location, their energy level and the device temperature [103].
The two main mechanisms involved in this electron trapping phenomenon are the OFF-state trapping and the hot-electron trapping [104]. The first one consists in some electrons trapping induced by the applied drain-to-source voltage. The latter phenomenon occurs during the switching event (i.e. voltage and current overlap period) [105]. The overall effect is the increase of the conduction losses. As a consequence, this phenomenon has been deeply studied and now manufacturers can mitigate it through the elongation of the source and gate field plate as shown in Fig. 2.29 [106]. This solution makes a more distributed gate-to-drain electric field [107].

Another solution to eliminate the current collapse phenomenon is the Hybrid-Drain (HD) GIT structure proposed by Panasonic and shown in Fig. 2.30. It features a recessed p-GaN gate. Moreover, an additional p-GaN layer is located near the drain and connected to it. This structure has the duty to inject holes which are going to recombine to the trapped conduction electrons.

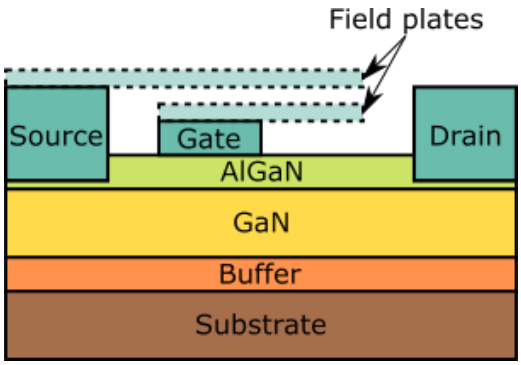


Fig. 2.29 GaN layer structure with gate and source field plates elongation to mitigate the current collapse phenomena.

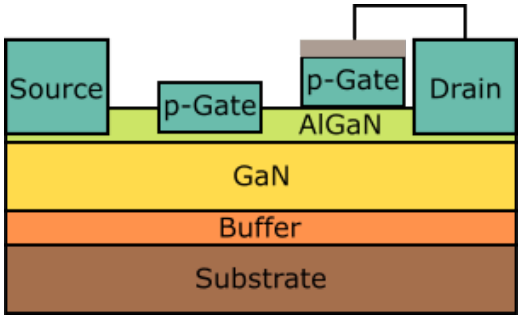


Fig. 2.30 HD GaN GIT layer structure.

GaN Device Breakdown

The breakdown voltage V_{BD} is one of the most important parameter for semiconductor transistors as it represents the maximum electrical field which can be applied to the power switch. By overcoming this value, the power switch fails and starts to conduct current. As a consequence, this fundamental constant has a great impact on the converter design.
In vertical power switch structure, the V_{BD} limiting factor is the material breakdown electric field (E_c). Since E_c is much higher compared to Si, GaN semiconductor has a great potentiality. Tacking into account that the commercially available GaN device have a lateral structure, the limiting factor results the surface material dielectric strength [91].
The breakdown mechanism differs from Si material. Indeed, for silicon MOSFET the failure is due to the avalanche breakdown across the pn junction. Under avalanche condition, the parasitic bipolar transistor can be turned ON causing the device failure [108]. To avoid these conditions, the manufacturer recommend to not overcome the

rated breakdown voltage.
On the other hand, GaN lateral device presents a dielectric breakdown mechanism. GaN power switches are built with a large safety margin. This difference is shown in Fig. 2.31, where the drain leakage current versus the applied drain-to-source voltage qualitative characteristic is compared between silicon and GaN 650V rated devices. While Si MOSFET goes in avalanche breakdown in a defined voltage value (i.e. between 650V and 700V), the GaN power switch can withstand more than 800V (i.e. typical value for Transphorm and Nexperia cascode devices). As a consequence they have a transient voltage capability, which is usually specified in the component datasheet (i.e. usually both the maximum transient voltage and the maximum time period are pointed out). The reason for this high margin is explained by the life-time models which are limited by the overvoltage events [91].

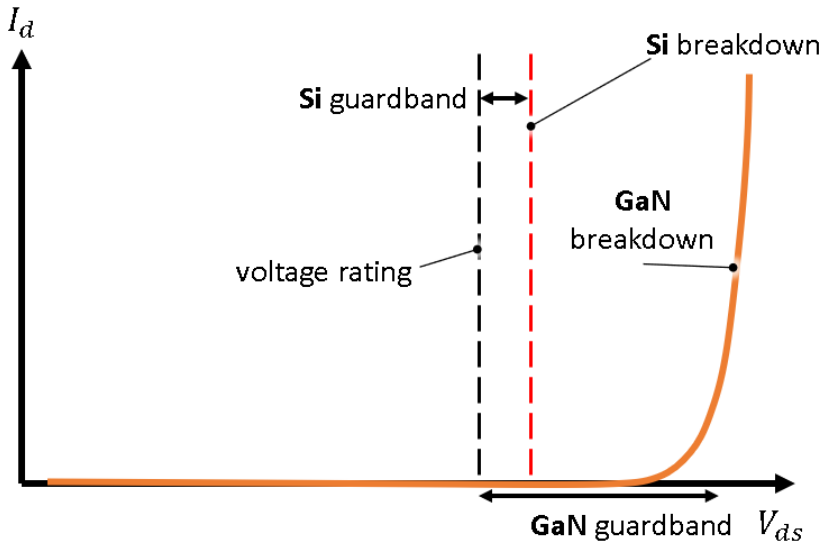


Fig. 2.31 Leakage current versus the drain-to-source voltage characteristics of the GaN devices. Due to the different breakdown mechanism GaN and Si devices have different guardband.

In Fig. 2.32 a static and dynamic breakdown voltage characterization is presented for the 650V VisIC V22TC65S1A direct drive device [99].

In particular, the static characteristic of the VisIC device under test (DUT) is shown in Fig. 2.32 (a); a breakdown voltage of 1600V (i.e. measured at $I_d = 250\mu A$) can be noted, much higher than the voltage rating of the DUT. The Fig.2.32 (b) shows a safe dynamic voltage application, while Fig. 2.32 (c) shows a device breakdown failure under a dynamic voltage of around 2000V.

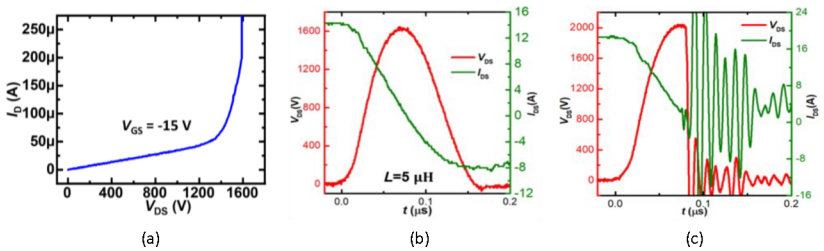


Fig. 2.32 VisIC V22TC65S1A (a) static breakdown voltage characteristic and dynamic breakdown voltage test (b) safe withstand and (c) device failure [99].

2.3.3 Future Trends

The electrification in the vehicle involves both low power (i.e. auxiliary systems) and high power (i.e. traction inverter) converters. As shown in Fig. 2.33, the semiconductor market will have a big growth in the next years [8]. These needs create a highly competitive environment among the different power switches technologies. The constant need of improvements brought to the adoption of wide band-gap material such as GaN and SiC that are gradually replacing the mature silicon based devices. Although this has already represented the biggest change from the adoption of silicon MOSFET in the seventies, the research to further improve and develop these new technologies does not stop.

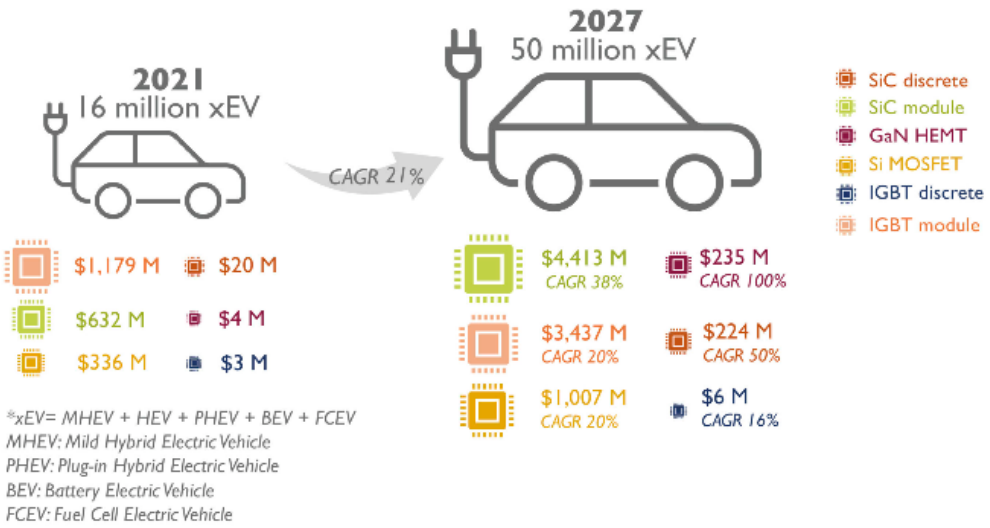


Fig. 2.33 Yole Group power semiconductor marker analysis and forecast [8]. CAGR=Compound Annual Growth Rate (mean annual growth rate over one year).

With focus on the GaN technology, in the next future three main research trends will be performed (Fig. 2.34):

- **Development of vertical GaN devices**: With the rising availability of reliable GaN substrate, the vertical structure can be adopted to rise the voltage and current ratings of the devices.
- **Circuit integration and smart devices**: Regarding the lateral devices, the monolithic integration of components such as sensors, protections and gate drivers represents an interesting approach to improve its reliability and the robustness of the component. With the reduction of the parasitic components higher switching frequency is feasible, introducing the possibility to increment the overall converter efficiency and power density.
- **Development of GaN power modules**: They are often preferred to discrete components because they simplify noticeably the final inverter assembly.

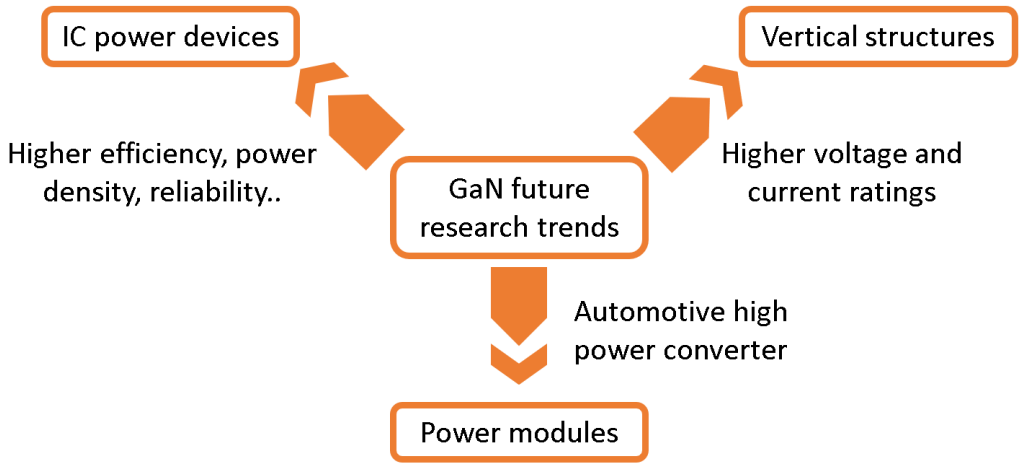


Fig. 2.34 The next future three main research trends will include the vertical structures, the IC power devices and the power modules.

Vertical Structure

As stated before, the GaN market will meet its next growth in the automotive high power converter (i.e.traction inverter and OFF board chargers). This explains the great interest in high voltage devices [109], [110]. Taking into account that the Dc-Link voltage automotive standard is shifting to 800V, 1200V rated device enables the use of simple and robust two-level inverter topology.
Up to now, the maximum commercial GaN device voltage ratings is limited to 650V.

The main problem in reaching high voltage ratings is in the lateral structure. As a matter of fact, growing GaN on a non-native substrate is particularly difficult due to the material lattice mismatch (i.e. proportional to the material defect generation) and the difference in thermal expansion coefficient (i.e. proportional to the material strains generation) [87]. Fig. 2.35 compares these parameters for different possible GaN substrates. Higher voltage rating requires thicker epitaxial layers. Consequently, the strain CTE management becomes more difficult to handle in the device [84]. Moreover, in a lateral structure the breakdown voltage is mainly limited by the gate-drain distance. As a consequence, a high voltage rating requires a big device area, increasing the device ON-resistance and cost [111].
In literature, two main research trends can be found. The first one consists in manufacturing high voltage devices with lateral structure (i.e. employing non native substrate). Some experimental devices that achieve up to 1200V of breakdown voltage ratings employing lateral GaN-on-Si structure are illustrated in [112–114]. On the other hand, the Saphhine substrate shows a GaN compatible thermal expansion coefficient and a lower lattice mismatch than Si (i.e. Fig. 2.35). For these reasons, compared to the GaN-on-Si structure, the Sapphine substrate requires a lower buffer layer thickness, translating in a easier manufacturing process and a reduced device cost [115]. Therefore, GaN-on-Sapphire devices represent an promising structure for 1200V GaN power devices. Also manufacturer industry shows interest in this field [116].

On the other hand, the second research trend focuses on the vertical structure as a solution to achieve higher currents and voltage ratings [110]. The main obstacle to the realization of vertical GaN device is the difficulty related to the production of a reliable and low cost GaN substrate [118]. Nowadays, GaN substrates with an acceptable low dislocation density have become more and more available on the market enabling the firsts vertical GaN experimental devices. However, it is important to underline that TD are still relatively high compare to Si and SiC substrate [119].

The vertical structure is made of a GaN substrate over which the other layers are grown through the MBE or MOCVD techniques [119]. Due to the presence of the native GaN substrate, there is an homoepitaxial growth. As a consequence there are not thermal mismatch problem in contrast to lateral devices where heteroepitaxial growth between GaN and Si substrate causes a CTE mismatch problem (i.e. there is need of a buffer layer). To sum up, this is an important advantage because it

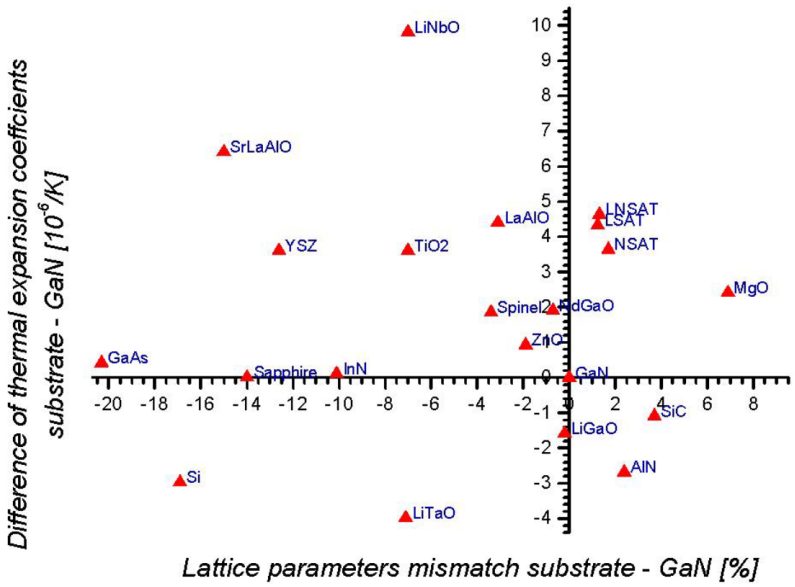


Fig. 2.35 CTE parameter and lattice mismatch comparison for different substrate material [117].

enables the growth of thicker and more reliable (i.e. with less defects) drift layer, thus enabling higher voltage ratings. Indeed, in vertical devices the drift region design is a crucial structure element. It is often a trade-off design point. To achieve high voltage ratings, the options are to increase the thickness or to lower the doping of drift region. On the other hand, the on state resistance is inversely proportional to its doping level [119]. Moreover, the vertical structure stands the voltage vertically, thus the critical electric field feature of the GaN material is fully exploited [91]. This enables smaller devices compared to lateral structure (i.e. limited by the high gate-drain distance required in high voltage ratings) with lower specific $R_{ds,on}$ [120]. In literature the two mainly promising GaN vertical structures are:

- **Current aperture vertical electron transistors CAVETs**: as shown in Fig. 2.36 (a) the CAVET structure includes a GaN substrate on which a GaN n^+ buffer and drift layer are epitaxially grown. Two current blocking layer CBLs are positioned in the drift layer to define the current aperture that will be the current channel of the transistor. Over the drift layer, an Al/GaN is formed. The 2DEG conductive channel is originated at the hetero-junction interface as explained for lateral devices. When the gate is positively biased (i.e. over its threshold value), the currents flow firstly laterally through the 2D electron

gas and then vertically in the aperture defined by the CBLs [121]. Finally, different gate structures are possible such as the insulated gate (Fig. 2.36 (a)), the p-GaN gate (Fig. 2.36 (b)). These devices present a very low gate threshold voltage. An higher threshold value can be obtained with the trench p-GaN gate shown in Fig. 2.36 (c) [109]. The main disadvantages of these devices are related to the complicated structure and the consequently complex epitaxial regrowth processes [110].

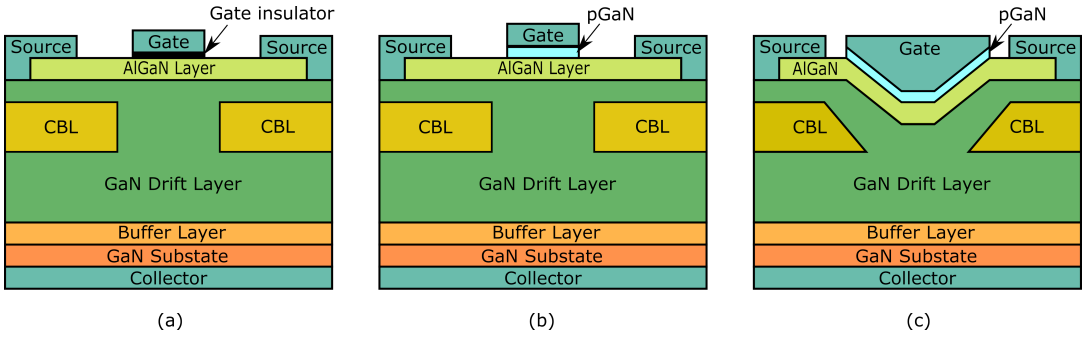


Fig. 2.36 Vertical GaN layer structure of (a) CAVET with insulated gate structure, (b) CAVET with p-GaN gate structure, (c) CAVET with trench gate structure.

- **Trench MOSFETs**: devices of this kind with a voltage rating up to 1600V have been reported in literature [111], [122]. The threshold voltage is relatively high compared to CAVETs. The main disadvantages of these devices are the low channel mobility and high gate voltage needed (i.e. > 30V) to fully enable the conductive channel. Also in this case, there are manufacturing difficulties especially the ohmic contact forming [109]. Fig. 2.37 shows the GaN trench MOSFET layer structure.

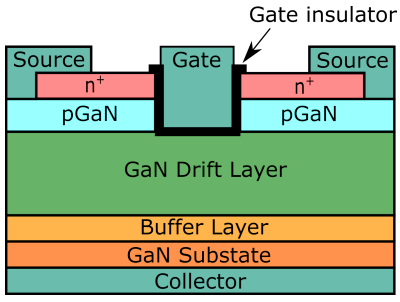


Fig. 2.37 Vertical GaN trench MOSFET layer structure.

In conclusion, several manufacturing attempts have been made in literature to develop vertical GaN structures since the initial availability of GaN substrate. The

vertical structure offers higher voltage and current rating possibilities compared to the lateral one. However, the fabricating process is still under studies and certainty these devices are far from maturity. It is interesting to notice that the GaN journey has just begun. Indeed, when the vertical structure will become mature, the superjunction concept could be implemented to further enhance the GaN performances as shown in Fig. 2.38 [10].

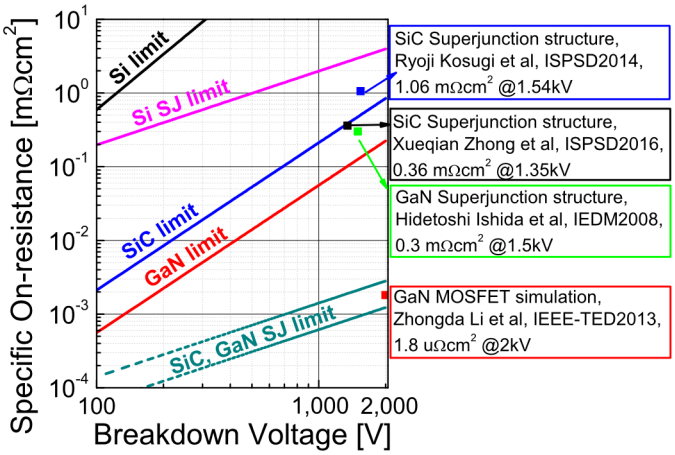


Fig. 2.38 Theoretical $R_{ds,on}$ limit related to the breakdown voltage [10]

Circuit integration and Smart Devices

A great advantage of the GaN lateral structure is the possibility to combine the power switch with other circuitry in the same package through monolithic integration [123]. Integrated Circuit (IC) power devices can be thought as a block with digital inputs and a power output. Indeed, signal transistors, diodes and even passive components like resistors and capacitors can be integrated in the device [124], [125]. The aim is to build substitutive functional block of the external components to eliminate relative parasitic elements originated by the bonding wire and PCB connections in a similar way described in the Direct Drive device section. The most required functions are the gate driver stage, the driver voltage regulator, the current sensing, the over-current and over-temperature and the commutation slew-rate control [126–129]. Circuit integration presents many benefits, such as:

- The reduction of the gate loop parasitics element due to the gate driver integration drastically mitigates the voltage spikes and oscillation. To further enhance

the gate driver robustness, a voltage supply regulator can be also integrated. This is particularly appreciated in the HEMT devices with a noise susceptible driver stage;

- The temperature sensing is made directly on the device. As a result, the over-temperature results faster and more precise compared to a standard solution (i.e. usually the temperature measurement is taken on the heat-sink far away from the switch);
- In a similar way to the previous point, the integration of the over-current protection helps to reduce the intervention time and to increase the reliability (i.e. the measurement is taken directly on the device);
- The integration of current sensing eliminates the parasitics introduced by an external sensor (i.e. shunt resistor) thus improving the commutation loop;
- The external component reduction leads to a more compact PCB design and a noticeable cost reduction. Moreover, the IC device results easier to use and to handle compared to a discrete components solution;
- The commutation slew-rate setting is very useful to manage the converter EMI compatibility.

IC power devices represent a strong research field not only in academia. Several manufacturers such as Navitas, EPC, ST Microelectronics and Texas Instruments have realised several products on the market. The latter includes also devices with two switch integrated in half-bridge topology. Fig. 2.39 shows the GaN market subdivision between IC and discrete devices outlying the main manufacturer. It is interesting to notice that GaN ICs are implemented in both enhancement and depletion (i.e. Direct Drive configuration) mode structures.

To summarize, IC power devices are a very interesting solution to enhance the switching frequency, the efficiency and the power densities of power converters [130]. Moreover, the gate driver, the sensing and the protection integration contribute to enhance the component reliability, which is a key feature in power electronic converters. As a consequence, the power IC market is already well established in the mobile and consumer markets and in the next future it will grow further in the automotive applications [131], [132].

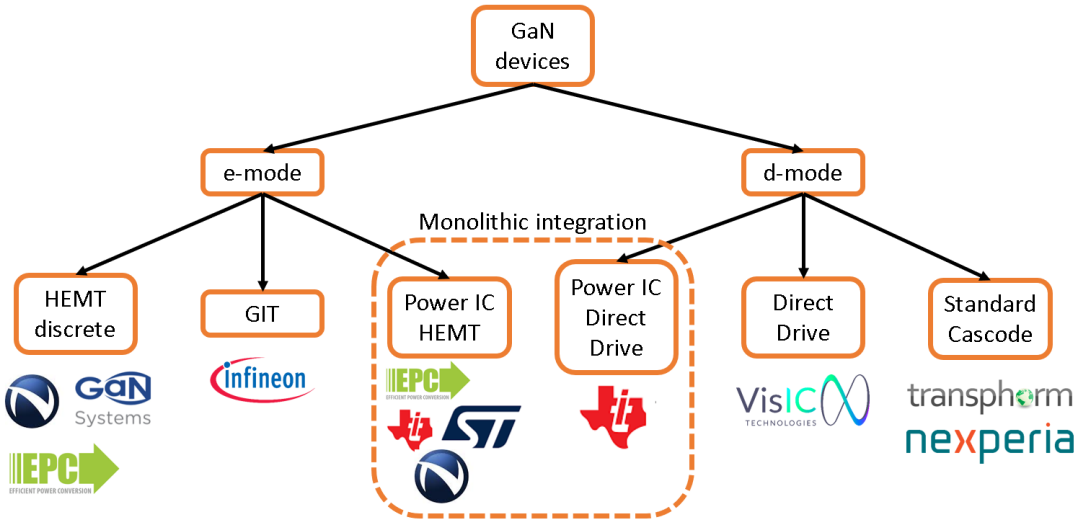


Fig. 2.39 GaN devices available on on the market divided by structure.

GaN Power Module

GaN devices enable higher switching frequency operation due to faster commutation speed and to the lower overall losses [94]. This brings to new design challenges related to the thermal management and parasitic oscillation handling. As a consequence, the power and driver commutation loops must be carefully designed to minimize parasitic inductances (L_σ) [133].
In addition to the PCB design optimization, also the device package has an important influence on the converter performances. Classical discrete packages such as TO-220 or TO-247 introduce an high parasitic inductance due to the long leads [100]. For this reason, it is often preferred a surface mounted package to reduce the device parasitic inductance. Each manufacturer has its own property package. Until now, there is no winning standard yet. At the time of writing, GaN devices are mainly marketed in discrete packages. As explained before, the next growth in GaN market will take place in the high power automotive converters [24]. Some manufactures have announced industry collaboration with the aim to produce traction inverters [61, 63, 66]. The majority of these converters seem to utilize discrete devices. On the other hand, a power module is often preferred to simplify the inverter assemble and thermal management [9]. The power module market is estimated to double from 2020 to 2026 according to studies performed by Yole Group [134], [135]. To follow the market requirements, the firsts high power rated modules have been recently commercialized in particular from VisIC [136] and GaNSystem [137]. These prod-

ucts are still not fully commercial. Also some module prototypes are presented in literature [138]. Currently GaN power modules are limited to 650V rating and thus usable only in 400V Dc-Link voltage supply.

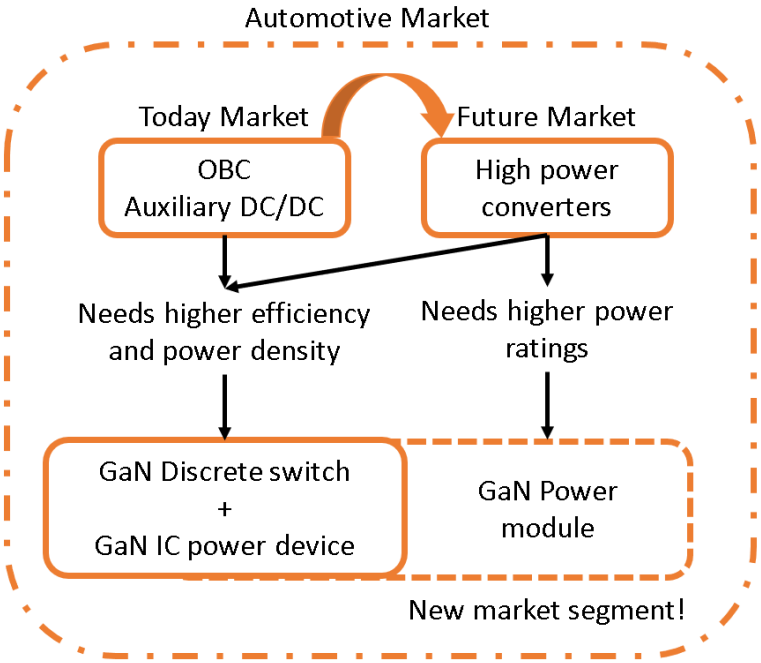


Fig. 2.40 Automotive market future prospect and needs according to the presented literature review.

2.4 FOM Based Device Comparison

The Figure of Merit (FoM) is an easy and effective tool to compare both the materials and devices properties. In this section different FoM are briefly presented in order to choice the best active switch for the target application. WBG devices are identified as a key technology which lead to an improvement in efficiency and power density of future traction inverters compared to standard Si technology. While SiC devices are now established in the automotive sector, GaN power switches are just entering in this market promising better theoretical performances but with a low maturity degree. As a consequence there is uncertainty on which is the best semiconductor for the next generation EV inverters. This section wants to give a performance comparison for the commercially available SiC and GaN device to drive the best power switch selection. This study focus on 600/650 voltage rating devices which can be employed in both

400 and 800 DC-Link voltage architectures (i.e. employing multilevel topologies) [139, 140]. As will be delve deeper into the topic, non-standard converter topologies (i.e. different by the two-level structure), such as multilevel converter, can combine well with this new technologies further exalting the benefits. Concluding, in this section the half-bridge hard-switching loss components are firstly presented. Then, the most popular FOM are analysed. Finally, the best ones are identified to compare 600/650V SiC and GaN devices taking into consideration also the converter switching frequency and its operating temperature. All the arguments treated in this section are published in [141].

2.4.1 Half-bridge Hard-switching Loss

The hard-switching losses for a two-level leg can be divided into two contributions: the conduction losses P_{cond} and the switching losses P_{sw}.

$$P_{tot} = P_{cond} + P_{sw} \tag{2.2}$$

The conduction losses depend on the device on resistance and on the RMS current I_{RMS} which flows in it, as illustrated in the following equation:

$$P_{cond} = R_{ds,on} I_{RMS}^2 \tag{2.3}$$

On the other hand, the switching losses include all the mechanisms which depend on the switching frequency f_{sw}. They can be divided into five contributions expressed as:

$$P_{sw} = P_g + P_{dt} + P_{oss} + P_{rr} + P_{vi} \tag{2.4}$$

where P_g is the gate driving loss, P_{dt} are the losses ascribed to the dead-time reverse conduction, P_{oss} are the losses related charge/discharge of the device output capacitance, P_{rr} is the reverse-recovery loss, P_{vi} a the losses due to the current and voltage overlap during the commutation.
The gate driving losses are described by the following equation:

$$P_g = f_{sw}(V_{g,on} - V_{g,off})Q_g \tag{2.5}$$

where $V_{g,on}$ and $V_{g,off}$ are the gate voltage levels and Q_g is the total gate charge. Usually, for high-voltage hard-switching operations, they represent the lowest contribution. These losses will be thus neglected in the following analysis.
The dead-time is used to avoid short-circuit that can occur during the devices turning ON/OFF in power electronics converter. In this period, the losses are generated by the current conduction in device the body diode (or in the equivalent body diode of the self-commutated reverse conduction phenomena for HEMTs). This loss is proportional to the difference between the dead time (t_{dt}) and the time to complete the zero-voltage switching (t_{ZVS}) [142] and the diode voltage drop (V_d). It can be expressed as:

$$P_{dt} = f_{sw}I_{sw}V_d(t_{dt} - t_{ZVS}(I_{sw})) \tag{2.6}$$

where I_{sw} represent the commutated current. These losses can be minimized by a proper adaptive dead-time control (i.e. considering that t_{ZVS} is current dependent) [143, 144]. As a consequence, also these losses will be neglected in the following analysis.
Another important contribution in the switching losses is the charging/discharging process of the transistor output capacitance that take place during each switching period. Knowing the commutated voltage V_{sw}, the switching frequency and the charge stored in C_{oss} at V_{sw} (Q_{oss}), this loss can be expressed as:

$$P_{oss} = f_{sw}V_{sw}Q_{oss}(V_{sw}) \tag{2.7}$$

A similar loss behaviour is related to the charge stored in the device bipolar diode. This phenomenon does not occur for HEMT transistor due to the fact that there is no pn junction and thus no parasitic body diode. This loss contribution is described as:

$$P_{rr} = f_{sw}V_{sw}Q_{rr}(I_{sw}) \tag{2.8}$$

where Q_{rr} is the reverse recovery charge which depend by the commutated current.

The last loss contribution considered is due to the voltage and current overlap that occur in the device channel during the turn-ON transition [141]. It features two loss contribution depending on the voltage and current derivatives:

$$P_{vi} = f_{sw}\left(\frac{1}{2}\frac{V_{sw}^2}{dv/dt}I_{sw} + \frac{1}{2}\frac{I_{sw}^2}{di/dt}V_{sw}\right) \tag{2.9}$$

In order to properly compare different devices, it should be identified a performance index which does not depend on the driving or the external parasitic properties. This can be represented by the minimum theoretical losses related to the device. From this prospective, the hypothesis of infinite switching derivatives (i.e. $di/dt \approx \infty$, $dv/dt \approx \infty$) can be made. Under this assumption, the overlap losses can be neglected ($P_{vi} \approx 0$) and thus the minimum switching losses depend only by the charge-related loss mechanisms. Moreover, considering $di/dt \approx \infty$, the charge recombination process in the diode has no time to happen, consequently the charge due to the forward bias polarization is given away as Q_{rr} [145]. Hence, under these conditions the reverse recovery charge is linearly dependent on the commutated current as in the following expression:

$$Q_{rr} \approx \tau_{rr} I_{sw} \tag{2.10}$$

where τ_{rr} represents the time in which occur the charge carrier recombination. Summarizing, considering all the previous assumptions, the theoretical minimal switching losses can be expressed as:

$$P_{sw} \approx f_{sw} V_{sw}[Q_{oss}(V_{sw}) + Q_{rr}(I_{sw})] \tag{2.11}$$

2.4.2 Figure of Merit Review

In literature there are different FOM types to compare the different analysed aspects of the semiconductor technology. The main classifications are at material-level [19, 146], at the device-level [18, 147, 148] and at the converter structure-level [149]. This paragraph briefly presents the principal device-level FOMs and outlines the best ones that can be used to select the optimal device for the considered application. The main device-level FOM analysed are:

- *Baliga High-Frequency Figure-of-Merit* (BHFFOM)[18]: this formulation assumes that the switching losses are represented by the charging/discharging process of the device input capacitance C_{iss} and the conduction losses are quantified by the on resistance according to the following equation:

$$BHFFOM = \frac{1}{R_{ds,on}C_{iss}} \tag{2.12}$$

  Since the switching loss hypothesis is not valid for high-voltage power switches (i.e. where $C_{oss}V_{ds}^2 \gg C_{iss}V_g^2$), the BHFFOM will not be used in the considered application.

- *New High-Frequency Figure-of-Merit* (NHFFOM) [147] is very similar to the previous one with the substantial difference of relating the switching losses to the charge/discharge of the output device capacitance C_{oss} as illustrated in the following equation:

$$NHFFOM = \frac{1}{R_{ds,on}C_{oss}} \tag{2.13}$$

  Even if this assumption is feasible for high-voltage devices, the high voltage value of the non-liner output capacitance is still not representative of the power switch parasitic capacitive losses (i.e. the charge-equivalent output capacitance should be considered) [142]. For this reason also this FOM is not considered in the following analysis.

- *Huang Device Figure-of-Merit* (HDFOM) [148], contrary to the other FOM, assumes that the switching losses due to the voltage and current overlap are dominant compared to the other contributions. Since the Miller charge (i.e. the gate charge during the Miller-plateau period is directly related to the voltage transition, the HDFOM is then defined as:

$$HDFOM = \sqrt{R_{ds,on}Q_{gd}} \tag{2.14}$$

  where the gate-to-drain charge Q_{gd} is the charge related to the gate-to-drain parasitic capacitance C_{gd} during the voltage derivative.

- *Switching Figure-of-Merit* (SFOM) [150] is an extension of the HDFOM. Indeed, to include also the current transition contribution in the VI overlap

loss, the FOM is modified adding a second gate charge contribution:

$$SFOM = R_{ds,on}(Q_{gd} + Q_{gs,i}) \tag{2.15}$$

where $Q_{gs,i}$ is the charge related to the gate-to-drain parasitic capacitance C_{iss} during the current derivative. Both HDFOM and SFOM are not considered to compare semiconductor technologies due to the fact that both does not consider the minimum theoretical switching losses related to high-voltage fast-switching devices as illustrated in the previous chapter.

- *Device Figure-of-Merit* (DFOM) proposed in [149] is similar to the NHFFOM with the difference of using the charge equivalent output capacitance $C_{oss,Q}$. Indeed, it provides a better representation of the device parasitic capacitive losses as illustrated in [142]. It has the following expression:

$$DFOM = \frac{1}{\sqrt{R_{ds,on}C_{oss,Q}}} \tag{2.16}$$

  The DFOM is inversely proportional to the minimum theoretical half-bridge hard-switching loss for devices in which the reverse recovery loss contribute is negligible or not present. For example, this assumption is valid for e-mode and direct-drive cascode GaN power switches. On the other hand, the DFOM is less effective to compare the more standard Si and SiC semiconductor technology.

- *Hard Switching Figure-of-Merit* (HSFOM) has been proposed in [141] to address the DFOM limit in a proper semiconductor technology comparison. Considering all the hypothesis made in the previous subsection, the minimum theoretical hard-switching losses for an half-bridge leg can be modelled as:

$$P_{tot} = \frac{r_{ds,on}}{A_{semi}} I_{RMS}^2 + f_{sw} V_{sw} (q_{oss} A_{semi} + \tau_{rr} I_{avg}) \tag{2.17}$$

  where the $r_{ds,on} = R_{ds,on} A_{semi}$ and $q_{oss} = \dfrac{Q_{oss}}{A_{semi}}$ are respectively the specific on resistance and the specific output capacitance of the considered device. Moreover, A_{semi} is defined as the semiconductor chip area and I_{avg} is the average current in the fundamental period analysed. The minimum chip size is obtained imposing the total loss trend equal to zero (i.e. $dP_{tot}/dA_{semi} = 0$):

$$A^*_{semi} = \frac{I_{RMS}}{\sqrt{f_{sw}V_{sw}}}\sqrt{\frac{r_{ds,on}}{q_{oss}}} \tag{2.18}$$

From this equation it can be deduced that the reverse recovery loss does not contribute to define the optimal semiconductor chip area. Hence, substituting (2.18) in (2.17), the expression of the total losses become:

$$P^*_{semi} = 2I_{RMS}\sqrt{f_{sw}V_{sw}r_{ds,on}q_{oss}} + f_{sw}V_{sw}I_{avg}\tau_{rr} \tag{2.19}$$

where two different parameter types can be distinguished: the ones related to the semiconductor technology (i.e. $r_{ds,on}, q_{oss}$ and τ_{rr}) and the ones related to the converter operating conditions (i.e. f_{sw}, V_{sw}, I_{RMS} and I_{avg}). Finally, expressing both the average and the RMS current in relation to the converter output peak current, the minimal theoretical semiconductor losses dependencies result:

$$P^*_{tot}\alpha\sqrt{r_{ds,on}q_{oss}} + k_i\sqrt{f_{sw}V_{sw}}\tau_{rr} \tag{2.20}$$

where the coefficient k_i is equal to $\sqrt{2}/\pi$ and the term q_{oss} is non-linearly dependent by the DC-Link voltage if a two-level inverter is considered. Once the loss model is defined, the HSFOM is expressed as:

$$HSFOM = \frac{1}{\sqrt{R_{ds,on}Q_{oss}} + k_i\sqrt{f_{sw}V_{sw}}\tau_{rr}} \tag{2.21}$$

It must be outlined that for very low switching frequencies or when the considered device has a negligible reverse recovery loss contribution (i.e. $\sqrt{R_{ds,on}Q_{oss}} \gg k_i\sqrt{f_{sw}V_{sw}}\tau_{rr}$), the HSFOM has a similar formulation to the DFOM (i.e. with the substitution of the charge-equivalent output capacitance with Q_{oss}). As explained before, the HSFOM is proportional to the proposed minimal theoretical half-bridge hard-switching loss proposed model. Even if the VI overlap contribution has been neglected, the HSFOM results a good performance comparison index for different semiconductor technologies which become more and more accurate as faster switching transitions are considered (i.e. the commutation derivatives increment is related to external factors difficult to predict such as the gate driving conditions and the parasitic loop

inductances minimization). Similarly to the loss model analysed, the HS-FOM includes some parameters related to the semiconductor technology (i.e. $R_{ds,on}, Q_{oss}$ and τ_{rr}) and some related to the converter operating conditions (i.e. f_{sw}, V_{sw}). Indeed, defined the switched voltage V_{sw}, the HSFOM depends substantially by the switching frequency and by the semiconductor junction temperature T_j. While the first parameter affects the reverse recovery loss contribution, the second one influences the on resistance and τ_{rr} (i.e. thus both conduction and switching loss contributions are conditioned). T_j is often neglected in these analyses, while it is a very important aspect which can change substantially the FOM performance comparison.

In literature, lots of FOM analysis have been carried out to compare the properties of different semiconductor devices. Most of them identify a loss model based on the gate parameters and on the on resistance similarly to the SFOM [104, 133, 151, 152]. In accordance to reported analysis, these comparisons are less significant for fast-switching, high-voltage power devices and thus a new approach must be identified for this study.
To sum up, after this critical FOMs review, it results that the proposed HSFOM is based to a minimal theoretical hard-switching model which well describe the total device loss for the considered application. As consequence, the latter FOM is selected to properly address the performance comparison for different high-voltage high-switching frequency semiconductor technology in the following analysis.

2.4.3 $R_{ds,on}Q_{oss}$ Comparison

With the aim to provide a proper comparison, all the commercially available GaN and SiC devices belonging to the major manufacturer have been considered in this analysis. In the following paragraph, a preliminary semiconductor technology evaluation is performed considering the $R_{ds}Q_{oss}$ product in a similar approach identified by the DFOM. While R_{ds} is always reported in the device datasheet, Q_{oss} parameter is less frequent. When it is not reported, it can be calculated by the output capacitance integral as:

$$Q_{oss} = \int_0^{V_{sw}} C_{oss}(v)\, dv \tag{2.22}$$

where v is the commutated voltage set at $V_{sw} = 400V$. Once all these parameters are available, average $R_{ds}Q_{oss}$ products are calculated considering all the devices belonging to the same producer. This represent a performance index directly related to the semiconductor technology owned by each manufacturer. These data are reported in Table 2.2 and 2.3 respectively for GaN and SiC devices. Moreover, a graphically representation is illustrated in Fig. 2.41 and 2.42 considering $T_j = 25^oC$ and in Fig 2.43 and 2.44 considering $T_j = 150^oC$. Since lower $R_{ds}Q_{oss}$ product means lower conduction and switching losses, it can be pointed out that SiC devices outperform most of the considered GaN devices. In particular, the best performance is obtained by the Infineon GaN e-mode HEMT (GIT). On the other hand, the GaN cascode d-mode HEMT has worst $R_{ds}Q_{oss}$. Interestingly, the GaN cascode direct-drive d-mode HEMT from VisIC presents a performance index more similar to GaN e-mode HEMT differing substantially from other classical cascodes. Looking at Fig. 2.41 and 2.42, it is clear that SiC devices have a more uniform behaviours while GaN devices differ more widely depending on the adopted technology. This is mainly due to the fact that for SiC devices there is a more affirmed technology while for GaN devices there is no a clear winning standard structure yet. Another important result of the analysis is the importance of including T_j in the performance comparison of different semiconductor technology. Indeed, Table 2.2 shows that GaN switches are much highly sensible to the operation temperature compared to SiC devices (i.e. ref to Table 2.3). This is clearly shown in Fig. 2.45 where the $R_{ds}Q_{oss}$ curves variation with the junction temperature are compared for SiC MOSFET from Wolfspeed and GaN direct-drive d-mode HEMT from VisIC. To sum up, this first analysis represents a semiconductor technology preliminary performance comparison which does not fully characterize all the loss aspects of hard switching application. However, this approach suggests that operating conditions must be considered in device FOM-based comparison because they can lead to unexpected results.

Table 2.2 COMMERCIALLY AVAILABLE 600/650V GAN DEVICES PERFORMANCE COMPARISON AT $V_{sw} = 400V$, $T_j = 25^oC$ AND 150^oC. THE REPORTED $R_{ds}Q_{oss}$ AND τ_{rr} ARE AVERAGED VALUES CONSIDERING ALL DEVICES BELONGING TO THE SAME MANUFACTURER. THE EXPRESSION 'N.A.' MEANS 'NOT AVAILABLE'.

Manufacturer	**Semiconductor Technology**	$R_{ds}Q_{oss}$		$\tau_{rr} = Q_{rr}/I_{sw}$	
		$T_j = 25^oC$	$T_j = 150^oC$	$T_j = 25^oC$	$T_j = 150^oC$
Infineon	GaN e-mode HEMT (GIT)	2.25 V/GHz	4.13 V/GHz	-	-
Navitas	GaN e-mode HEMT	3.10 V/GHz	7.25 V/GHz	-	-
GaN System	GaN e-mode HEMT	3.18 V/GHz	8.24 V/GH	-	-
VisIC	GaN direct-drive d-mode HEMT	3.52 V/GHz	6.95 V/GHz	-	-
Texas Instruments	GaN direct-drive d-mode HEMT	4.39 V/GHz	8.51 V/GHz	-	-
Nexperia	GaN cascode d-mode HEMT	5.75 V/GHz	11.86 V/GHz	≈ 0 ns	n.a.
Transphorm	GaN cascode d-mode HEMT	6.20 V/GHz	12.84 V/GHz	≈ 0 ns	n.a.

Table 2.3 COMMERCIALLY AVAILABLE 650V SIC DEVICES PERFORMANCE COMPARISON AT $V_{sw} = 400V$, $T_j = 25^oC$ AND 150^oC. THE REPORTED $R_{ds}Q_{oss}$ AND τ_{rr} ARE AVERAGED VALUES CONSIDERING ALL DEVICES BELONGING TO THE SAME MANUFACTURER. THE EXPRESSION 'N.A.' MEANS 'NOT AVAILABLE'.

Manufacturer	**Semiconductor Technology**	$R_{ds}Q_{oss}$		$\tau_{rr} = Q_{rr}/I_{sw}$	
		$T_j = 25^oC$	$T_j = 150^oC$	$T_j = 25^oC$	$T_j = 150^oC$
Wolfspeed	SiC MOSFET	3.23 V/GHz	4.00 V/GHz	5.95ns	9.10ns
RHOM Semiconductor	SiC MOSFET	3.59 V/GHz	5.03 V/GHz	0.83ns	n.a.
ON Semiconductor	SiC MOSFET	3.64 V/GHz	4.21 V/GHz	$\approx$0ns	n.a.
Infineon	SiC MOSFET	3.72 V/GHz	4.85 V/GHz	2.93ns	n.a.
ST Microelectronics	SiC MOSFET	3.75 V/GHz	5.06 V/GHz	1.06ns	n.a.

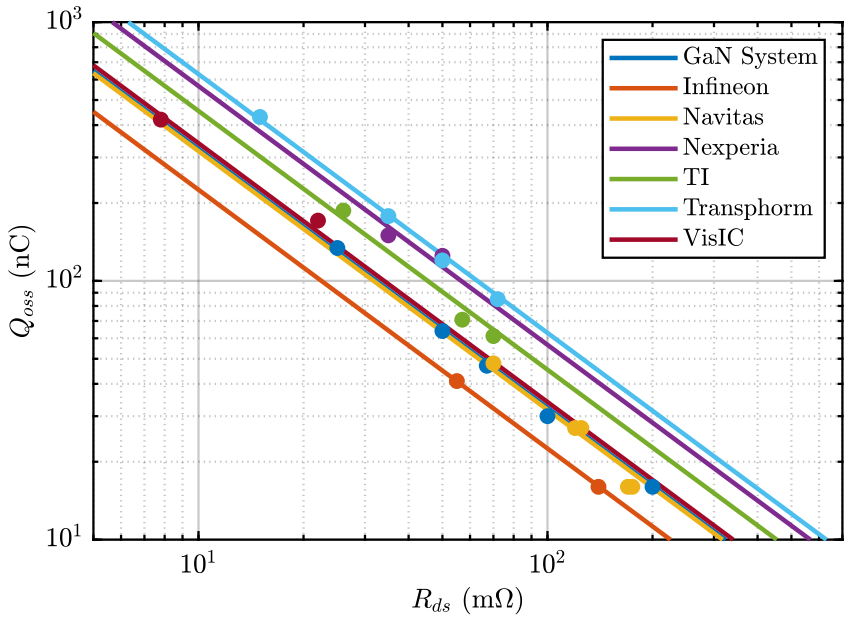


Fig. 2.41 600/650V GaN semiconductor technologies performance comparison considering $V_{sw} = 400V$ and $T_j = 25^oC$ operating conditions. The dots represent the single analysed devices parameters and the straight line depicts the average performance (i.e. $R_{ds}Q_{oss} = const$) behaviour of each semiconductor technology.

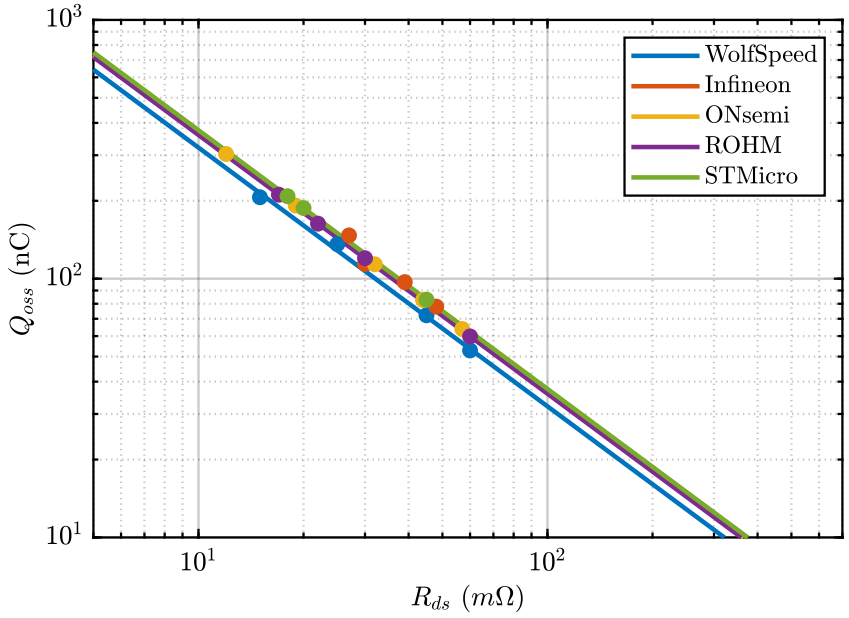


Fig. 2.42 650V SiC semiconductor technologies performance comparison considering $V_{sw} = 400V$ and $T_j = 25^oC$ operating conditions. The dots represent the single devices parameters and the straight line depicts the average performance (i.e. $R_{ds}Q_{oss} = const$) behaviour of each semiconductor technology.

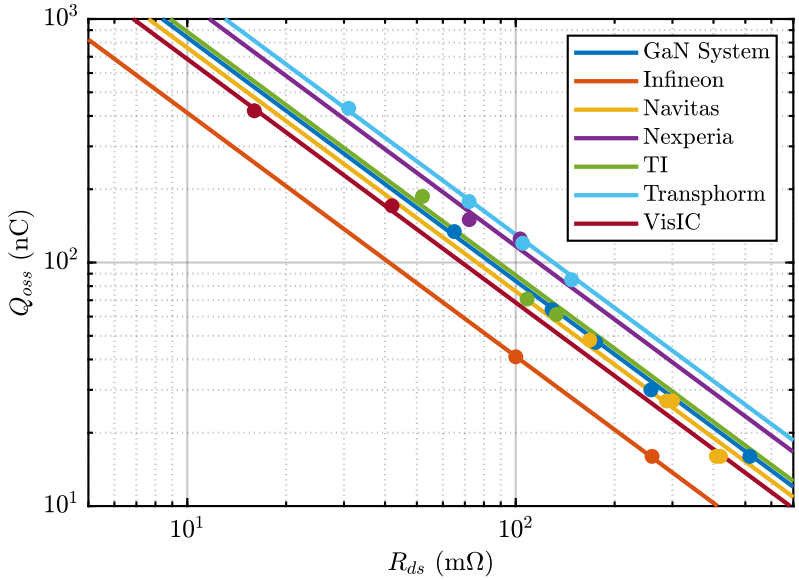


Fig. 2.43 600/650V GaN semiconductor technologies performance comparison considering $V_{sw} = 400V$ and $T_j = 150^oC$ operating conditions. The dots represent the single analysed devices parameters and the straight line depicts the average performance (i.e. $R_{ds}Q_{oss} = const$) behaviour of each semiconductor technology.

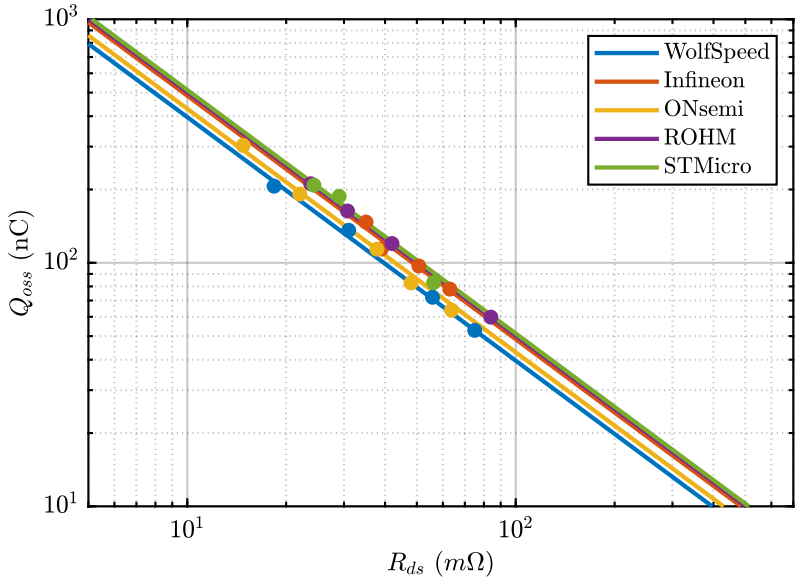


Fig. 2.44 650V SiC semiconductor technologies performance comparison considering $V_{sw} = 400V$ and $T_j = 150^oC$ operating conditions. The dots represent the single devices parameters and the straight line depicts the average performance (i.e. $R_{ds}Q_{oss} = const$) behaviour of each semiconductor technology.

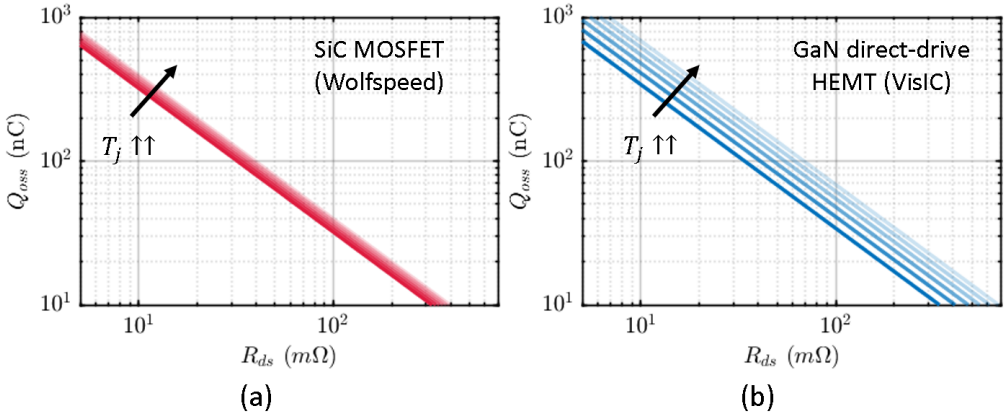


Fig. 2.45 Example of the junction temperature T_j dependence of the $R_{ds}Q_{oss}$ curves for different semiconductor technologies: (a) SiC MOSFET from Wolfspeed, (b) GaN direct-drive d-mode HEMT from VisIC. It has been considered $V_{sw} = 400V$ and variable junction temperature (i.e. $T_j = 25, 50, ..., 150^oC$).

2.4.4 HSFOM Comparison

The semiconductor technology comparison is now presented with the introduced HSFOM to overcame the $R_{ds}Q_{oss}$ theoretical limitations. Thus a more accurate performance analysis is outlined. For simplicity, only two manufacturers for each considered technology have been selected. For SiC MOSFET, Woolfspeed is chosen due to availability and pertinence (i.e. high di/dt value $\approx 5000A/\mu s$ test condition) of the device data. Indeed, the reverse recovery phenomenon is usually not fully characterised (i.e. Q_{rr} value is reported only for ambient temperature) or the test conditions are not consistent with the considered application (i.e. low di/dt value $\approx 1000A/\mu s$ does not properly match with the equation 2.10 assumption). On the other hand, GaN cascode direct-drive HEMT from VisIC has been considered due to the high current range, gate driver robustness and high $R_{ds}Q_{oss}$ performances. To obtain the τ_{rr} parameter, first of all the reverse-recovery charge is deprived by the Q_{oss} contribute and then the charge carrier recombination lifetime is calculated by inverting the equation 2.10. In a similar way explained for the $R_{ds}Q_{oss}$ product, all the calculated τ_{rr} are averaged for all the devices belonging to the same manufacturer in order to obtain a specific performance index related to their own semiconductor technology. These are reported in Tables 2.2 and 2.3.
The HSFOM curves are then calculated by using the equation 2.21 assuming AC sinusoidal operation and constant switched voltage (i.e. $V_{sw} = 400V$). A linear

interpolation has been used to describe the devices junction temperature dependence due to the low data availability. Finally, Fig. 2.46 shows the HSFOM curves for the Wolfspeed and VisIC semiconductor technologies. It is clear that only the SiC MOSFET presents a dependence on the switching frequency because GaN devices from VisIC are not affected by the reverse recovery loss contribution. As for the $R_{ds}Q_{oss}$ analysis, the GaN technology performance worsening is more evident with the junction temperature variation compared to SiC. However, Fig. 2.46 shows that there is always an intersection between the SiC and GaN curves. This means that there is a f_{sw} where GaN outperform SiC. This frequency depends mainly by the operating junction temperature.

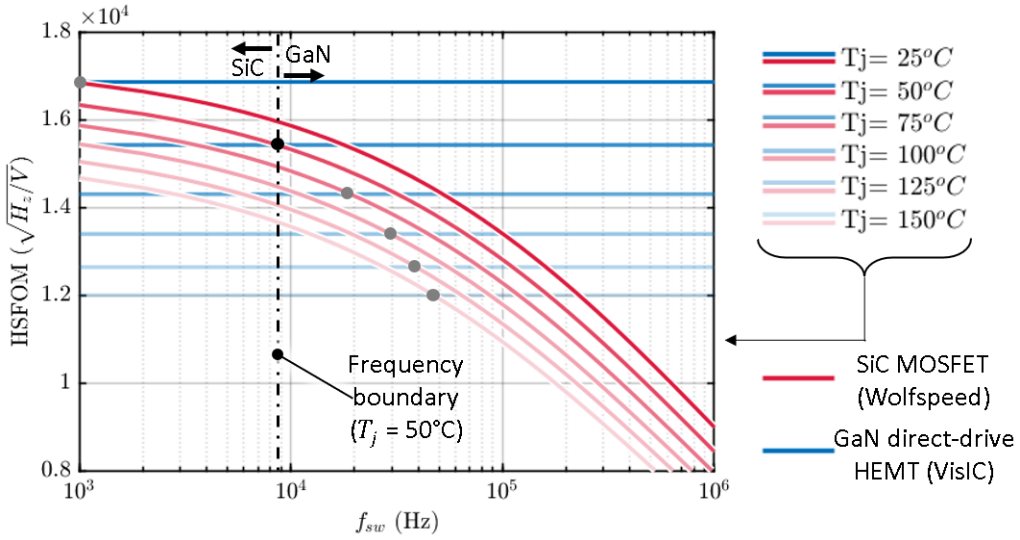


Fig. 2.46 Performance comparison of different semiconductor technologies based on the proposed HSFOM. SiC MOSFET from Wolfspeed (red colour) and GaN direct-drive d-mode HEMT from VisIC (blue color) HSFOM curves are shown for different junction temperatures (T_j) and switching frequency (f_{sw}) values. The grey dots identify the f_{sw} where GaN outperform SiC. This frequency boundary is clearly shown in black for $T_j = 50^oC$.

2.5 Conclusion

This chapter aims to briefly explain the state-of-the-art power device technology and the reason why the new generation of WGB power devices are getting more and more popularity on the market. It is clear that now Si power switches have reached the technological limit due to the intrinsic material properties. Under the pressure of increasing the efficiency and the power density and lower the cost of the converters,

new materials such as SiC and GaN have gained attention from both academy and industry. While SiC MOSFETs have already become the power switch standard replacing the consolidated Si IGBT, the GaN devices has started their journey in the power electronics recently. Gallium Nitride has not reached the technological maturity, however it shows promising potential for the future. Certainty, this technology is not simple to handle because its insertion in the power converter environment modify lots of fundamental aspects such as EMI compatibility, gate driving, parasitism and many more as shown in Fig. 2.47. After a material properties comparison, GaN power devices have been analysed. In particular, the lateral structure has been described and the main differences (i.e. layer and gate structure) between the main e-mode and d-mode devices have been reported. Then, some additional issues of this new technology has been studied including the reverse conduction behaviour, the current collapse and the breakdown phenomena. Finally, some possible interesting future trends have been identified by the presented literature review. They include the development of vertical devices, the circuit integration in smart switch and the manufacturing of high voltage/current power modules.
The second part of this chapter focuses on the comparison among different semiconductor technologies. The 600/650 device voltage rating class is identified as optimal for the considered application. Firstly, an half-bridge hard-switching loss model has been proposed. Then, a literature review of the main FOM have been detailed and a new FOM suitable for the case study have been proposed [141]. The paragraph ends showing that the optimal semiconductor choice strongly depends by the operating condition of the realized converter. The analysed semiconductor technology performance comparison will be used later in the thesis for the converter power switch selection.

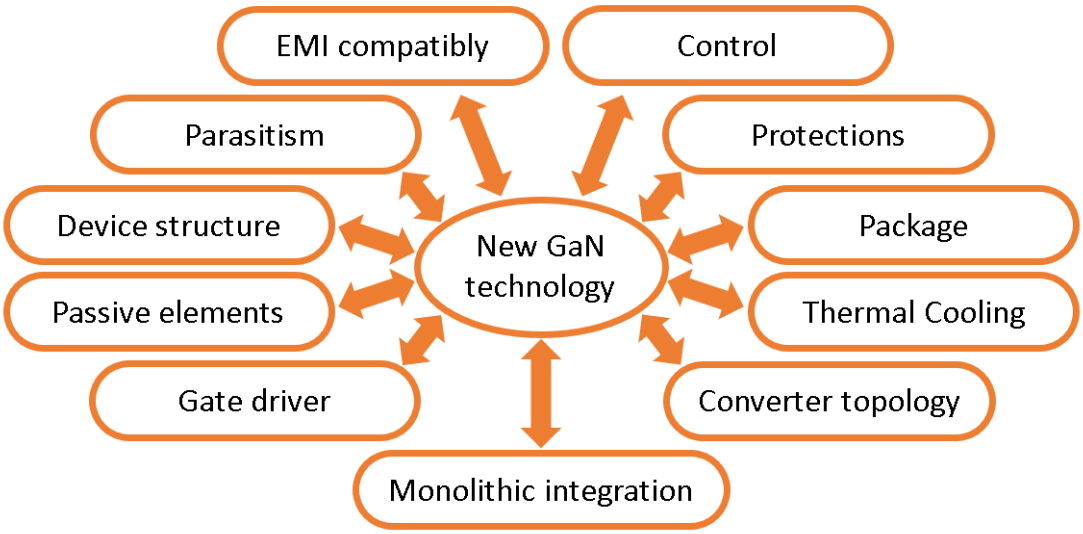


Fig. 2.47 The adoption of GaN devices in power electronic converter modify many fundamental aspects that need to be properly investigated.

Chapter 3

Multilevel Converter Topology

3.1 Multilevel Converter: Current Applications and Future prospectives

The most simple and robust three-phase converter structure is the two-level inverter for both grid connected and motor drive application. This topology has an intrinsic power ratings limitation due to the power switch technology adopted. Indeed, the device voltage rating limits the DC-Link voltage that can be commutated. Currently, it is difficult to connect a single power device directly to the medium voltage range which is between 2.3 kV up to 13.8 kV [153]. To overcome this limits, medium voltage converters used to adopt the devices series connection (i.e. usually the power switch current rating is sufficient, thus parallel connection is not necessary) [154]. This configuration is strongly affected by the devices parameters mismatches. Consequently, it is complicated to ensure equal voltage sharing among each device in both static and dynamic conditions (i.e. it is important to avoid device over-voltage failure). The off-state leakage current mismatch and its device temperature dependence affect the static voltage sharing. The dynamic voltage sharing is mainly influenced by the unequal device switching characteristics (i.e. the turn ON/OFF delay times and gate driving parameters and their temperature dependence)[154]. Some passive elements can be added in parallel to the devices, but they do not assure a satisfactory result [153]. For these reasons, the devices direct series connection is very difficult to handle. In order to satisfy the growing medium voltage market needs, the scientific research proposed new converter architectures that can ensure both dynamic and

static voltage sharing among power devices. On the other hand, these topologies are more complicated than the traditional two-level converter. Therefore, the multilevel structures are a particular converters topology, which enable the usage of indirectly series connected switches (i.e. through the usage of clamping capacitors or diodes). So, the DC-Link converter voltage can be commutated by multiple device of lower voltage ratings (i.e. each switch commutate a portion of the DC-Link voltage) compared to an equal two-level structure [154–156].

On the other hand, in the low voltage application, the device current rating results the maximum converter power rating bottleneck. So, for high power low voltage applications (i.e. automotive traction inverter and ultra-fast battery chargers), the power switches are usually displaced in parallel configuration [157]. It is less critical than series connection, but the devices parameters mismatch can similarly lead to static and dynamic current sharing problems which can bring to a device over-current failure. In particular, the device on resistance ($R_{ds,on}$) and its temperature dependence affect the static current sharing among devices in parallel configuration. On the other hand the gate voltage threshold ($V_{gs,th}$), the device transconductance (g) and their temperature dependences affect the dynamic current sharing. To avoid these issues, a proper gated driver and power commutation loops must be adopted in the converter design. The main parameters that influence the direct series and parallel connection are listed in the following table.

Table 3.1 MAIN CAUSES OF VOLTAGE AND CURRENT UNBALANCES RESPECTIVELY IN SERIES AND PARALLEL CONNECTION

Device Configuration	**Static Unbalance Causes**	**Dynamic Unbalance Causes**
Series Connected	OFF-state leakage current	Device switching characteristics
Parallel Connected	$R_{ds,on}$	$V_{gs,th}$, g

The multilevel structures have been particularly adopted in medium voltage application where the commutated voltage is considerably higher than the maximum commutable voltage of the commercially available devices [154, 155]. This does not represent the only advantage of these structures adoption in this field. As a matter of fact, the multilevel converters synthesize an output leg applied voltage with multiple voltage levels (i.e. more than two voltage levels). As shown in Fig. 3.1, the two-level converter synthesizes an output waveform (i.e. the voltage between the output phase

and the DC-Link mid point) alternating only the positive and the negative voltage rail of the DC-Link. Fig. 3.1 (b) shows a generic three-level inverter output voltage waveform which is realized with an additional voltage value. It is clear that extending this concept to N-level converter, the output voltage shape will resemble more and more to a sinusoidal waveform, thus having a reduced harmonic content[156, 158].

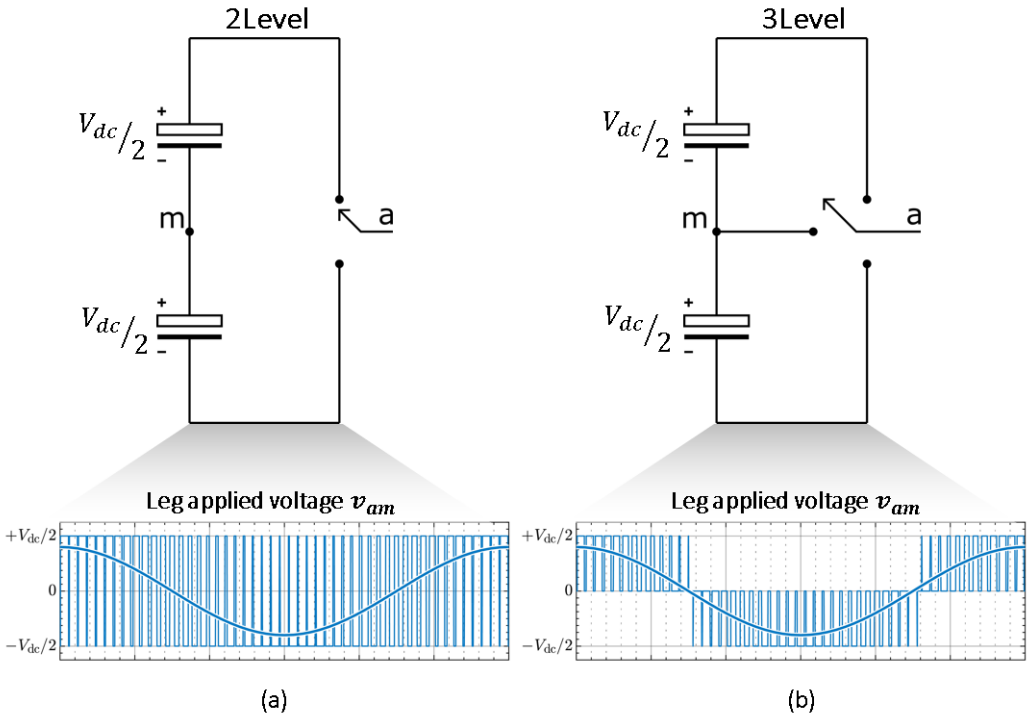


Fig. 3.1 2-Level (a) and 3-Level converter output voltage waveform principle (the first harmonic component is highlighted). The multilevel converter synthesize the leg applied voltage alternating more than two voltage values.

In addition, the multilevel converter enables the usage of lower voltage rating devices with a better figure of merit that can thus switch at an higher frequency. Compared to the standard two-level inverter, the combination of the higher switching frequency and the smaller voltage levels improve the quality and reduce the harmonic content of the output voltage waveform [158, 159]. Moreover, considering the reduced voltage steps commutated, the dv/dt stress is attenuated resulting in a lower stress for the AC load. To sum up, the possibility of high DC-link voltage commutation, the enhanced output voltage waveform and the reduced dv/dt stress have favoured the spread of the multilevel converter over the two-level topology in high voltage applications, even though these converters present a substantially enhanced structural and control complexity [158, 159]. The main adopted and well

established structures for MV applications are the cascaded H-bridge, the neutral point clamped converter and the flying capacitor converter [154–156, 160, 161]. In medium voltage, the main applications are in grid-connected systems and motor drive applications (i.e. electric ships, electrical railways, pumps, compressors, high power fans to name a few) [153, 158, 162].

Nowadays, automotive is a particularly dynamic sector that contribute to push forward the related scientific research as illustrated in the previous chapter. Even if the electric car presents a more efficient energy conversion process, a better acceleration dynamic and a potential lower total emission structure if combined with the renewable energies, it has still some important drawbacks compared to the traditional gasoline alternative [162]. The main challenges of the electric vehicle is to enlarge the autonomy range and to speed up the battery charging process [163, 164]. The car maker response to this need of improvement is a continuous evolution and modification of the power-train, of which the main parts are the battery, the inverter and the electric motor as depicted in Fig. 2.2. Recently, the automotive DC-Link standard is moving from 400V to 800V [162]. The first electric vehicle featuring 800V power-train has been the Porsche Taycan in 2019 [165], this trend is confirmed by the new electric models available on the market [166–168]. One of the main reason of this drastic change can be found in the need of higher converter power rating (i.e. to reduce the charging time) [163]. Indeed, the need of up to 300 kW chargers has been estimated in order to compete with the gasoline vehicle fill up time [164]. The increase of the DC voltage favours the higher converter power ratings featuring a limited phase current amount. A consequent important benefit is the cables size reduction, which translate in the total vehicle weight reduction and in the easier charging cable handling capabilities (i.e. high voltage cable are usually more flexible and less heavy) [162].

Nowadays state-of-the-art automotive traction inverter structure is the two-level inverter employing 1200V Si IGBT or 1200V SiC inverter [157], as shown in 3.2. Since the traditional converter topology has been maintained, there has been a consequent change in the semiconductor technology. Indeed, the power switch voltage rating passed from 650V (i.e. for 400V DC-Link) to 1200V (i.e. for 800V DC-Link).

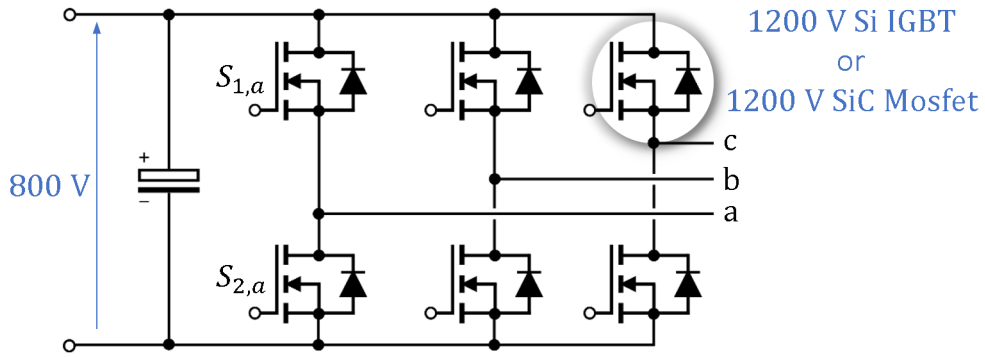


Fig. 3.2 Two-level inverter electric schematic. The voltage rating of the power MOSFET and diodes are specified for 800V of DC-Link voltage.

The 2-level structure is used for its simplicity, robustness and low cost. On the other hand, in a highly competitive and innovate sector such as automotive, power electronic converters are continuously pushed to improve. The main required features are high efficiency, high power density, high switching frequency and high temperature operation. The converter efficiency is one of the most important feature of the converter design due to the fact that it has a direct impact on the maximum car autonomy range and on the cooling system density [162]. The recent adoption of SiC power MOSFET have brought to an higher switching frequency and a converter loss reduction especially at light low due to the MOSFET absence of the threshold voltage compared to the traditional Si IGBT devices (ref to Chapter 2). The switching frequency is another important converter element to enhance the output quality voltage waveform thus reducing the reactive components (i.e. input inductors in the ultra-fast battery chargers), the PWM induced loss in the electric motor [169, 170] and rising the controllability in the load motor with low phase inductance. Exploiting new available technologies (i.e. GaN devices) with non-conventional topologies could be the enabler condition to improve both efficiency and power density of the next generation of traction inverters. The GaN switches are now entering in the semiconductor market promising better performances than the state-of-the-art Si/SiC devices (see Chapter 2). Their breakdown voltage limitation (i.e. mainly due to the lateral structure) combined with the continuous research of the converter efficiency and power density improvement have favoured the research activities on multilevel converter applied to low voltage (LV) applications (i.e. traction inverter and ultra-fast battery chargers) [171, 172]. As a matter of fact, the multilevel structures can bring lots of benefit compared to the traditional 2L inverter as stated before

[169, 173], although they have not penetrated the LV automotive market yet [157]. In addition, they enable the usage of 650V GaN devices in 800V three-level converter architecture. On the other hand, these topologies have some challenges that must carefully explored such as a non standard structure, a complex control and balancing problems [162].
Summarizing, GaN devices approach to this extremely competitive market offering low losses and very high switching frequency. The multilevel structure unlocks the usage of these innovative power switches with a substantially better FOM, in the 800V power-train architecture. The mixture of these two innovative elements have the potentiality to enhance the overall converter efficiency, power density and output voltage waveform quality. The aim of this work is to analyse the advantages of this combination in the design and optimization of the next generation EV inverters. The chapter thus compares the main challenges, advantages and drawbacks for the main multilevel structures in order to give a clear overview and an optimal choice for the traction inverter prototype object of this thesis.

3.2 Multilevel Converter Structure Analysis

The aim of this work is to realize an innovative prototype for the next generation of traction inverter. It is clear that innovative converter structures and technologies are mandatory to improve both system efficiency and power density. GaN devices are now starting to penetrate the semiconductor market, on the other hand their structure limits the devices voltage rating to 650V as stated in Chapter 2. This makes impossible to use these power switches in traditional two-level structures for the new 800 DC-Link voltage power-train standard unless multilevel topologies are considered. Neglecting for a moment the advantages of the GaN device adoption, it is important also to know the multilevel differences compared to the traditional two-level structure. Indeed, there are lots of topologies, each one has its own strengths and weaknesses. This paragraph aims to analyse and find out the best multilevel structure suitable for the considered application. At this point is useful to introduce some project constrains to reduce the optimization degrees:

- *The 800 DC-Link voltage standard* is selected because it represents the future trend in automotive power-train;

- *100 kVA converter power rate* is selected to realize a proof-of-concept prototype;
- *GaN devices* are identified as the most promising technology. Therefore, it is decided to employs these devices for the target prototype to explore its effective advantages over the nowadays state-of-the-art converters;
- *The 650 voltage rating* is selected because it is the most adopted standard of power switches currently available on the market. Lower voltage ratings lead to an excessive multilevel levels and control complexity;
- *Selection of the three-level inverter structure* is the direct consequence of the previous decisions (i.e. device voltage rating and the power-train DC-Link voltage standard).

Precise design requirements will be enunciated in the following converter design chapter. Among the most established multilevel structures, we can suddenly eliminate the cascaded H-bridge (CHB) from the topology selection. Indeed, the CHB structure features the series connection of multiple single phase converters, thus presenting a modular structure. Its output waveform is synthesized by the series arrangements of these modules [174]. The main drawbacks are the elevated power devices number and the need of an isolated voltage source for each module. In medium voltage application, this is overcome by using rectifiers or multi-pulse transformers which are usually bulky components [153]. On the other hand, in the automotive field, the isolated voltage source can be realized directly by the battery packs. However, there is a consequent need of a more complex battery management system with additional measurements to guarantee an equal voltage balancing in the charging/discharging process of the battery [162]. This represents the main reason why the CHB structure has been discarded for this prototype realization. Thus, this paragraph proceed with the analysis of the neutral-point-clamped, active neutral-point-clamped, T-type and flying capacitor multilevel structures. The advantages and drawbacks are highlighted for each topology with particular attention to the automotive traction inverter application.

3.2.1 Neutral Point Clamped Converter

The Neutral Point Clamped (NPC) converter was presented for the first time by the Agaki research group in 1981 [175]. By then, it has become one of the most popular multilevel topology adopted for medium voltage drives. This is mainly due, the low harmonic content is combined with the reduction of the voltage derivatives which are related to an overall system efficiency increase [153]. Its structure consists of four switches and two diodes for each phase connected, as shown in Fig. 3.3.

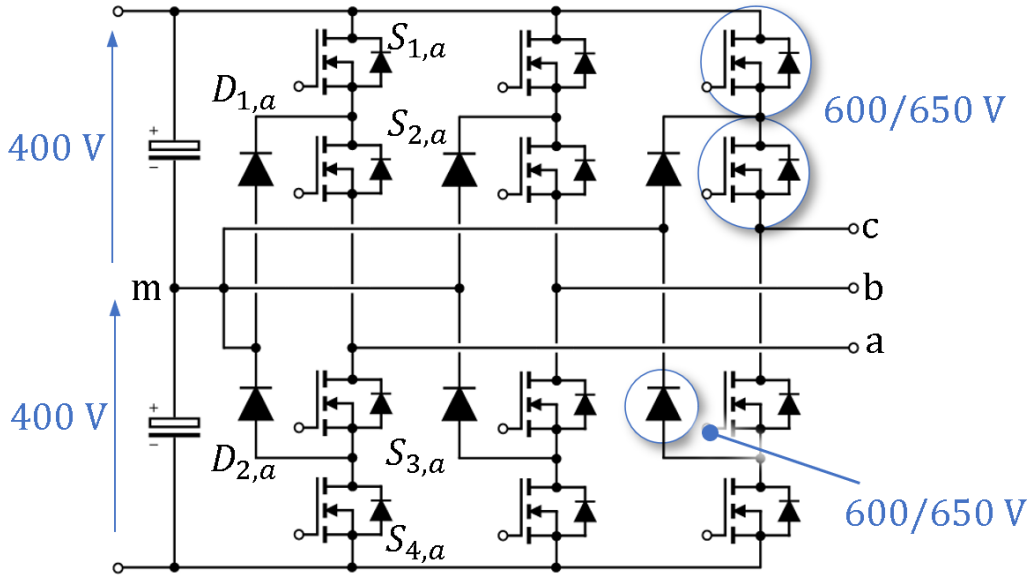


Fig. 3.3 NPC electric schematic. The voltage rating of the power MOSFET and diodes are specified for 800V of DC-Link voltage.

Moreover, the NPC converter features a split DC-Link to enable the diode physical connection to the medium point potential. Indeed, each power device must stand only the half of the DC-Link voltage. In the case of 800 DC-Link voltage, both employed diodes and switches must be rated at least 650V. This fact represents a further advantage because, low voltage rating devices (i.e. 650V compared to 1200V) correspond to a better device FOM. The NPC converter presents some advantages and drawbacks compared to the 2-level converter. As an example, some benefits are the low output voltage harmonic content combined with the reduction of the voltage derivatives on the load. However, the greater number of modulation states must be handled with a more complex modulation strategies. Moreover, this structure has a DC-Link mid point low frequency voltage ripple due to the current flow enabled by the diode connection. This phenomenon translates in a capacitance over-sizing

unless a proper modulation strategy is adopted. This paragraph briefly analyses all these aspects, which will be useful to select the best topology for the considered application.

Modulation States

Before the NPC converter operation principles analysis, it is useful to briefly summarize the two-level inverter (fig. 3.2) gate signal generation method. This is possible by adopting both the carrier based and the space vector modulation methods. The carrier based switching states calculation is performed by the comparison between the three-phase reference waveforms $V_{mx}(x = a,b,c)$ (i.e. three equal waveforms out of phase with each other by 120 degrees) with a single triangular carrier V_{cr}. In this Pulse-Width-Modulation (PWM) scheme, the converter switching frequency is defined by the carrier frequency. Moreover, the output voltage fundamental harmonic component is controlled by modulation index amplitude $m_x(x = a,b,c)$, which is defined as the ratio between the desired output voltage and the DC-Link one (i.e. $m_x = V_{mx}/V_{cr}(x = a,b,c)$). The comparison result defines the switching state for each inverter phase (i.e. when the $V_{mx} > V_{cr}$ the relative upper switch is turned ON and the lower one is turned OFF, a proper dead time must be setted in order to avoid shoot-through events). The resulting leg applied voltage $V_{xm}(x = a,b,c)$ (i.e. the voltage defined between the output switch node phase and the DC-Link mid point m) features only two levels as shown in Fig. 3.5 (b). Usually, the third harmonic modulation technique is adopted to increase the output waveform voltage avoiding the over-modulation (i.e. when the modulation index is greater than one). Indeed, adding a third harmonic to the three-phase reference waveform system allows to increase its fundamental output voltage component, on the other hand the overall waveform peak results still lower than the triangular carrier. The maximum fundamental amplitude increment of $2/\sqrt{3}$ (i.e. maximum linear operation range) is obtainable with the triangular third harmonic injection. It is calculated as follow:

$$vo = \frac{max(V_{ma},V_{mb},V_{mc}) + min(V_{ma},V_{mb},V_{mc})}{2} \tag{3.1}$$

Fig. 3.4 shows the schematic principle of the reference waveform calculation adding the triangular third harmonic injection.

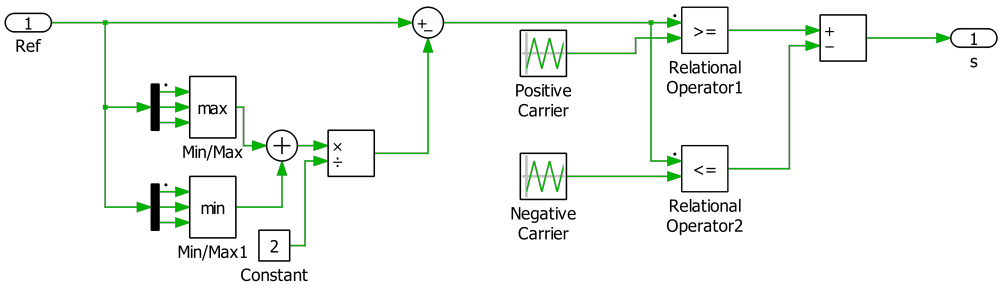


Fig. 3.4 Reference waveform modification by adding triangular third harmonic in carrier based modulation to obtain the same space vector modulation pattern (i.e. so the maximum linear operation range).

Clearly, the resulting reference waveform will not present a sinusoidal shape as shown in Fig. 3.5 (a). The space vector modulation (SVM) is usually preferred when digital control of the voltage source inverter is implemented. The gate signal generated implementing the triangular common mode injection is the same generated by the space vector modulation technique.

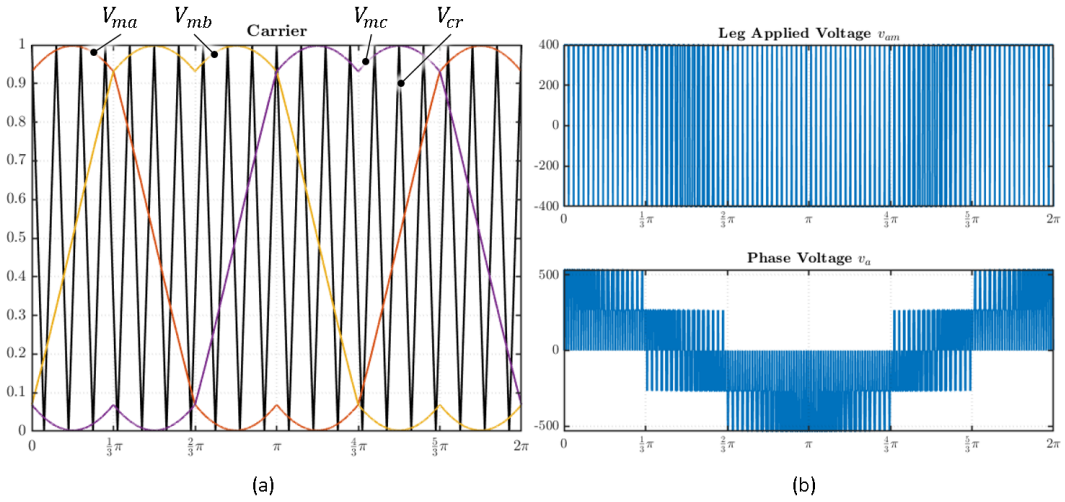


Fig. 3.5 The carrier based switching states calculation scheme for a two-level voltage source inverter: (a) the triangular carrier V_{cr} comparison with the reference signals $V_{mx}(x = a,b,c)$ modified with the triangular third harmonic technique, (b) the resulting two level leg applied voltage V_{am} and phase voltage V_a.

In the NPC converter, the switching function $S_x(x = a,b,c)$ can define the operating status of the NPC converter for each phase. Indeed, as illustrated in Table 3.2, if S_x is equal to +1/-1, the output phase is connected respectively to the positive and negative rails of the DC-Link. On the other hand, if the switching function is equal

to zero, the switch node is connected to the DC-Link mid-point through diodes (i.e. the current path is decided by the load condition).

Table 3.2 SWITCHING STATE OF THE THREE-LEVEL NPC INVERTER

Device			
$S_{1,x}$	ON	OFF	OFF
$S_{2,x}$	ON	ON	OFF
$S_{3,x}$	OFF	ON	ON
$S_{4,x}$	OFF	OFF	ON
S_x	+1	0	-1
V_x	$+V_{dc}/2$	0	$-V_{dc}/2$

V_{xm}: output leg applied voltage
S_x: switching function
$x = a, b, c$

The NPC gate signals can be generated with both carrier based and space vector method with few differences compared to the two-level inverter. In the carrier based method, the reference waveform $V_{mx}, (x = a, b, c)$ (i.e. duty cycles) are implemented with the triangular third harmonic injection as in the two-level case, as shown in Fig. 3.6 (a). However, to create the three level switching function, two triangular carriers (V_{cr1}, V_{cr2}) vertically shifted are usually adopted (i.e. Fig. 3.6 (a)). Thus, S_x is obtained through the comparison between the duty cycles and the modulation carriers. It is then equal to 1 when the duty cycle is greater than the upper carrier and to -1 when the duty is smaller than the lower carrier, otherwise it gets the zero value. The resulting leg applied output voltage V_{xm} has three levels similarly to the switching function, as shown in Fig. 3.6. As it can be noticed, this converter can utilize the mid point of the DC-Link to synthesize the phase voltage, differently from the two level inverter. This significantly reduces the harmonic content and the dV/dt stress generated by the output waveform.

The space vector hexagon diagram is useful to represent the switching states of the converter. Taking into account a two-level inverter, its switching states can assume two values for each phase, hence eight space vectors can be synthesizes. On the other hand, the three-level three-phase NPC topology is able realize 27 switching states (each phase can synthesize three voltage levels as shown in Table. 3.2). However, the possible space vectors are only 19 due to redundant states (i.e. vector that can be synthesized by different switching states). These converter switching

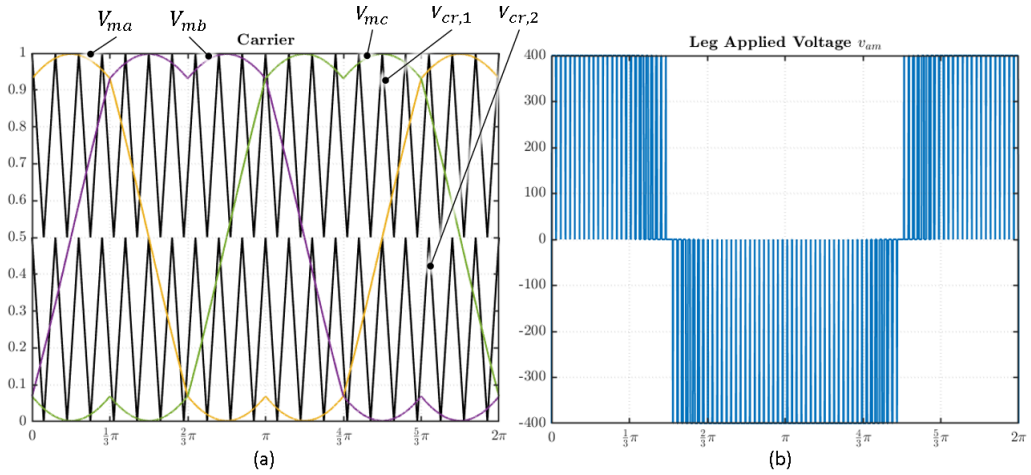


Fig. 3.6 The carrier based switching states calculation scheme for a three-level NPC voltage source inverter: (a) the upper and lower triangular carrier comparison with the reference signals $V_{mx}(x = a,b,c)$ modified with the triangular third harmonic technique, (b) the resulting two level leg applied voltage V_{am}.

states can be represented in a space vector digram, that is made up of different hexagon for the three-level converter as illustrated in Fig. 3.7. These space vector can be divided in large (V_L), medium (V_M), small (V_S) and zero (V_0) types depending on their magnitude, as shown in Fig. 3.7 (i.e. the switching state of each phase is specified in bracket). It can be pointed out that each small vector can be synthesized by two switching state configurations. In a similar way, the zero vector has three redundancy options. In a two-level converter, the space vector diagram is represented by a singe hexagon with six active vector and two redundant zero vectors (i.e. they can be synthesized turning ON all the upper or lower switches).

Low Frequency Neutral Point Voltage Ripple

Similar to the other multilevel topologies, the main NPC disadvantages lie on the higher control complexity and higher number of device count. Moreover, in normal converter operation (i.e. applying traditional space vector modulation), the neutral current flowing in the DC-Link mid point generates a low frequency (LF) oscillation of the DC-Link neutral point [176]. This LF neutral point oscillates at three time of the output fundamental frequency and its magnitude depends on the modulation index and the power factor angle of the working point [177]. As a matter of fact, Fig. 3.8 shows these dependences with the simulation result of the charge ripple

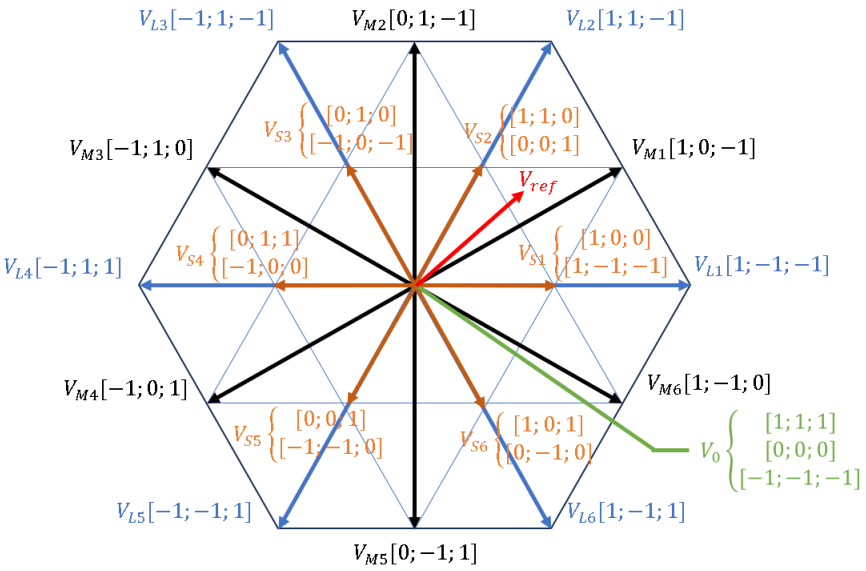


Fig. 3.7 Representation of the space vector hexagon for a three-level NPC converter. The adopted colors are: blue for the large virtual vectors V_{ZL}; black for the medium virtual vector V_{ZM}; orange for the virtual small vector V_{ZS} and green for the zero virtual vector V_{Z0}. The switching state of each phase is specified in bracket.

requirements (i.e. directly related to the required DC-Link capacitance) for a 100kVA NPC converter (800V inverter DC-bus voltage, 145A output peak phase current and 50 Hz output fundamental frequency).

Due to this issue, the DC-Link capacitors and the power switches have to stand an higher voltage than $V_{dc}/2$. This ripple will affect also the output line-to-line voltages [178]. For these reasons the LF oscillation has represented an interesting scientific research field for many years. Some mid-point voltage deviations can occur due to unbalanced load operations or to inconsistency related to the DC-Link capacitors and to switching characteristics of devices [153]. This causes will be neglected in this dissertation.

In order to mitigate the LF neutral point oscillation, an easy solution is represented by the increase the DC-Link capacitance value. It is clear that to maintain high converter power density a proper control of the neutral point current is mandatory. Regarding this problem, many modulation techniques have been proposed in literature relying on both Space Vectors (SVPWM) and carrier based modulation [179–181].

Looking at Fig. 3.7, it can be pointed out that only the zero and the large vector does not generate i_m (i.e. no connection of the phase to the DC-Link mid point). The small vector effect on the mid point current can be eliminated exploiting their

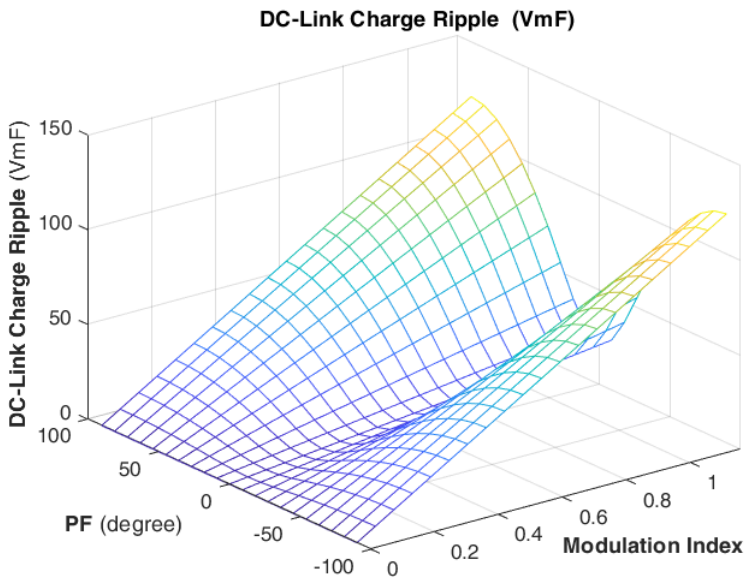


Fig. 3.8 Simulation of the charge ripple requirements for a 100kVA NPC converter (800V inverter DC-bus voltage, 145A output peak phase current and 50 Hz output fundamental frequency). The charge ripple requirements is simulated for a SVM control. Power factor angle (PF) and modulation index dependences are outlined.

redundant states as implemented in three-nearest-vector (NTV) modulation [182–184]. However, the LF oscillation persists at high modulation indices. Indeed, the medium vector does not have redundant switching states and inject a mid current that depends on the load. Its effect is not mitigated by the NTV, but it is properly handled by the nearest three virtual space vector PWM modulation as explained in the following subsections [176, 185–187].

Three-nearest-vector (NTV) Modulation

Fig. 3.7 shows clearly that each small vector can be synthesized by two different inverter configurations with the same output voltage results, but with different mid point current direction. This redundancy can be exploited by the modulation technique (i.e. an example is the three-nearest-vector (NTV)) to achieve zero average mid point current and thus eliminating the LF mid point voltage ripple [183]. Fig. 3.10 shows the normalized neutral point voltage ripple for NTV control and its dependences by the modulation index and the power factor. It can be pointed out that the NTV control can eliminate the LF mid point oscillation for low modulation index.

However, for higher modulation index (i.e. >0.5), the influence of small vectors is reduced compared to the one of the medium vectors and thus this neutral point voltage control is limited leading to the same results of the space vector modulation.

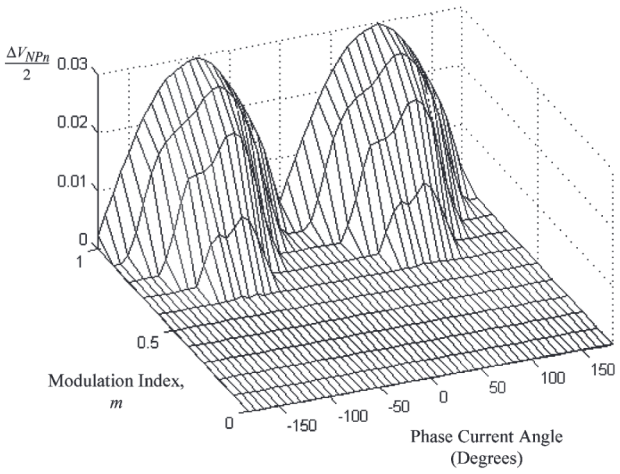


Fig. 3.9 Normalized neutral point voltage ripple for NTV control. Power factor angle (PF) and modulation index dependences are outlined [183].

Nearest Three Virtual Space Vector (NTVV) PWM Modulation

The Nearest Three Virtual Space Vector (NTVV) is a modulation that eliminates the low frequency DC-Link mid-point oscillation in each operating condition [185, 187]. The aim of this technique is to realize a zero average mid-point current in the switching period. If we analyse the space vector hexagon of Fig. 3.7, this can be done for low modulation indexes exploiting the small vector redundancies. Since at high modulation indexes there is an uncontrolled mid-point current generated by the medium vectors, the NTVV modulation defines new virtual vectors that will synthesize the reference vector (i.e. it is not defined by a sequence of the three nearest standard vectors as in the SVM) [187]. While the large virtual vectors V_{ZL} has the same definition of the large vectors since they do not produce mid point variations, the virtual small vector V_{ZS} is obtained by equally combining the two redundant small vectors (i.e. they generate the same mid-point current with an opposite sign). The zero virtual vector V_{Z0} is defined by the switching state [000]. In the end, the medium virtual vector V_{ZM} is generated by three vectors equally weighted as shown in Fig. 3.10 for the first sextant of the space vector hexagon. To sum up, each virtual

vector is synthesized to achieve an average zero mid point current as outlined (i.e. red equations) in Fig. 3.10.

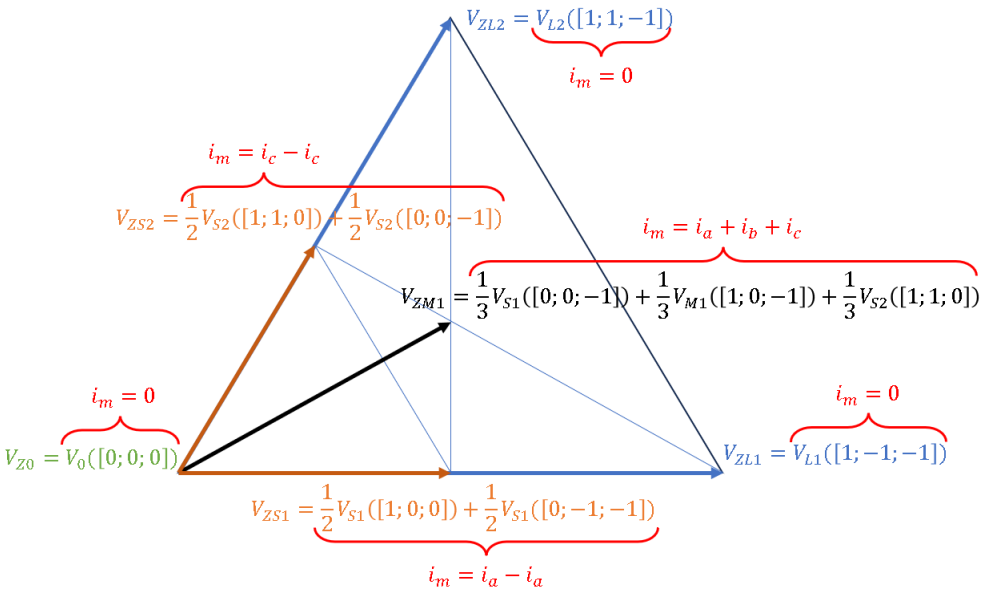


Fig. 3.10 Virtual space vector calculation example for the first sector of the space vector hexagon. The adopted colors are: blue for the large virtual vectors V_{ZL}; black for the medium virtual vector V_{ZM}; orange for the virtual small vector V_{ZS} and green for the zero virtual vector V_{Z0}.

The carrier based modulation equivalent to NTVV space vector technique is shown in [185, 176]. Its main advantage is the simpler algorithm implementation and the consequent relaxed micro-controller requirements. In this method, each reference signal is divided in two separate waveforms: $V_{ma,p}$ compared with the upper carrier $V_{cr,1}$ and $V_{ma,n}$ compared with the lower carrier $V_{cr,2}$, as shown in Fig. 3.12. To ensure the average zero mid-point current, a different common mode is added to the positive and negative reference waveforms as illustrated in the following formulas:

$$V_{mx,p} = \frac{V_{mx} - min(V_{ma}, V_{mb}, V_{mc})}{2} \quad for\ x = a,b,c \tag{3.2}$$

$$V_{mx,n} = \frac{V_{mx} - max(V_{ma}, V_{mb}, V_{mc})}{2} \quad for\ x = a,b,c \tag{3.3}$$

Fig. 3.11 shows the $V_{mx,p}$ and $V_{mx,n}$ reference signals generation just explained. Moreover, Fig. 3.12 (a) shows the NTVV modified reference waveforms compared

with the upper and lower carriers and Fig. 3.12 (b) illustrate the resulting leg applied voltage.

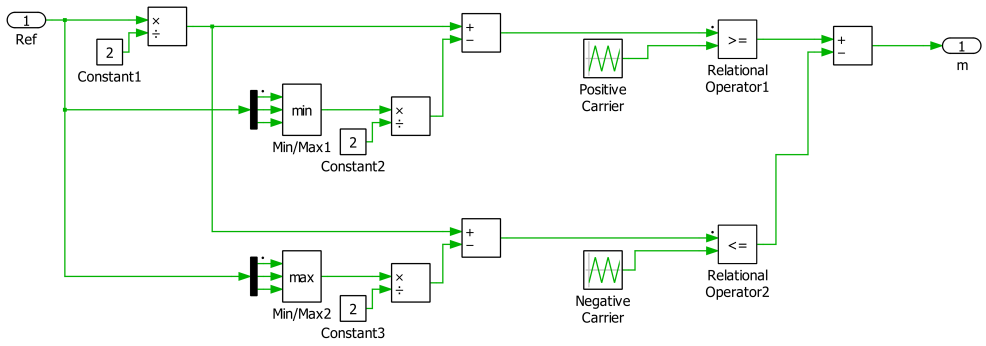


Fig. 3.11 Scheme of the $V_{mx,p}$ and $V_{mx,n}$ reference signal generation starting from V_{mx}, according to NTVV carrier based modulation technique (i.e. x=a,b,c).

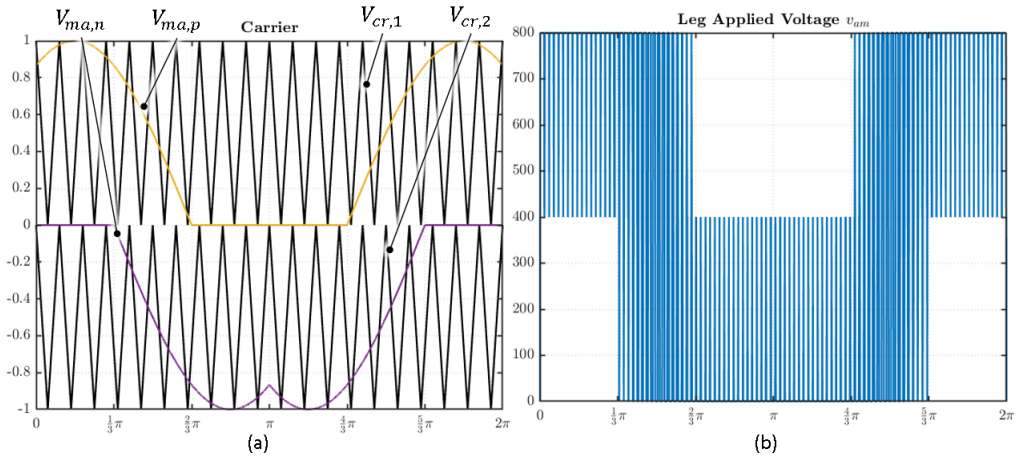


Fig. 3.12 The carrier based switching states calculation scheme for a three-level NPC voltage source inverter adopting the NTVV modulation: (a) the upper and lower triangular carrier comparison with the reference signals $V_{ma,p}$ and $V_{ma,n}$ modified with the triangular third harmonic technique (the other phases are not shown for the image clearness), (b) the resulting two level leg applied voltage V_{am}.

To sum up, the NTVV is able to minimize for any operating condition the LF DC-Link mid-point voltage oscillation generated by the the traditional modulation techniques. This allows to reduce the switch over-voltage stress and relax the DC-Link capacitance constrain featuring an increased equivalent switching frequency. As a matter of fact, Fig. 3.13 shows a PLECS simulation of the DC-Link mid point voltage for a three-level NPC inverter. Considering the same converter parameter and the same operating condition, it is clear the low frequency voltage minimization effect of the NTVV (green waveform) compared the traditional SVM technique (red

waveform). Another similar example is the charge ripple requirements. Its power factor and modulation index dependences for the NTVV modulation are shown for a 100kVA NPC converter (800V inverter DC-bus voltage, 145A output peak phase current and 50 Hz output fundamental frequency) in Fig. 3.14. If it is compared to the SVM requirement reported in Fig. 3.8 (i.e. the simulation feature the same converter parameters), it is clear that DC-Link capacitance requirement is strongly minimized. The drawback of this modulation technique is the rising (i.e. one third) of the equivalent switching frequency compared to the standard SVM [185, 187].

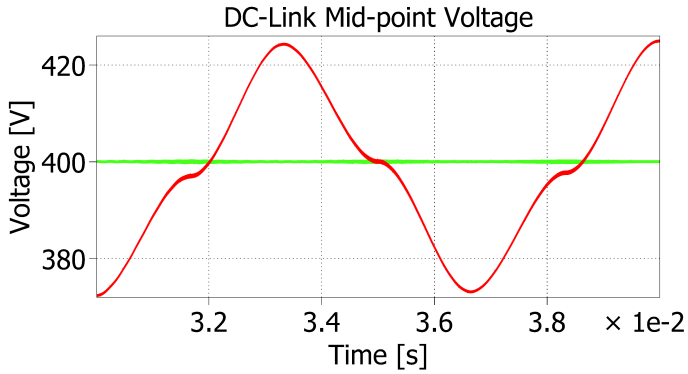


Fig. 3.13 PLECS simulation of the DC-Link mid-point voltage low frequency oscillation in a three-level NPC inverter. It is outlined the NTVV modulation effect (green waveform) compared to the standard SVM technique (red waveform) for the same converter parameters and operating conditions.

Commutation Loop

One of the main challenges of using GaN devices is to optimize the gate and power loop inductances to avoid destructive overshoot due to the fast voltage and current transitions. The NPC converter has a commutation loop which depends on the current direction as it can be seen in Fig. 3.15. Indeed, the switching transition involves two transistors or one transistor and the respective diode. On the other hand, the physical loop can include two or four devices. In the last case, the power loop inductance could determinate a disruptive over-voltage or a consequent limitation in the transition slope (i.e. rising the switching losses). With the aim to not limit the GaN device performances, the three-level NPC has been kept out from the topology selection for this case study.

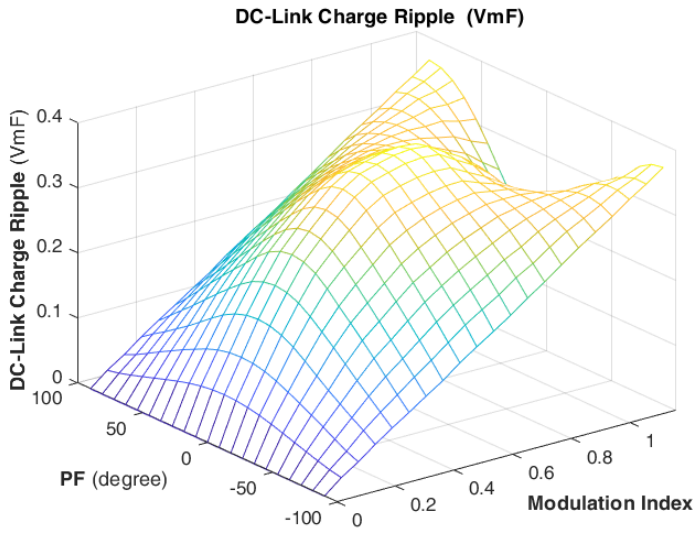


Fig. 3.14 Simulation of the charge ripple requirements for a 100kVA NPC converter (800V inverter DC-bus voltage, 145A output peak phase current and 50 Hz output fundamental frequency). The charge ripple requirements is simulated for a VSVM control. Power factor angle (PF) and modulation index dependences are outlined.

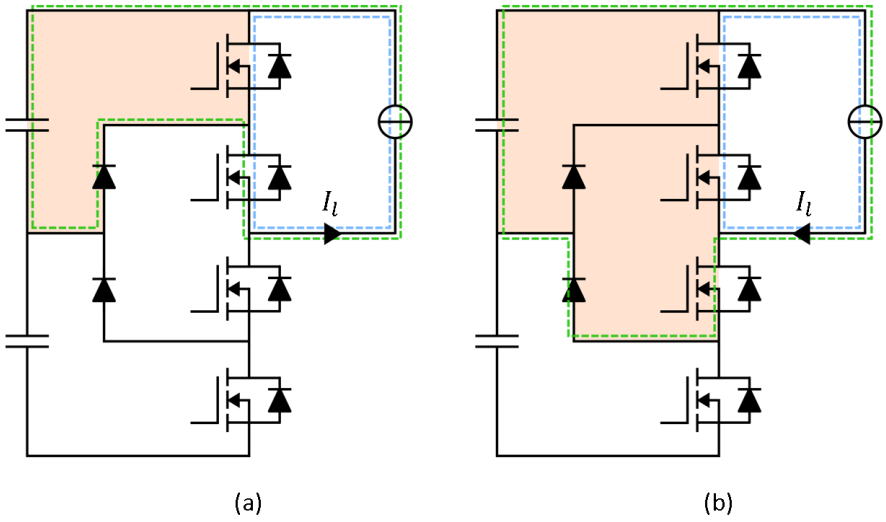


Fig. 3.15 Representation of the three-level NPC inverter commutation loops (orange), which depend by the load current direction and can involve two (i.e. case (a)) or four devices (i.e. case (b)).

3.2.2 Active Neutral Point Clamped Converter

The three-level active neutral point clamped converter (ANPC) is an extension of the 3L NPC converter debated in the previous paragraph. Indeed, their electrical

schemes are similar, as shown in Fig. 3.16. The main difference is the replacement of the clamping diodes with active switches, which translates in the introduction of alternative switching states [188]. For a 800 DC-Link voltage all the employed devices must be 650 volts rated. The ANPC was firstly introduced to solve the unequal loss distribution among the NPC devices [189]. As a matter of fact, the ANPC allow to share evenly the losses among devices and thus lower current rated devices or higher switching frequency can be employed [190]. However, there are some drawbacks such the increased component count of six unit (both power devices and gate drivers) and the enhanced control complexity since six new gate signal must be generated. To sum up, the advantages are not sufficient considering the cost and system complexity increment. So the ANPC will not be considered in the proposed prototype realization.

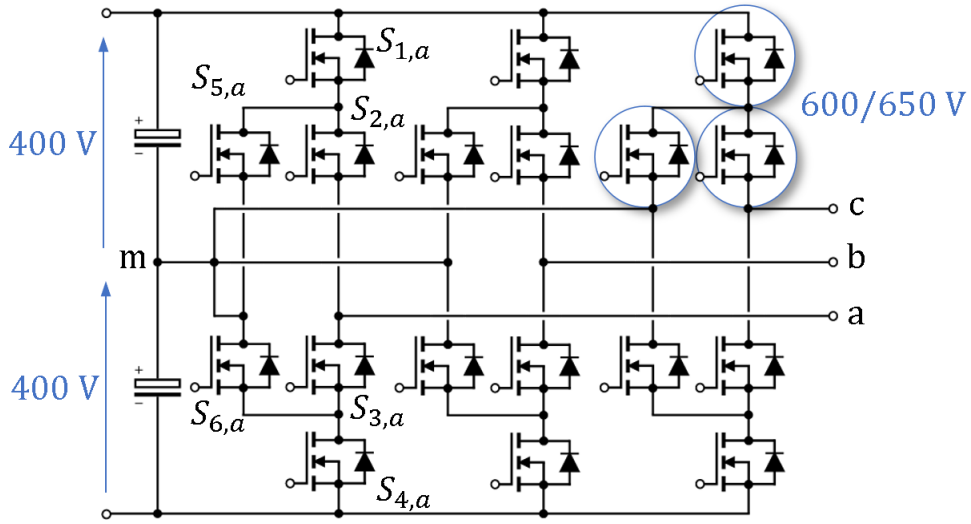


Fig. 3.16 ANPC electric schematic. The voltage rating of the power MOSFET and diodes are specified for 800V of DC-Link voltage.

3.2.3 T-type Converter

The T-type converter is an extension of the traditional 2-level voltage source inverter (2L VSI). The main schematic difference consists in the bidirectional switch (i.e. realized by the anti-series connection of two power devices) that connects the leg switch node to the DC-Link mid point.

On the other hand, the overall device count is increased and the commutation loop includes three devices with a consequent inductance/over-voltage increment. In addition, this topology employs power switch with different voltage ratings. Indeed, the upper and lower switch are rated 1200V to block the entire DC-Link voltage (i.e. 800V), while the mid point switches are rated 650V since they must commutate only half of the DC-Link voltage. Also this structure has been excluded from the selection since the project constrains foresee a full-GaN converter (i.e. commercially available GaN devices are limited to 650V rating due to their lateral structure).

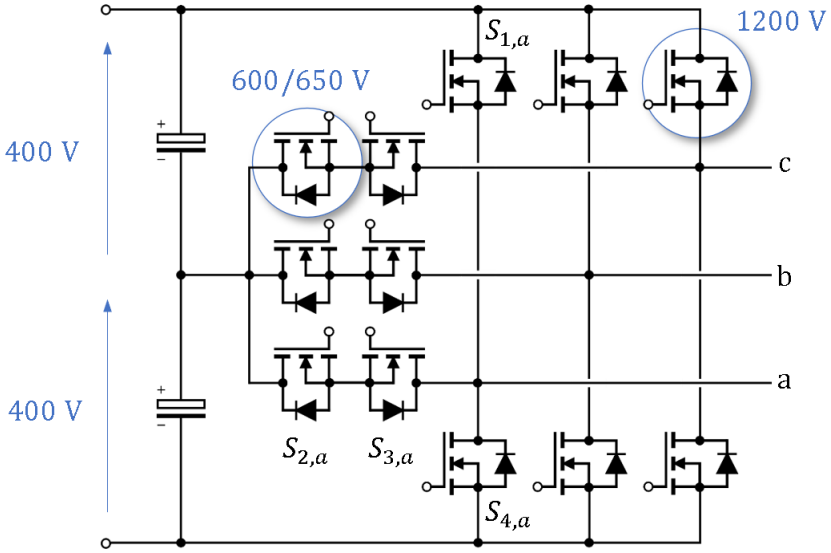


Fig. 3.17 T-type electric schematic. The voltage rating of the power MOSFETs are specified for 800V of DC-Link voltage.

3.2.4 Flying Capacitor Converter

The three-phase, three-level Fling Capacitor (FC) converter electric scheme is shown in Fig. 3.18. It features twelve power switches (i.e. four for each phase) rated 650 V and three flying capacitors rated 400V considering an 800V DC-Link. When the FCs are balanced, the switches have to commutate only the DC-Link half. In contrast to the previous structures, the DC-Link does not present a mid-point connection (i.e. there are no low frequency oscillation related to the mid-point current path). Moreover, the flying capacitors potential is not defined statically to the DC-Link as the name suggest. This structure presents the same advantages of the other multilevel topologies (i.e. low-harmonic three-level output voltage waveform,lower voltage

derivatives and so on). The main drawbacks lay in the complicated control due to the FC balances and the converter start-up and shut-down procedures as will be explained in the next subsections.

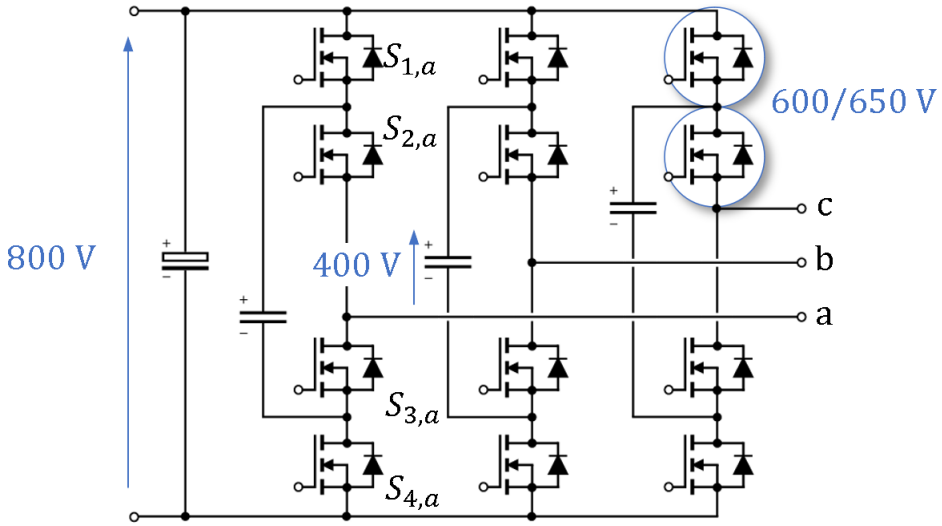


Fig. 3.18 Flying capacitor electric schematic. The voltage rating of the power MOSFETs are specified for 800V of DC-Link voltage.

Modulation states

In the FCC structure, the power devices are controlled as independent bridge-legs. Fig. 3.19 shows a single three-level flying capacitor converter with an alternative electric scheme which emphasize the flying capacitors modularity cell (i.e. the converter level number increase linearly with the cell number). Indeed, the cells are very similar to each other and remind a two-level half-bridge cell (i.e. the power commutation loop involve always two devices) even if the level number rise. As a consequence, all the considerations assumed for the device FOM comparison in the previous chapter can be applied for this converter.

The gate signal generation method is similar to the two-level inverter. The reference waveforms are generated equally through the space vector or through the carrier based method (i.e. adding the triangular common mode seen before). On the other hand, each converter cell has its relative triangular carrier. They are then phase shifted according to the cell number. Considering a three-level converter, there are two triangular carriers which are phase shifted by 180^o as shown in Fig. 3.20

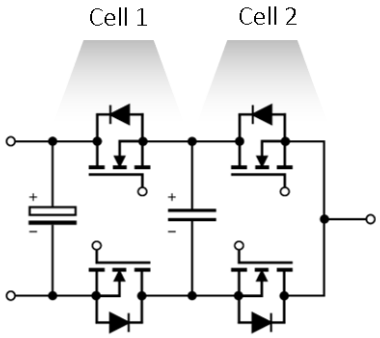


Fig. 3.19 Single phase flying capacitor electric schematic alternative representation.

(a). This phase shift pulse width modulation (PSPWM) operation ensures a simple implementation, a natural flying capacitor voltage balancing and a symmetrical loss distribution among the devices [171]. Fig. 3.20 (b) shows the flying capacitor converter synthesized output leg applied voltage. It has a three-level waveform similar to the other multilevel converters, with the difference that the effective output frequency is two times the switching frequency (i.e. considering the three-level case) due to phase-shift modulation.

The PSPWM guarantees also that the DC-Link and the flying capacitor can never be short-circuited. Tab. 3.3 sums up the feasible switching states ($S_x(x = a,b,c,)$) for the three-level flying capacitor converter. Similar to the NPC convert S_x can be equal to ± 1 or 0.

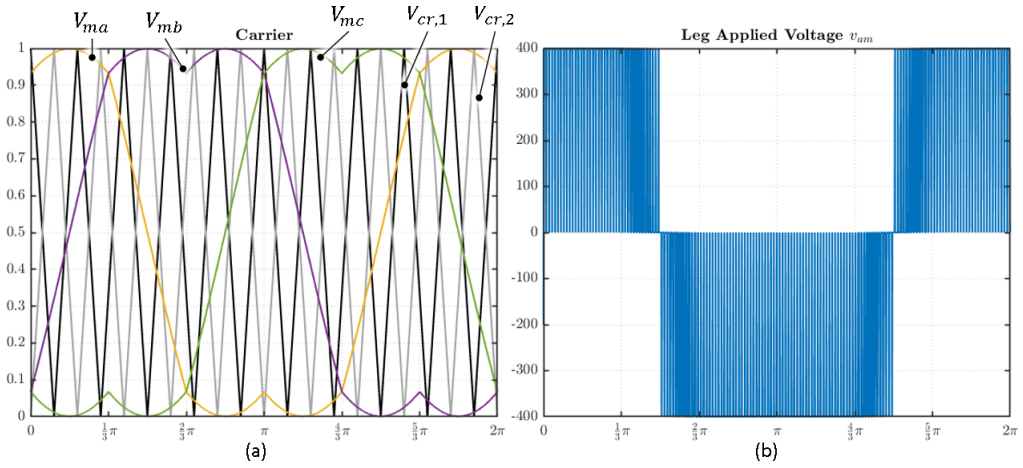


Fig. 3.20 The carrier based switching states calculation scheme for a three-level FCC voltage source inverter: (a) the two phase shifted triangular carrier comparison with the reference signals $V_{mx}(x = a,b,c)$ modified with the triangular third harmonic technique, (b) the resulting two level leg applied voltage V_{am}.

Table 3.3 SWITCHING STATE OF THE THREE-LEVEL FCC INVERTER

Device				
$S_{1,x}$	ON	OFF	ON	OFF
$S_{2,x}$	ON	ON	OFF	OFF
$S_{3,x}$	OFF	OFF	ON	ON
$S_{4,x}$	OFF	ON	OFF	ON
S_x	+1	0	0	-1
V_x	$+V_{dc}/2$	0	0	$-V_{dc}/2$

V_{xm}: output leg applied voltage
S_x: switching function
$x = a, b, c$

The frequency doubling effect is evident in the generated output phase voltage and in its flux ripple. This is shown in Fig. 3.21 where the main harmonic content is at the double rate of the switching frequency (i.e. $f_{sw} = 100kHz$ for this simulation). On the other hand, this effect is not present in the DC-Link and flying capacitor currents and in their charge ripple as shown in Fig. 3.22 and Fig. 3.23. In this last figure it is visible that the PSPWM ensure the FC balancing due to the fact that the mean current flowing through the capacitor is zero.

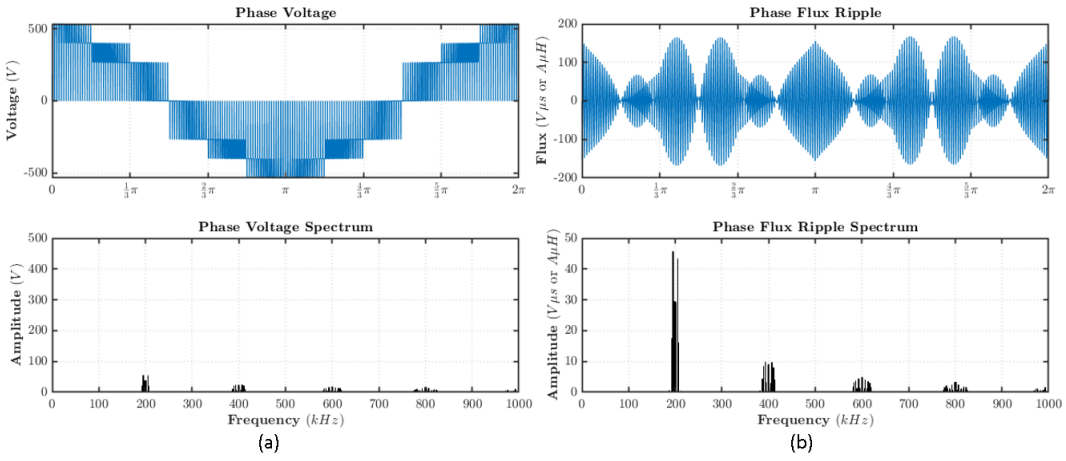


Fig. 3.21 (a) Output phase voltage (b) Phase flux ripple. These waveforms have been simulated in Matalab for a three-level flying capacitor inverter featuring 800V DC-bus voltage, 145A output peak phase current, 100 kHz switching frequency and 1 kHz output fundamental frequency).

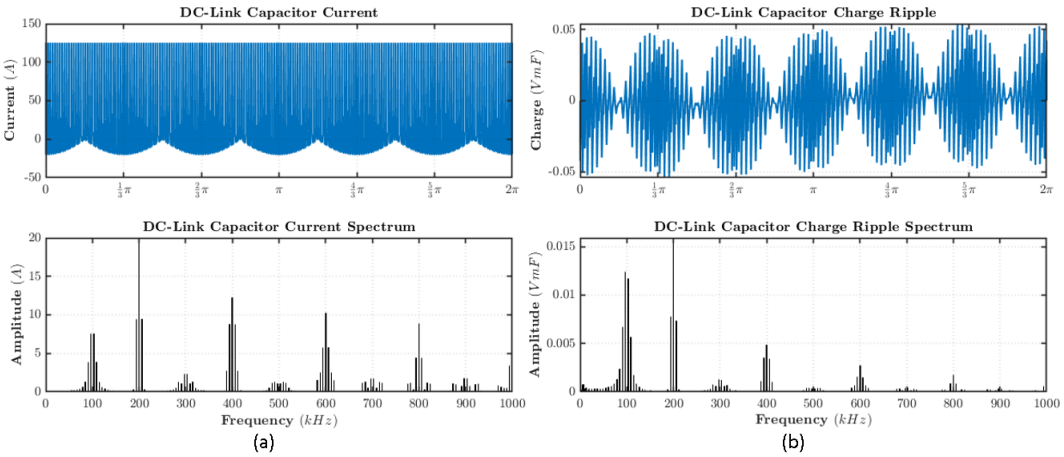


Fig. 3.22 (a)DC-Link capacitor current (b) DC-Link capacitor charge ripple. These waveforms have been simulated in Matalab for a three-level flying capacitor inverter featuring 800V DC-bus voltage, 145A output peak phase current, 100 kHz switching frequency and 1 kHz output fundamental frequency).

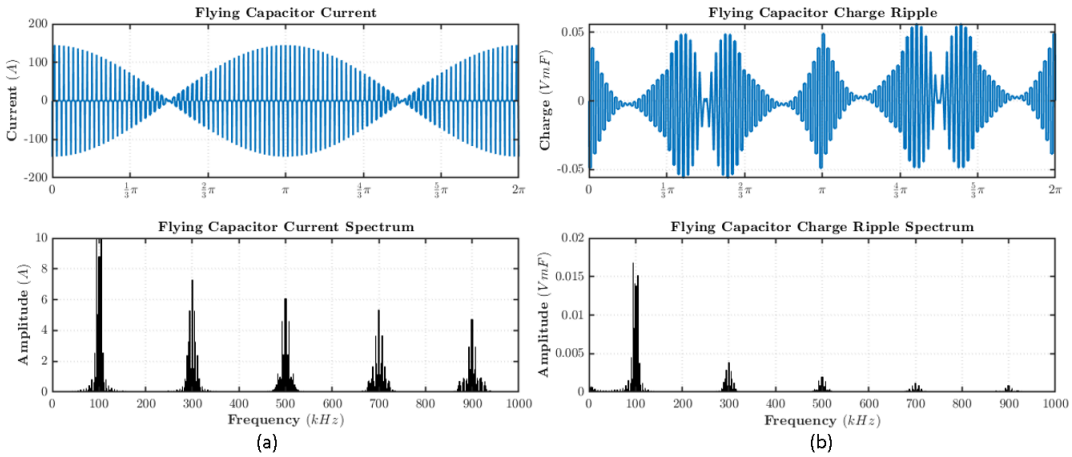


Fig. 3.23 (a)Flying capacitor current (b) Flying capacitor charge ripple. These waveforms have been simulated in Matalab for a three-level flying capacitor inverter featuring 800V DC-bus voltage, 145A output peak phase current, 100 kHz switching frequency and 1 kHz output fundamental frequency).

Start-up/Shut-down

Since it must be assured that the flying capacitor must be balanced at the DC-Link half voltage, the converter start-up and shut-down can be considered as critical operating modes. An easy procedure is to generate a voltage ramp (i.e. for both situation), in this way the PSPWM self-balancing properties is exploited and no additional circuit is needed. In an automotive application this is not feasible, so

two alternative procedures are shown in Fig. 3.24 and in Fig. 3.25. The start-up procedure has the following steps:

- *Step 1*: the pre-charge circuit is activated and the high-side and low-side switches are commanded ON. Consequently, both the DC-Link and the flying capacitor are charged;
- *Step 2*: the high-side and low-side devices are turned OFF once the FC voltage reach its nominal value. The DC-Link continues to charge;
- *Step 3*: the pre-charge circuit is disabled and the PWM is enabled once the DC-Link achieve its nominal value.

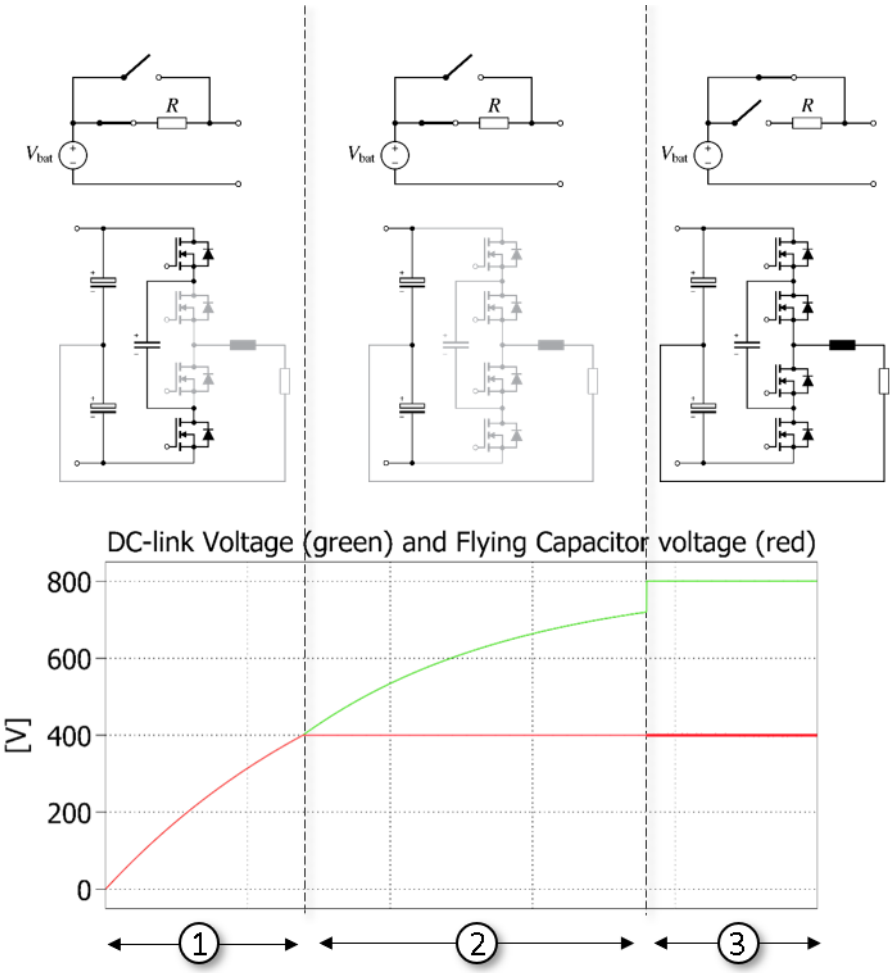


Fig. 3.24 Possible start-up procedure with external pre-charge circuit. For clearness explanation it is shown a single phase inverter.

The shut-down procedure has the following steps:

- *Step 1*: the converter operates normally until the shut-off signal;
- *Step 2*: the discharge circuit is then activated. The DC-Link begins to discharge until the FC nominal voltage value is achieved;
- *Step 3*: when the DC-Link voltage falls below the FC one, the high-side and low-side power switches body diodes are forward biased and directly connect the two capacitors, which start to discharge together.

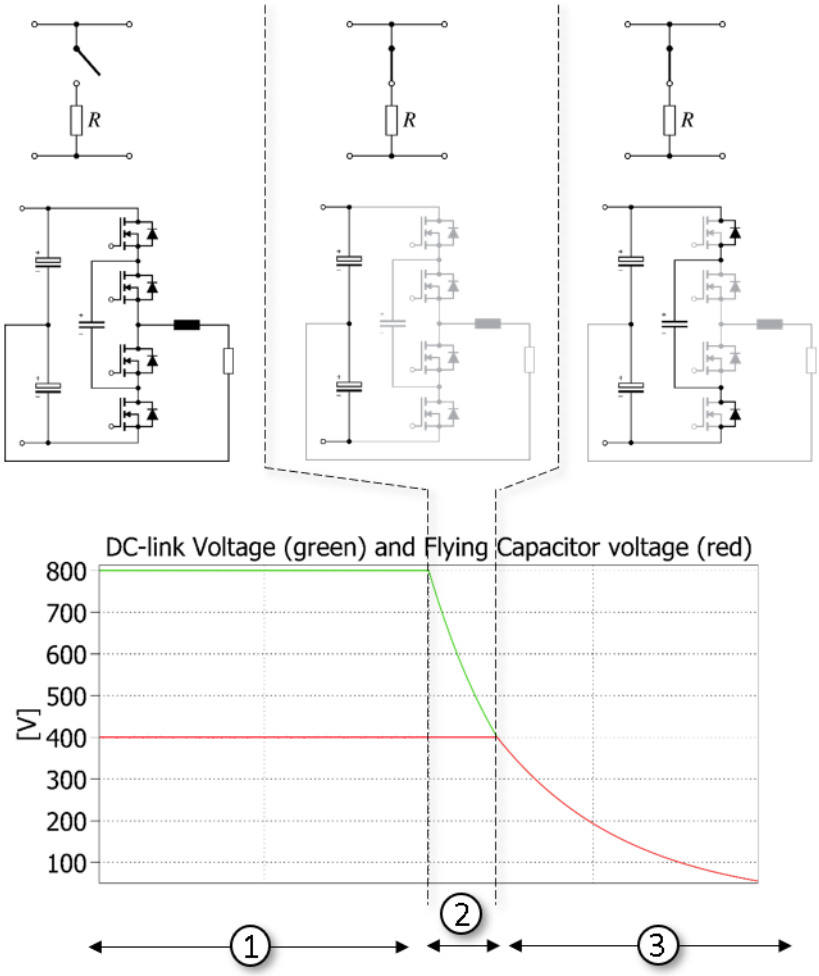


Fig. 3.25 Possible shut-down procedure with external pre-charge circuit. For clearness explanation it is shown a single phase inverter.

3.3 Conclusion

Multilevel structures have been firstly proposed to commutate high voltage DC-Link voltages without connecting power switches with limited voltage range directly in series. Indeed, the main application until today lays in the medium voltage sector. These topologies have lots of advantages compared to state-of-the-art 2-level converters (i.e. low harmonic content of the output voltage waveform, usage of lower voltage devices with better FOM...). These structures combined with GaN devices features are now becoming competitive also in the low voltage sector promising better efficiencies and power densities. The chapter continues presenting briefly the main required characteristics of the converter prototype which is the main focus of this thesis. With these assumptions, the topologies analysis are then restricted to 800 DC-Link voltage, three-level structure employing 650V rated GaN devices. Then, the main multilevel topologies considered for the application are presented outlying the main advantages and drawbacks. Summarizing:

- *Neutral Point Clamped (NPC) converter* is one of the most popular, simple and robust structure. With standard modulation techniques, a low frequency oscillation originates in the DC-Link mid-point that can cause a capacitance over-sizing and a semiconductor over-voltage failure. This problem is solved by the NTVV modulation at the cost of an higher equivalent switching frequency. This structure has been discarded by the selection due to the current load dependent power commutation loop. Indeed it can include up to four devices. This parasitic inductance increment can bring to a device critical over-voltage or to a GaN performance de-rating.

- *Active Neutral Point Clamped (ANPC) converter* has a similar structure to the NCP. Indeed, the clamping diodes are replaced with active power power switches. This translates into a symmetrical loss distribution among devices in inverter operation mode (i.e. contrary to NPC inverter) and a commutation loop that does not depend on the load condition. The mid-point oscillation can be handled similar to NPC converter. Also this structure has been withdrawn from the topologies selection considering the cost and complexity increment due to the additional semiconductors.

- *T-type converter* is an extension of the two-level voltage source inverter. Indeed, each switch node leg is connected to DC-Link mid-point through the

bidirectional switch. The mid-point current oscillations originate and have similar effects to the NPC and ACNP converters. However, this topology cannot be implemented for the considered application due to the required semiconductor technologies (i.e. a project constrain is the only usage of GaN semiconductors). As a matter of fact, for the two-level bridge leg switches, 1200V rating devices are needed and the GaN technology is limited to 650V due to lateral structure characteristics.

- *Flying Capacitor (FC) converter* does not present mid-point oscillation problems. Moreover, it has a modular cell structure easy scalable for high level numbers. The main drawbacks are the FC balance and the start-up and shut-down procedures. On the contrary, the structure does not present GaN device limitations (i.e. each cell present a two-level commutation loop) and well meet with high switching frequencies GaN features (i.e. the reactive elements are shrink).

All these aspect are summarized in Fig. 3.26. The next chapters will focus on the Flying Capacitor converter.

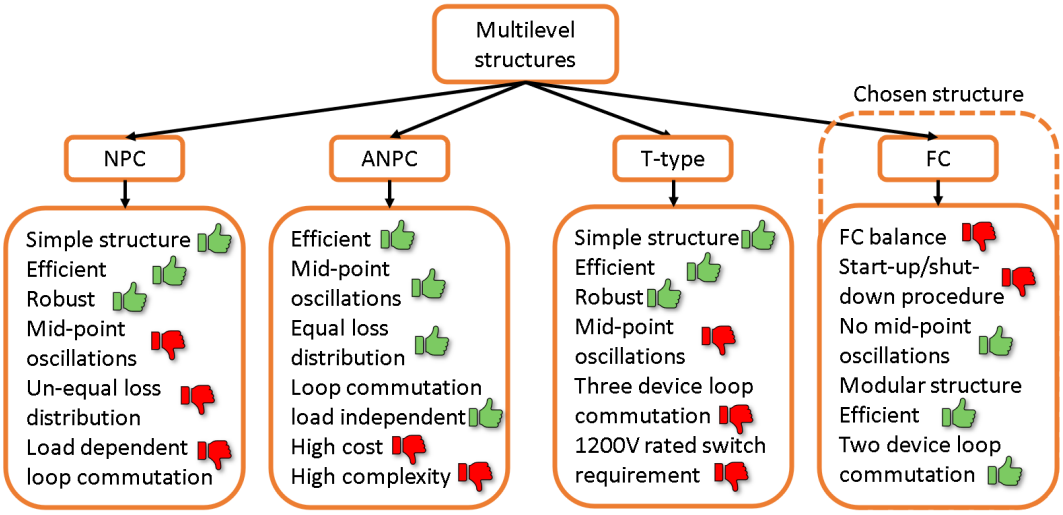


Fig. 3.26 Multilevel structure main features comparison and topology selection for the considered application.

Chapter 4

Capacitor Technology

4.1 Introduction

The traction inverter is one of the fundamental element in the electric vehicle powertrain as shown in Fig. 2.2. It has the role to realize the electric power conversion and to regulate the energy flow between the battery and the electric motor. As stated before, it is subject of a great pressure to improve the efficiency and the power density (i.e. both gravimetric and volumetric) to achieve the tighten quality standard required by the competitive automotive market. This pressure is lead to the capacitive reactive component, which plays a fundamental role in both two-level and multilevel structures. Indeed, the capacitive DC-Link is one of the bulkiest component in the power converter and thus directly limits its power density. It is currently realized employing the film capacitor technology. Consequently, it does not take any advantage by the higher switching frequency due to the WBG devices adoption, since the main limiting design requirement is the RMS current stress (i.e. not related to the f_{sw}). Moreover, the selection of state-of-the-art two-level inverter or multilevel topologies does not change the DC-Link sizing requirements (i.e. both voltage ripple and RMS current stress are the same) [191]. Since the optimization does not even depend on the converter structure, new improving solutions can be found by the usage of new capacitor technologies. Among them, the PLZT ceramic capacitors show better values of specific capacitance, maximum operating temperature and RMS current capabilities compared to standard film capacitors. They also feature a low series inductance mainly due to the relative small package. Moreover, the equivalent series

resistance (ESR) decreases along the rising frequency thus enabling a substantial benefit from the WBG power switch adoption. In literature, there are many papers that focus on the characterization and loss model of standard Class II multi-layer ceramic capacitors [192–196]. However, there are still few works on PLZT technology, especially with an experimental validation on a converter prototype [197–199].
This chapter firstly presents and compares the film and ceramic capacitor technologies. Then, an extension of the traditional 2LVSI DC-Link sizing procedure is presented. It takes into consideration the ESR variation proper of the ceramic technology. Moreover, the PLZT ceramic capacitor is experimentally tested to verify its effective thermal and electric capabilities. In the end, the proposed DC-Link design validation is performed on a standard two-level SiC EV traction inverter (i.e. featuring 800 DC-Link voltage and 550 kVA power rating). This structure has been chosen for its simplicity considering that the DC-Link stresses are the same of an equivalent to the 3LFC power converter. Indeed, the proposed theory and this experimental characterization will be used for the sizing of both the DC-Link and flying capacitors in the more complicated design of the three-level FC converter presented in the following chapter. All the arguments presented here are illustrated in the articles [200, 201].

4.2 Automotive Capacitor Technologies

The most relevant features of an automotive DC-Link can be summarized as:

- high specific capacitance (i.e. related to the require peak-to-peak voltage ripple constain);
- high RMS current capability which translates into high thermal conductivity and low ESR;
- high maximum operating temperature;
- high self-resonance frequency (i.e. mainly due to the equivalent series inductance related to the package dimension).

Even if electrolytic capacitors present excellent specific capacitance, they to not achieve the minimum standard in the other requirements. They are usually discarded

for the realization of high voltage automotive inverters [202]. Thus, only film and ceramic technology will be considered in the following analysis.

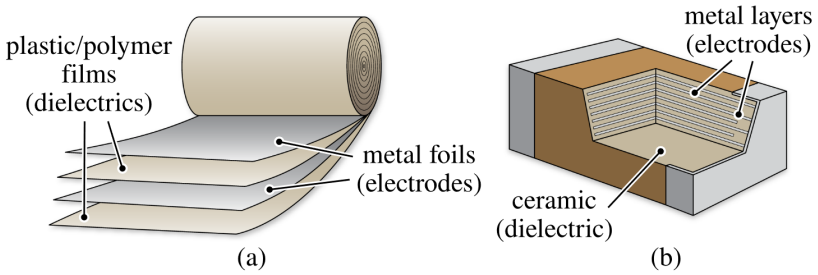


Fig. 4.1 (a) Film capacitors and (b) multi-layer ceramic capacitors (MLCCs) technologies internal structure scheme [201].

4.2.1 Film Capacitors

The film capacitors internal structure is illustrated in Fig. 4.1 (a). They are manufactured alternating metal layers (i.e. representing the two electrodes) with a polymer dielectric film. The adopted dielectric materials feature a relatively low permittivity which leads to a substantially low specific capacitance compared to the electrolytic capacitors. However, in the relevant switching frequency rage (i.e. from 10 to 100 kHz), the film ESR is practically constant. Then, it starts to increase with a $\sqrt{f_{sw}}$ dependence due to the skin effect in the metal contacts and foils, as illustrated in Fig. 4.2 (a). A first important conclusion is that film capacitor does not benefit or it is even negatively affected by the switching frequency increment. On the other hand, the ESR is almost constant related to the temperature variation (i.e. Fig. 4.2 (c)). Consequently, their maximum operating temperature range is around $100-125^{o}C$. Moreover, the self-healing properties enhance the overall DC-Link reliability which is highly appreciated in the automotive sector. The automotive DC-Link film capacitors are usually an optimized custom block. Their relatively big size leads to an high equivalent series inductances value. The consequent low self-resonance value directly limits the capacitor operating switching frequency range (i.e. thus limiting the potential benefit introduced by the WBG adoption). Another important drawback is the reduced self-heating temperature range (i.e. around $10-20^{o}C$). This limits the RMS current capability or sometimes imposes an active DC-Link thermal management.

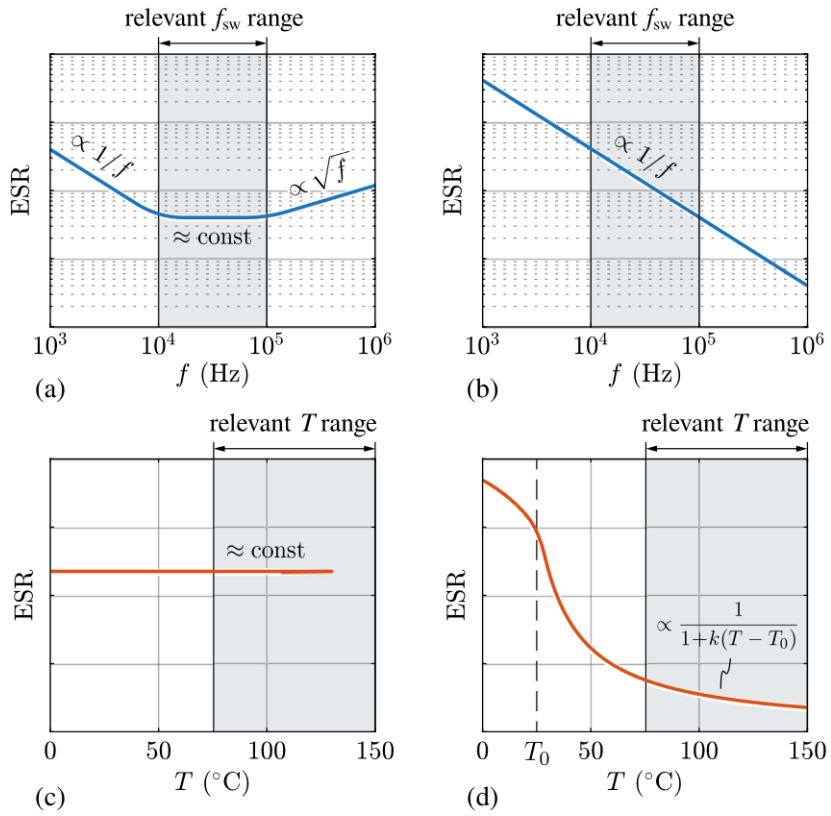


Fig. 4.2 Qualitative ESR curves dependences on frequency (a)/(b) and temperature (c)/(d) are shown for film capacitors (a)/(c) and PLZT ceramic technology (b)/(d). The relevant frequency and temperature automotive operating ranges are outlined [201].

4.2.2 Ceramic Capacitors

The ceramic capacitors usually show a multilayer structure which features the alternation of the metal electrodes soaked in a ceramic dielectric paste as illustrated in Fig. 4.1 (b). Due to this internal structure, they are also known as multilayer ceramic capacitors (MLCCs). Commonly they present higher operating temperature (i.e. up to 150^oC) and higher RMS current capabilities compared to film technology. They are available in small discrete packages (i.e. the dimension is limited by the brittleness of the ceramic paste). Since they have a low equivalent series inductance, they are suitable for high switching frequency operations. On the other hand, the main drawback is the need of parallel connection of various components to reach high capacitance values. This raises many problems regarding the displacement (i.e. the layout have impact on the mechanical forces distribution) and a proper current

sharing among the devices. The main classification is based on the ceramic paste type:

- **Class I** devices employ the titanium dioxide (TiO_2) ceramic paste. They are also classified by the C0G or NP0 code. These capacitors present an extremely linear dependence with the applied DC voltage an the operating temperature variation. Also the ageing is minimal. These ceramic capacitors are commonly used for all the applications that require a n high capacitance stability with low capacitance density.

- **Class II** elements utilize the barium titanate ($BaTiO_3$) ceramic paste. They are classified by the EIA coding system (i.e. X7R,X6R..), which defines tolerances and thermal properties. Compared to class I, they show a substantially higher capacitance densities. On the other hand, the utilized non-linear ferroelectric dielectric material causes a sensible capacitance drop with the increasing operating temperature and the applied DC bias voltage. In addition, the rigidity and brittleness of the dielectric paste make these components sensible to mechanical stresses and vibration that can causes a short-circuit failure. The consequent low reliability represents the main obstacle to overcome for the adoption in a DC-Link automotive applications.

- **Lead-lanthanum-zirconate-titanate (PLZT)** capacitors (i.e. CeraLink from TDK [203]) use the homonyms ceramic paste. Compared to class II ceramic capacitors, they show a higher specific capacitance at the rated voltage. Furthermore, the employed antiferroelectric material features a permittivity increment with the increasing DC bias voltage [204, 205]. The ESR almost decrease linearly with the temperature, as shown in Fig. 4.2 (d), this allows a substantially high operating temperature rating of 150^oC. However, above 75^oC, the capacitance features a negative temperature coefficient ensuring a natural current balance among all the paralleled devices and thus preventing the thermal run-away [197]. The equivalent series resistance also decrements approximately as $1/f$ as reported in Fig. 4.2 (b). This trend translates in an enhanced RMS current capability related to a incremented converter switching frequency (i.e. as prospected by the WBG device adoption). Regarding the reliability, the considered PLZT capacitors from TDK are released with a flex assembly package that makes the device more resistant to the applied mechanical forces. Moreover, the internal structure features two capacitors connected in series

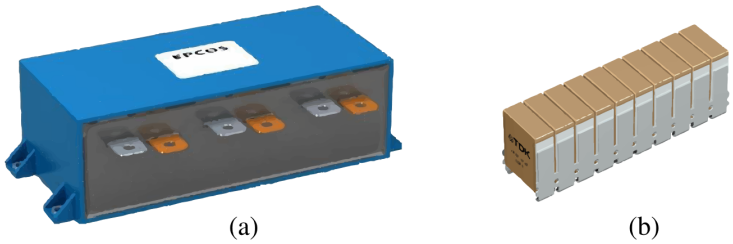
which substantially prevent the component failure due to the first crack in the dielectric paste and thus improving the overall reliability. Finally, the package copper electrodes contribute to further rise the RMS currents capability and thermal dissipation performances ratings.

Considering all these features, the PLZT ceramic capacitors are the best candidate to realize a full-ceramic automotive DC-Link. More detailed comparison between PLZT and class II ceramic capacitors can be found in [197, 198, 206]. Consequently, the CeraLink PLZT ceramic capacitors from TDK will be considered the benchmark in the following section.

4.2.3 Performance Comparison

In order to perform a proper technological performance comparison, two high-voltage, high-performance capacitors available on the market have been selected. In particular the benchmarks are the B25655P9127K51 film capacitor by EPCOS [207] and the Ceralink FA10 PLZT ceramic capacitor by TDK [208]. They are described in Table 4.1 and Fig. 4.3. In particular, it is considered the small-signal capacitance value for the PLZT ceramic technology. Indeed, the datasheet provides different capacitances rating since the capacitance is variable according to the DC voltage bias excitation. However, the small-signal value represents a conservative choice because it is the worst-case capacitance value for the DC-Link application (i.e. where a large DC bias voltage with a relatively low AC voltage ripple is applied on the DC-Link capacitor).

Since the selected benchmarks present sensibly different absolute value parameters, a preliminary performance comparison is shown in Fig. 4.4 using relatives terms.



(a) (b)

Fig. 4.3 Selected technologies benchmark for the comparison [201]:(a) B25655P9127K51 film capacitor by EPCOS [207], (b) Ceralink FA10 PLZT ceramic capacitor by TDK [208].

Table 4.1 FEATURES OF THE 900V CAPACITORS BENCHMARK SELECTED FOR THE COMPARISON

	Film	**Ceramic**
Manufacturer	EPCOS (TDK)	TDK
Part Number	B25655P9127K51	Ceralink ®FA10
Rated Voltage	900V	900V
Rated Capacitance	120 μF	1.3μF^*
Rated RMS Current	120A	32A
Maximum Temperature	105^oC	150^oC
Volume	554.4cm^3	2.0cm^3
Weight	800g	11.5g

*small-signal value at 800V

With the exception of the gravimetric capacitance density, it can be concluded that the PLZT ceramic technology substantially outperform the film one. In particular the main advantages lay in the RMS current capabilities. Since this represents the main limiting criterion for the the realized film-based DC-Links, the PLZT ceramic technology has the potential to enhance the performances of the DC-Link for the future EV traction inverters.

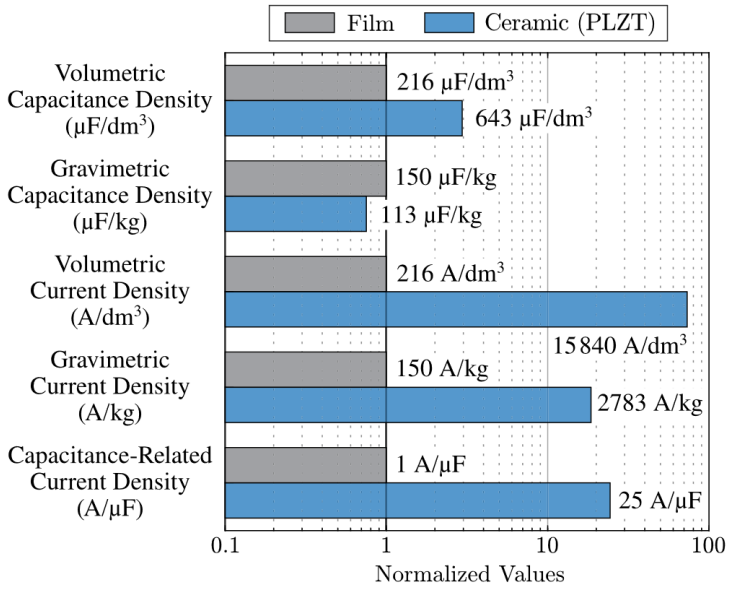


Fig. 4.4 Preliminary technological comparison of the selected capacitor benchmarks using relatives terms. The resulting specific performance indexes are obtained normalizing with respect to the Film capacitors values and represented in logarithmic scale [201].

4.3 DC-Link Sizing Procedure

In this paragraph the DC-Link design procedure for a three-phase two-level inverter is illustrated. In the next section, it will be validated on a 550 kVA 800 V SiC EV traction inverter by exploiting the substantial structure and experimental set-up simplicity compared to multilevel topologies. Since the stresses are the same [191], all the considerations and the results obtained will be used in the DC-Link design for the three-phase three-level flying capacitor converter presented in the next chapter. Moreover, a similar procedure slighted modified to consider the proper stresses will be presented for the flying capacitors design.
To sum up, a DC-Link has to satisfy two design constrains at the same time: to stand the maximum RMS current (i.e. it generates losses and the relative capacitor temperature rise) and to ensure a fixed peak-to-peak voltage ripple amplitude (i.e. to limit the voltage commutated by the semiconductors). Supposing to neglect the phase current ripple the RMS current flowing in a inverter DC-Link can be analytically expressed as [209]:

$$I_{C_{dc},RMS} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi} + cos^2\phi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right]} \tag{4.1}$$

where the modulation index is calculated as $M = 2V/V_{dc}$ (i.e. V is the peak value of reference voltage and V_{dc} is the DC-Link voltage), I is the value of the peak phase current and ϕ is the load power factor angle. As explained in [209], this RMS value is not affected by the PWM modulation strategy adopted. Its worst case value is obtained for $\phi = 0$ and $M = 10\sqrt{3}/9\pi$, resulting:

$$I_{C_{dc},RMS,max} = \frac{5}{2\sqrt{3}\pi}I \approx 0.46I \tag{4.2}$$

Fig. 4.5 shows the normalized (i.e. with the peak phase current I) DC-Link RMS current stress in relation to the converter power factor angle ϕ and modulation index M. There is a linear dependence between the voltage ripple ($\Delta V_{dc,pp}$) and the capacitor peak-to-peak charge ripple ($\Delta Q_{C_{dc},pp}$). It can be expressed through the DC-Link capacitance value C_{dc} as:

$$\Delta Q_{C_{dc},pp} = C_{dc} \Delta V_{dc,pp} \tag{4.3}$$

Unfortunately, a generic analytical expression similar to the RMS current stress is not available for the peak-to-peak charge ripple. This is mainly due to the fact that it depends on ϕ, M and the selected modulation techniques [210]. Fig. 4.6 shows the numerical calculation of the normalized (i.e. with the factor $\Delta Q_n = I/f_{sw}$) DC-Link peak-to-peak charge ripple $\Delta Q_{C_{dc},pp}$ stress in relation to the converter power factor angle ϕ and modulation index M (i.e. the SVPWM technique is selected). The worst-case design point is obtained for $M = 2/\sqrt{3}$ and $\phi = \pm\pi/2$. The resulting expression (i.e. independent by the modulation strategy) is [210]:

$$\Delta Q_{C_{dc},pp,max} = \frac{1}{4}\frac{I}{f_{sw}} \tag{4.4}$$

As specified before the DC-Link design must ensure that the capacitor satisfies at the same time all the described constrains:

$$C_{dc} = max[C_{dc,I_{RMS}}, C_{dc,\Delta V_{pp}}] \tag{4.5}$$

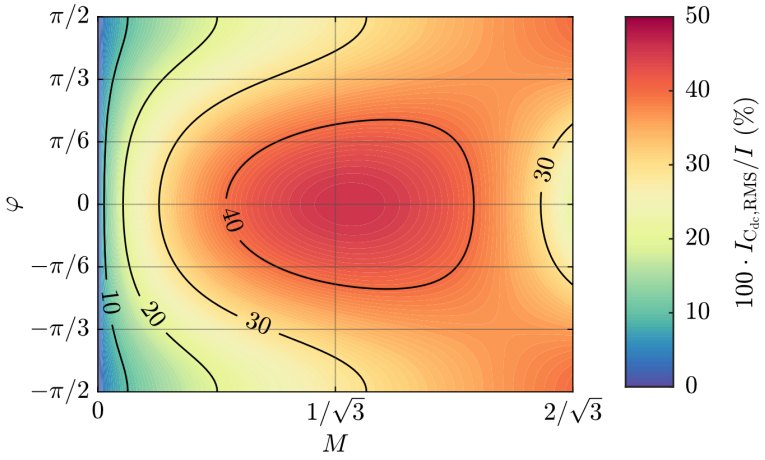


Fig. 4.5 Map of the normalized (i.e. with the peak phase current I) DC-Link RMS current $I_{C_{dc},RMS,max}$ stress in relation to the converter power factor angle ϕ and modulation index M [201].

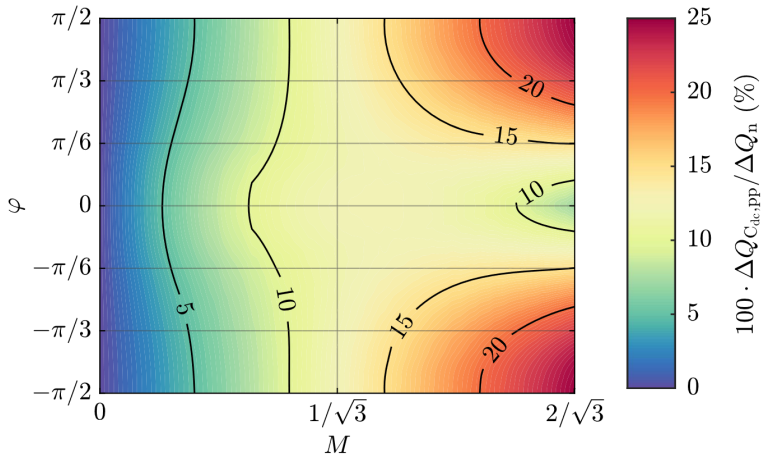


Fig. 4.6 Map of the normalized (i.e. with the factor $\Delta Q_n = I/f_{sw}$) DC-Link peak-to-peak charge ripple $\Delta Q_{C_{dc},pp}$ stress in relation to the converter power factor angle ϕ and modulation index M (i.e. the SVPWM is selected) [201].

Once the maximum peak-to-peak DC-Link voltage ripple $\Delta V_{dc,pp,max}$ allowed by the application is decided, combing 4.4 and 4.5, $C_{dc,\Delta V_{pp}}$ results:

$$C_{dc,\Delta V_{pp}} = \frac{\Delta Q_{C_{dc},pp,max}}{\Delta V_{dc,pp,max}} = \frac{1}{4}\frac{I}{f_{sw}\Delta V_{dc,pp,max}} \tag{4.6}$$

The $C_{dc,I_{RMS}}$ expression needs some more considerations. The generated losses and the device thermal dissipation depends on several factors such as ESR, temperature, operating frequency, physical dimensions and the component configurations (i.e. parallel/series). A simplified scheme of a capacitor is shown in Fig. 4.7 (a). The relative capacitor losses are:

$$P = R_{ESR}(f,T)I_{RMS}^2 \tag{4.7}$$

where I_{RMS} is the RSM current which flows in the capacitor and R_{ESR} is its equivalent series resistance (i.e. it depends on the operating frequency and temperature). From now on, it is assumed the simplified hypothesis of a sinusoidal current at the frequency f.

The thermal model scheme which describes the capacitor loss dissipation towards the surrounding ambient is shown Fig. 4.7 (b) and gives the following expression:

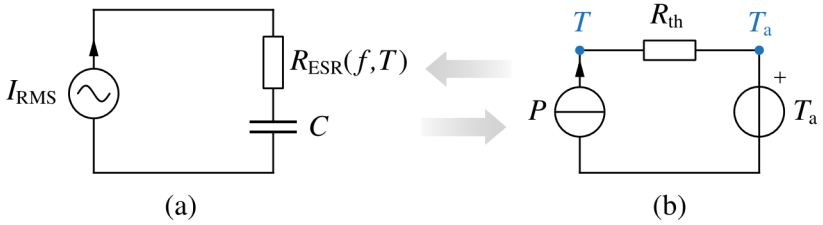


Fig. 4.7 (a) capacitor simplified electrical scheme and (b) its equivalent thermal circuit.

$$T - T_a = PR_{th} \tag{4.8}$$

where P is the dissipated power, R_{th} is the thermal resistance and T is the temperature achieved by the device compared to the ambient one T_a. Therefore, manipulating the last two equations, the capacitor RMS current capability results:

$$I_{RMS} = \sqrt{\frac{T - T_a}{R_{th}R_{ESR}(f,T)}} \tag{4.9}$$

The generic ESR temperature and operating frequency dependences can be assumed respectively as $R_{ESR}\alpha 1/f^{\alpha}$ and $R_{ESR}\alpha 1/[1+k(T-T_0)]^{\beta}$ according to Fig. 4.2. Considering N parallel capacitors (i.e. $N = C/C^*$), the consequent scaling laws can be expressed as:

$$\begin{cases} R_{ESR}(f,T) = R^*_{ESR}(f^*,T^*)\dfrac{C^*}{C}\left(\dfrac{f^*}{f}\right)^{\alpha}\left(\dfrac{1+k(T^*-T_0)}{1+k(T-T_0)}\right)^{\beta} \\ R_{th} = R^*_{th}\dfrac{C^*}{C} \end{cases} \tag{4.10}$$

where the signal * refers to the value of a single device of the considered parallel configuration (i.e. assuming the nominal operating condition specified in the datasheet provided by the manufacturer). Making the same assumption of Fig. 4.2, $\alpha \approx \beta \approx 0$ for film capacitors and $\alpha \approx \beta \approx 1$ for PLZT ceramic technology. From equations 4.9 and 4.10, the capacitor RMS current scaling law can be calculated as:

$$I_{RMS} = I^*_{RMS}\frac{C}{C^*}\left(\frac{f}{f^*}\right)^{\alpha/2}\left(\frac{1+k(T-T_0)}{1+k(T^*-T_0)}\right)^{\beta/2}\sqrt{\frac{T-T_a}{T^*-T^*_a}} \tag{4.11}$$

The total RMS current flowing in the DC-Link features several component at different frequencies. However, in a conservative design procedure, it is reasonable to consider the worst-case condition where the complete RMS current is associated at the f_{sw} (i.e. in other words, the lowest frequency in the spectrum). Inverting the previous equation, the $C_{dc,I_{RMS}}$ has the following expression:

$$C_{dc,I_{RMS}} = C^* \frac{I_{C_{dc},RMS,max}}{I^*_{RMS}} \left(\frac{f^*}{f_{sw}} \right)^{\alpha/2} \sqrt{\frac{T_{max} - T^*_a}{T_{max} - T_a}} \tag{4.12}$$

where T_{max} is the maximum working temperature of the capacitor.
The two DC-Link sizing constrains (i.e. related to $C_{dc,I_{RMS}}$ and $C_{dc,I_{RMS}}$) are depicted in Fig. 4.8 for both film and PLZT ceramic technologies. They are represented in normalized form (i.e. with respect to the peak phase current I) in relation to the converter switching frequency. $V_{dc} = 800V$, $T_a = 85^oC$ and $\Delta V_{dc,pp,max} = 10\% \cdot V_{dc}$ are hypothesized. A first conclusion is that, at low f_{sw} values, the limiting criterion is related to the capacitance needed to guarantee the target DC-Link voltage ripple. On the other hand, at higher switching frequencies the RSM current related constrain becomes the most stringent. The frequency boundary between the two limits is substantially different between the two technologies. In this case, for the film capacitor, it is around $7kHz$ as shown in Fig. 4.8 (b), while the CeraLink technology allows a sensible capacitance reduction if the switching frequency is further increased. It must be pointed out that once that the frequency boundary is achieved, the DC-Link capacitance requirements remain constant for film technology and keep decreasing for PLZT ceramic capacitor. This means that even if the RMS current constrain is dominant, it is still possible to have lighter the DC-Link requirements for higher switching frequency for CeraLink capacitor (i.e. due to the $ESR\alpha 1/f$ trend).

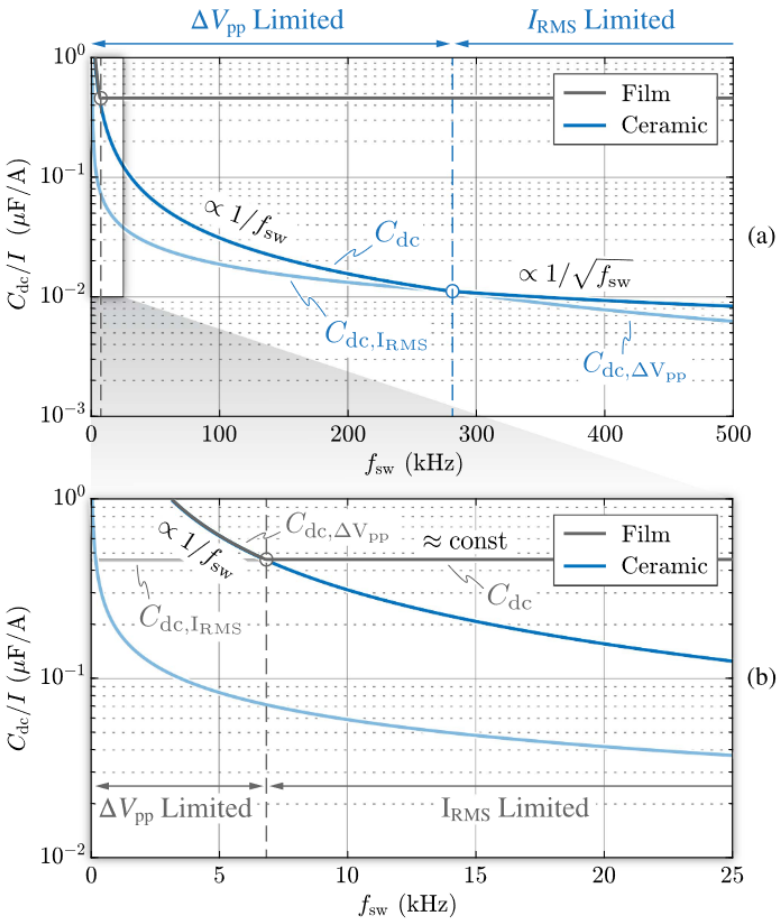


Fig. 4.8 DC-Link voltage ripple and RMS current related design constrains in relation to the switching frequency and normalized with the phase peak current I. The frequency boundary between the two constrains is outlined for both film and PLZT ceramic technologies. (b) highlight the $0 < f_{sw} < 25kHz$ region. $V_{dc} = 800V$, $T_a = 85^oC$ and $\Delta V_{dc,pp,max} = 10\% \cdot V_{dc}$ are hypothesized [201].

4.4 PLZT Ceramic Capacitor Experimental Characterization

In this section, some electrical and thermal characterization tests are performed on a single CeraLink FA3 capacitor sample [208] (i.e. rated 900V and 390nF small-signal capacitance value) in order to verify the hypothesis assumed by the models described in the previous paragraph. The realized experimental set-up schematic is shown in Fig. 4.9. It features a SiC MOSFET half-bridge operated in buck configuration at a

fixed duty-cycle (i.e. $d = 0.5$). The device under test (DUT) (i.e. the CeraLink FA3) is the converter DC-Link. The DC power supply is completely decoupled through a large inductor (i.e. L_i). This configuration ensures that the AC components of the current commutated by the buck converter flows completely in the DUT. With this assumption, the current flowing in the DC-Link capacitor is a square wave with an amplitude equal to $I_o/2$ as shown in Fig. 4.10. The consequent stresses can be expressed as:

$$I_{RMS} = \frac{I_o}{2}, \quad \Delta Q_{pp} = \frac{1}{4}\frac{I_o}{f_{sw}} \tag{4.13}$$

All the experimental tests presented in the following subsections are performed by varying systematically the DC-Link voltage bias V_{dc}, the converter switching frequency and the output load current I_o. These represent the set-up degrees of freedom outlined in blue in Fig. 4.9.

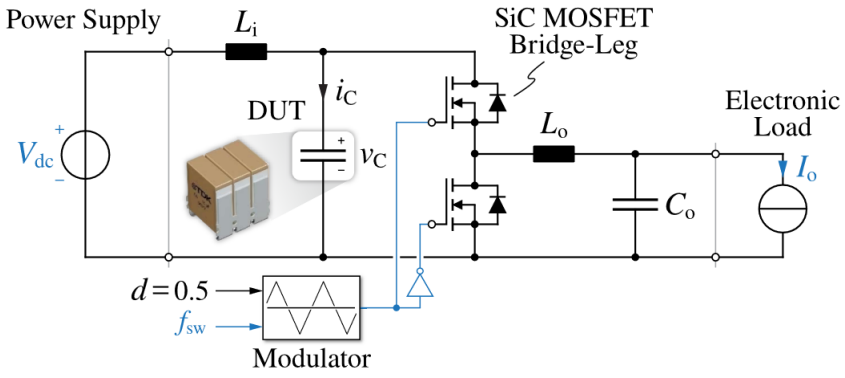


Fig. 4.9 Experimental set-up scheme used to test the CeraLink FA3 [208]. The filtering elements have the following values: $L_i = L_o = 64mH$ and $C_o = 66uF$. The half-bridge leg employs two SiC MOSFET C3M0032120K by Wolfspeed (i.e. 1200V, $32m\Omega$). The set-up three degree of freedom are I_o, V_{dc} and f_{sw}[201]

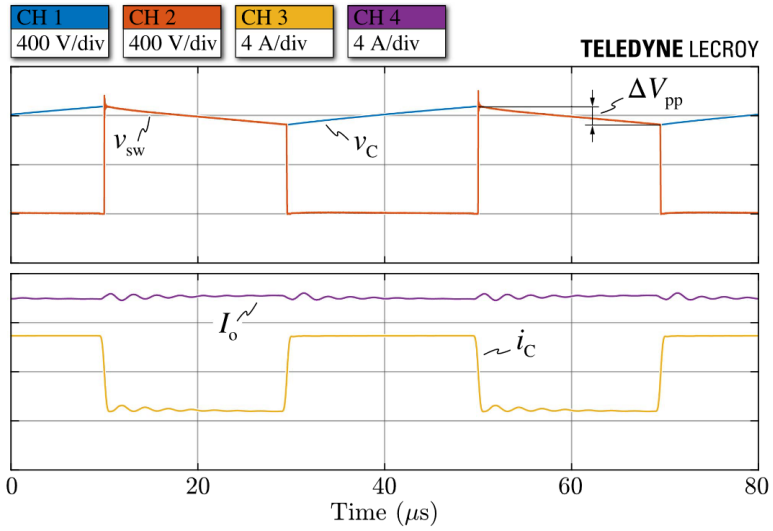


Fig. 4.10 DUT current i_c and voltage v_c, the half-bridge switch-node voltage V_{sw} and the output current I_o experimental waveforms. The tests conditions are: $I_o = 6A$, $V_{dc} = 800V$ and $f_{sw} = 25kHz$[201].

4.4.1 Peak-to-Peak Voltage Ripple

The first test aims to verify the equivalent capacitance C_{eq} of the device. As it is known, for these capacitors, C_{eq} changes with the amplitude of the excitation (i.e. in other words the voltage voltage ripple) due to hysteretic antiferroelectric behaviour of the PLZT dielectric [208]. Therefore, these tests measure the peak-to-peak voltage variation in relation to the imposed charge ripple (i.e. changed varying I_o according to 4.13). It is important to notice that these curves are not provided by the manufacture. However, they are important for a precise DC-Link design.
In Fig. 4.11 (a) and (b), the measured voltage ripple ΔV_{pp} and C_{eq} (i.e. $C_{eq} = \Delta Q_{pp}/\Delta V_{pp}$) are illustrated as function of the DC bias voltage and ΔQ_{pp}. The tests are performed at $f_{sw} = 25kHz$ featuring short burst period to avoid the heat-up of the DUT during the measurement (i.e. it is kept approximately costant at $T \approx T_a \approx 23^oC$). A first conclusion is that ΔV_{pp} does not present a linear trend respect to ΔQ_{pp} (Fig. 4.11 (a)), consequently there is an equivalent capacitance increase for higher charge ripple excitations (Fig. 4.11 (b)). Moreover, the antiferroelectic behaviour proper of PLZT ceramic capacitors is clearly visible by the DC bias voltage dependence of C_{eq} curves. Fig. 4.11 (c) shows the relation between C_{eq} and ΔV_{pp}. The $C_{eq}(\Delta V_{pp})$ curves are not provided by the manufactures, but they give fundamental informations

for a precise DC-Link design. Looking at the 800V curve, it is visible that for the considered design point (i.e. $\Delta V_{dc,pp,max} = 10\% V_{dc} = 80V$ as illustrated in the following section), the experimental measurements result in lower C_{eq} value than the small-signal capacitance (i.e. $C^* = 390nF$), implying a $\approx 11\%$ capacitance mismatch.

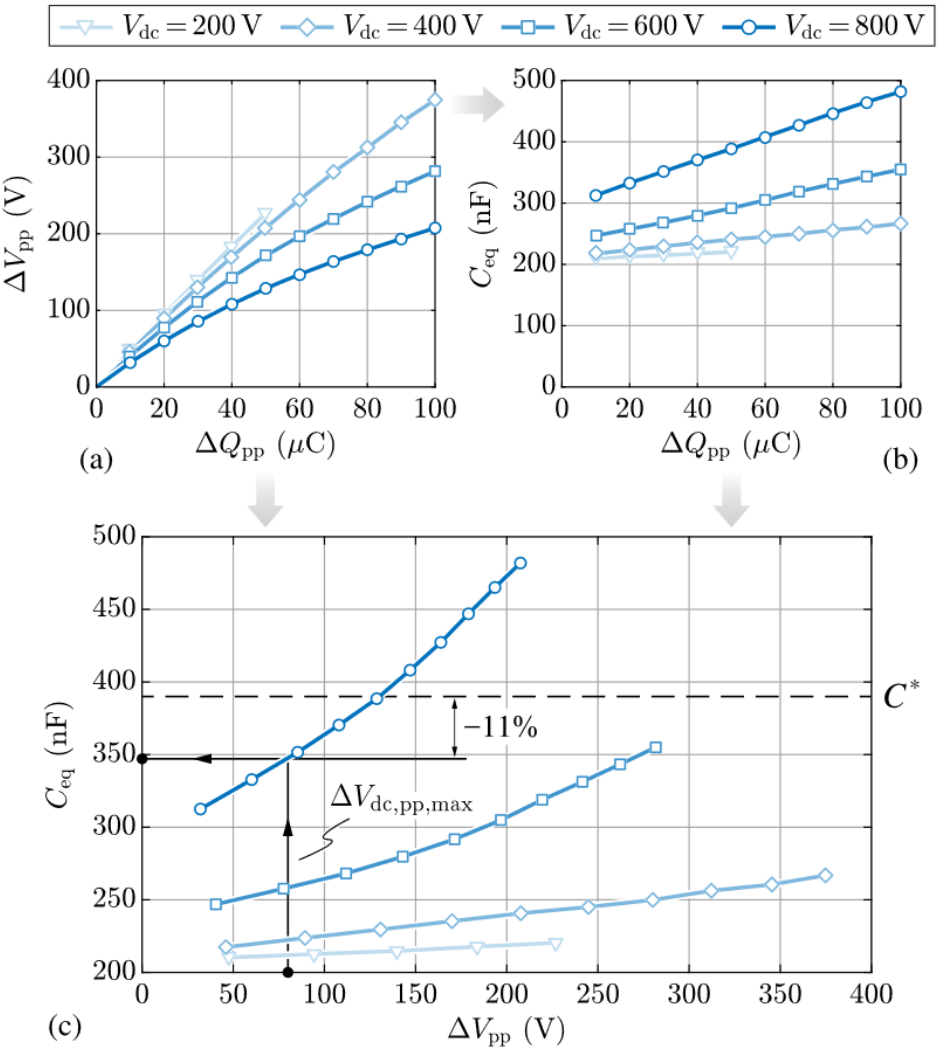


Fig. 4.11 Experimental measurements of (a) ΔV_{pp} and (b) C_{eq} in relation to the peak-to-peak charge ripple ΔQ_{pp}. (c) show the consequent relation between C_{eq} and ΔV_{pp}. The considered design point is outlined showing a $\approx 11\%$ capacitance mismatch. The tests are performed at variable DC bias voltage, $f_{sw} = 25kHz$ and $T_a = 23^oC$ [201].

4.4.2 RMS Current Capability

The following tests aim to verify the scaling law adopted in the previous section to obtain the equation 4.12. The DC bias voltage is set at 800V while the switching frequency varies. Then, the temperature rising (i.e. with respect to $T_a = 23^oC$) of the capacitor is monitored by a thermal camera for different RMS current stresses. All these experimental measurements are shown in Fig. 4.12. The first consideration is that the device temperature increases linearly with the RMS current (i.e. not αI^2_{RMS}). It suggests that the ESR capacitor decreases proportionally with the temperature rising. This is confirmed by the trend illustrated in Fig. 4.2 (d), making the hypothesis of $k(T - T_0) \gg 1$(i.e. high valued of T or k), as reported in the following equation:

$$\frac{R_{ESR}(T)}{R_{ESR}(T_0)} = \frac{1}{1+k(T-T_o)} \approx \frac{1}{k(T-T_o)} \tag{4.14}$$

Moreover, in Fig. 4.12 it is visible that when the operating switching frequency halves, there is a $\approx \sqrt{2}$ increment factor on the device temperature (i.e. due to the capacitor losses rise αESR). Taking into consideration that the ESR is inversely proportional to the temperature riseing as explained in equation 4.14. If this effect is compensated, halving the f_{sw} corresponds to have a double ESR. Also in this case the R_{ESR} proportion to $1/f$ is verified for large signal excitation.

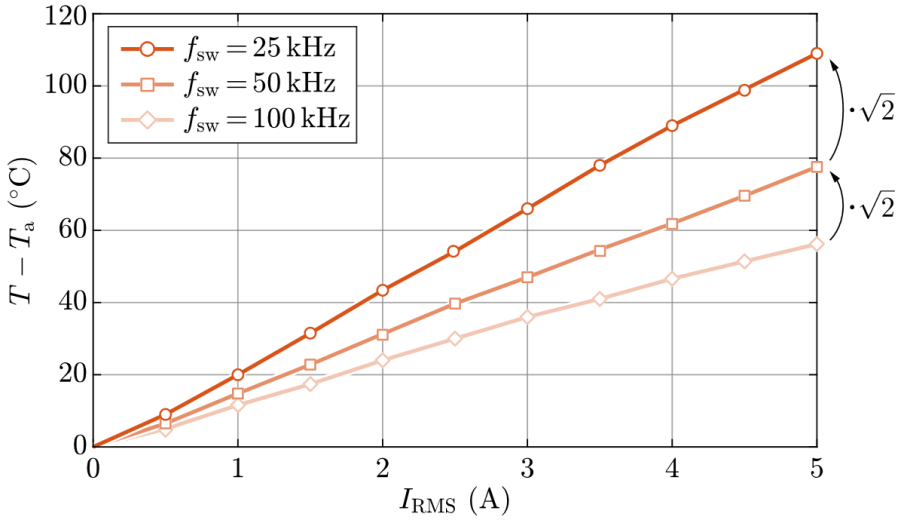


Fig. 4.12 Experimental DUT temperature measurement for different RMS current stresses and different operating switching frequencies. These tests are performed at $V_{dc} = 800V$ and $T_a = 23^oC$ [201].

4.5 Experimental Validation on a Two-Level 550kVA Automotive Inverter

This paragraph starts with a brief description of the two-level inverter prototype realized to validate the proposed models and DC-Link sizing procedure. Then, the experimental tests are presented. In particular, the measurement of the peak-to-peak DC-Link voltage ripple will be compared to the large-signal model-based estimations. As said before, it has been preferred to start the experimental test in a well-known, simple and easy to debug structure. The obtained results will be used in the sizing of the DC-Link and flying capacitor in the next chapter for the three-level FC prototype.

4.5.1 Realized Inverter Prototype

The nominal specification of the three-phase inverter prototype are illustrated in Table 4.2 and a complete description is presented in [211]. It features a full-ceramic DC-Link and DC-side EMI filter integrated in a IP 67 aluminium case. In particular Fig. 4.13 (a) and (b) show respectively a 3D view with all the main part specified and the prototype view.

Table 4.2 REALIZED INVERTER PROTOTYPE SPECIFICATIONS (NOMINAL CONDITIONS)

Parameter	**Description**	**Value**
S	Apparent Power	550kVA
I	Peak Phase Current	795A
V_{dc}	DC-Link Voltage	800V
f_{sw}	Switching frequency	20 kHz

The power stage is composed by three automotive Danfoss half-bridge modules (i.e. SiC MOSFET 1200V 2.1 $m\Omega$, DP660b1200T105606). They are cooled by a direct cooling technology (i.e. the liquid coolant flows in contact with the base plate of the module) enabling an high heat extraction rate and thus high current operation. The active cooling is implemented with a custom heatsink integrated in the aluminium case, as shown in Fig. 4.14. The final inverter prototype features a closed-loop control through the usage of a control board specifically designed.

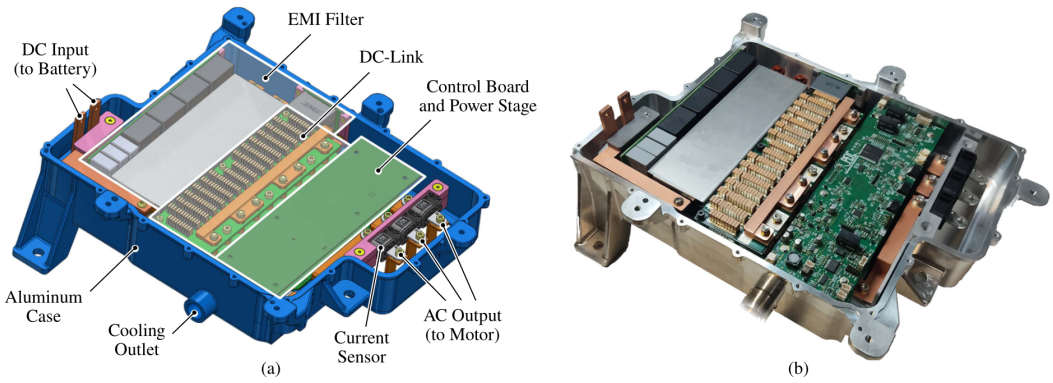


Fig. 4.13 (a) 3D overview and (b) prototype view of the 550 kVA 800V EV traction inverter featuring a full-ceramic DC-Link, a DC-side EMI and the power semiconductor stage integrated in a Ip 67 aluminium case [211].

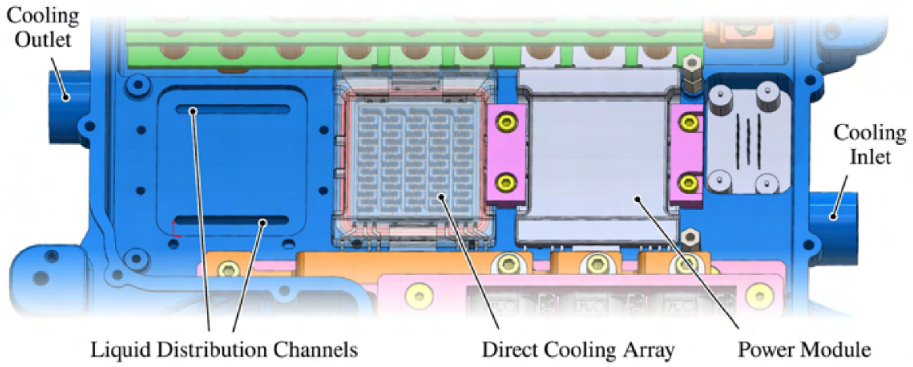


Fig. 4.14 Direct cooling structure integrated in the inverter aluminium case 3D overview [211].

DC-Link Sizing and Realization

A DC-Link design has been performed considering the inverter specification of Table 4.2 for both film and PLZT ceramic technologies. The adopted design procedure is illustrated in Section 4.3. It is assumed an inverter ambient temperature of $T_a = 85^oC$ and $\Delta V_{dc,pp,max} = 10\% V_{dc} = 80V$. The comparison of weight, volume, capacitance, RMS current and peak-to-peak voltage ripple is shown in Fig. 4.15. As specified before the limiting design constrain is the RMS current for the film technology and the $\Delta V_{dc,pp,max}$ for the ceramic capacitors. This leads to a capacitance requirement respectively of 365μF and 125μF.

At the time of the DC-Link design, no large-signal experimental test reported in the previous section were performed. Thus, the small-signal capacitance (i.e. provided by the manufacturer) has been used in the sizing. As shown in Fig. 4.11, this

assumption leads to a $\approx 11\%$ of DC-Link capacitance under-sizing at the target voltage ripple ($\Delta V_{dc,pp,max} = 80V$). From this consideration, the importance of the large signal $C_{eq}(\Delta V_{pp})$ provided in the previous section is clear. In conclusion, superior theoretical benefit for the volume and weight are achieved by the PLZT ceramic solution. This is mainly due to the high RMS current capabilities of the CeraLink technology. Indeed, the RMS current constrain limit is encountered for high switching frequency values, as shown in Fig. 4.8. This corresponds to a substantial capacitance requirement reduction if the f_{sw} is increased. This is not true for film capacitors where this increment does not provide any benefit, since the limit criterion is reached for low frequency values (i.e. $\approx 7kHz$ in Fig. 4.8).

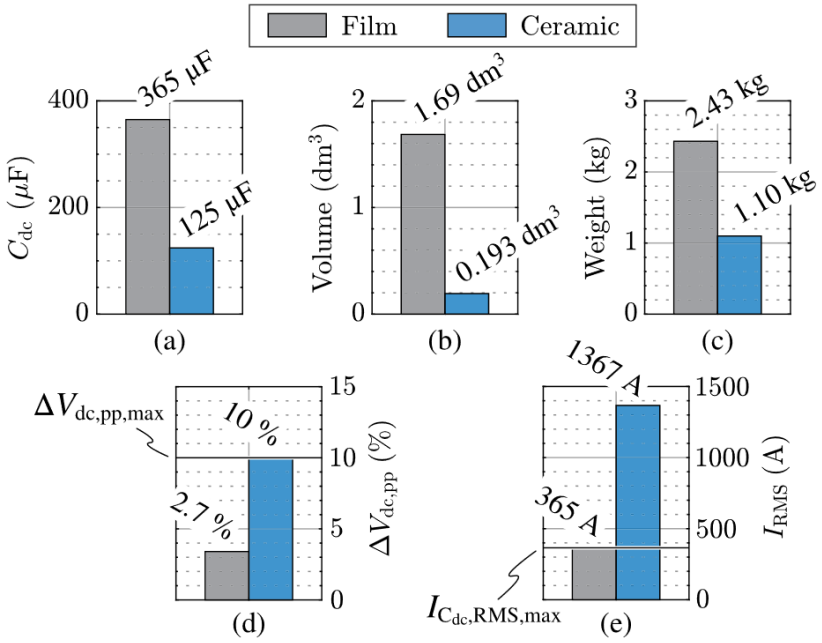


Fig. 4.15 DC-Link sizing results comparison between film and PLZT ceramic technologies: (a) DC-Link capacitance (C_{dc}), (b) volume, (c) weight, (d) peak-to-peak voltage ripple ($\Delta V_{dc,pp}$) and (e) RMS current capability. It is assumed an inverter ambient temperature of $T_a = 85^oC$ and $\Delta V_{dc,pp,max} = 10\% V_{dc} = 80V$ [201].

Fig. 4.16 (a) shows a 3D overview of the DC-Link assembled with the PLZT ceramic capacitor realized for the considered inverter prototype. It features three equal PCB board (i.e. 800 μm copper thick) interconnected by stand-offs and busbars. They compressively house 80 FA10 B58035U9255M001 (1.3 μF each) [208], 60 FA3 B58035U9754M062 (0.39 μF each) [208] and 6 LP B58031U9254M062 (0.25 μF each) [212]. The total capacitance amount is 128 μF (i.e. slightly higher than the requirement of Fig. 4.15). The upper board has capacitors mounted only on

the top face, while the other two also at the bottom. Moreover, 6 LP devices are positioned only in the lower board near the power modules inputs with the role of decoupling capacitors (i.e. with the main aim to minimize the commutation loop inductance) as shown in Fig. 4.16 (b).

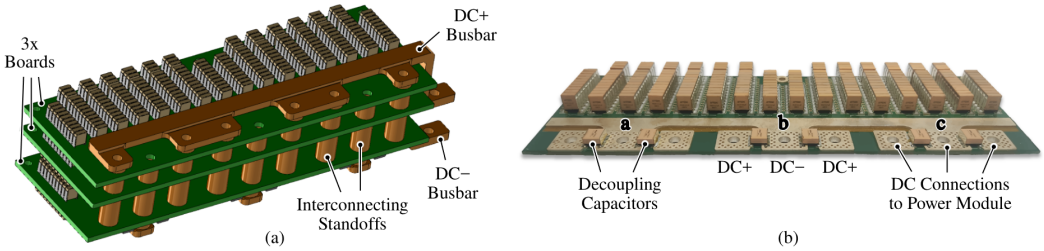


Fig. 4.16 (a) DC-Link 3D overview realized with PLZT ceramic capacitors and (b) bottom view of the lower board showing the decoupling capacitors [211].

The realized DC-Link (i.e. excluding busbars and interconnections) has a total weight of 1.73kg and a volume equal to 0.53 dm^3, as shown in Fig. 4.17. It is clear that these values are far away from the theoretical prospects shown in Fig. 4.15 (i.e. respectively ≈ 1.6 and ≈ 2.7 times lower).

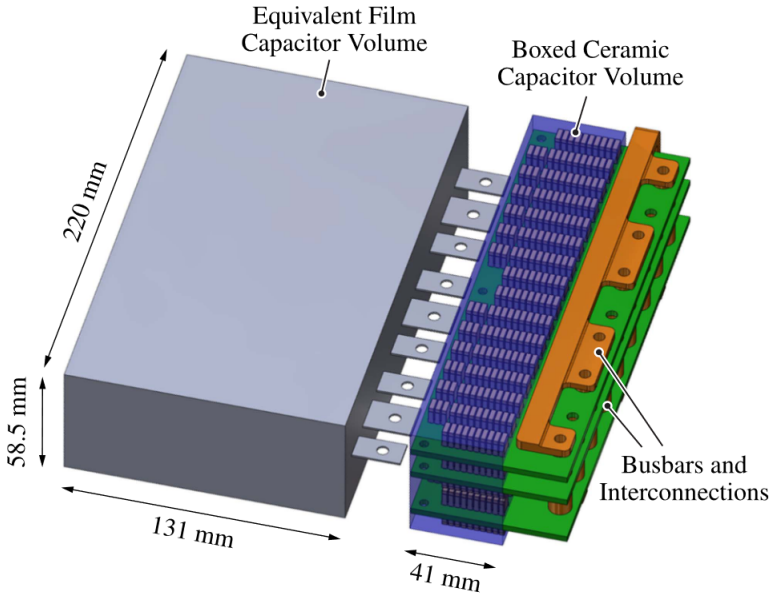


Fig. 4.17 3D comparison between the realized full-ceramic DC-Link assembly and the performance-equivalent film-based alternative[211].

The weight mismatch can be attributed to the additional thick-copper PCBs, while in the volume case it is mainly due to the creepage and clearance required by the application. The assembly volume could be strongly reduced adopting industrial manufacturing process and dielectric molding compounds. Even if the inefficient volume usage (i.e. due to the prototype nature of the inverter), the realized DC-Link feature 29% lower weight and 69% lower volume compared to the relative film-based solution.

4.5.2 Experimental Validation

The DC-Link design procedure described in Section 4.3 is now validated on the realized 550kVA 800V inverter prototype. Fig. 4.18 shows the used experimental set-up scheme. It features a current closed-loop control ($\approx 1kHz$ of bandwidth). The inverter has been tested on three-phase inductive load ($L = 105\mu H$) with high saturation currents (i.e. 400A). The testing on an electrical machine was not possible during the work for the thesis. To achieve an acceptable high modulation index the fundamental output frequency has been set to 400Hz for all the measurements. The main drawback of such solution was the low power factor due to the purely inductive load. However, when the converter is operating at low power factors, the voltage ripple on the DC link capacitor reaches its maximum, representing a worst-case working operating condition.

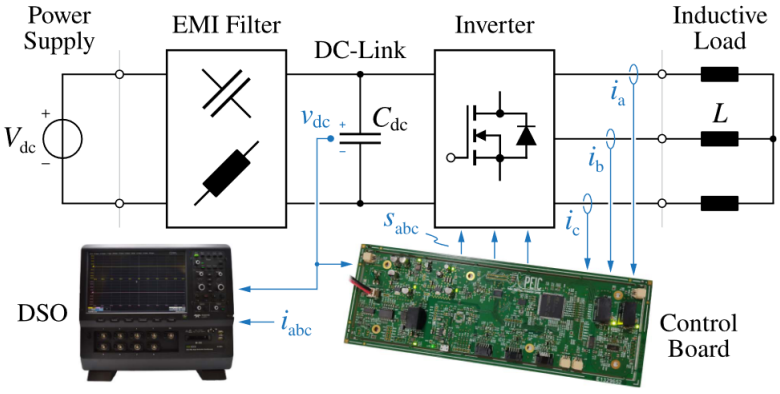


Fig. 4.18 Experimental set-up scheme adopted to evaluate the DC-Link peak-to-peak voltage ripple on the 550kVA inverter prototype. The system measure and and control (i.e. closed-loop) the three output phase currents (i_{abc}). The output inductances (i.e. $L = 105\mu H$) have a saturating current equal to 400A [201].

Several test have been performed varying the peak phase current from 0 to 400A and the DC-Link voltage from 200V to 800V. The resulting experimental measurements are shown from Fig. 4.19 to Fig. 4.22 with fixed peak phase current equal to 400A and variable DC-Link voltage from 200V to 800V. These results outline the DC voltage bias importance on the peak-to-peak voltage ripple. This phenomena can depend by two factors. The first one is the non-linear behaviour of PLZT ceramic that increases its capacitance with the polarization voltage. The second reason is attributed to the test conditions. Indeed, if the inverter is tested on a inductive load, the output fundamental frequency and the phase peak current are imposed. The modulation index is then inversely proportional to the DC-Link voltage (i.e. $M = 4\pi fLI/V_{dc} \alpha 1/V_{dc}$) and thus affect linearly the peak-to-peak voltage charge ripple.

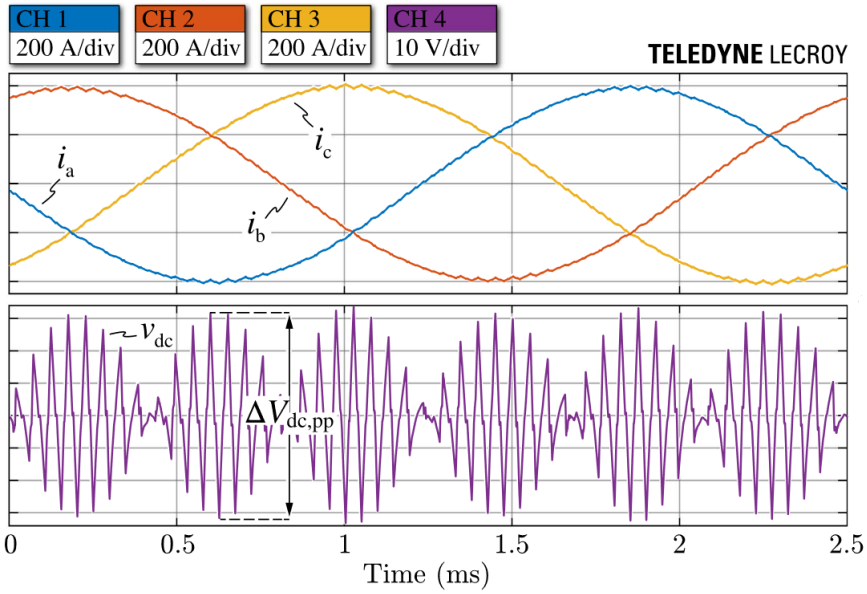


Fig. 4.19 Experimental measurement of the phase currents i_{abc} and DC-Link voltage ripple v_{dc} with I=400A and $V_{dc} = 200V$. To remove the switching noise a digital low-pass filter has been to v_{dc} (i.e. cut-off frequency 1MHz) [201].

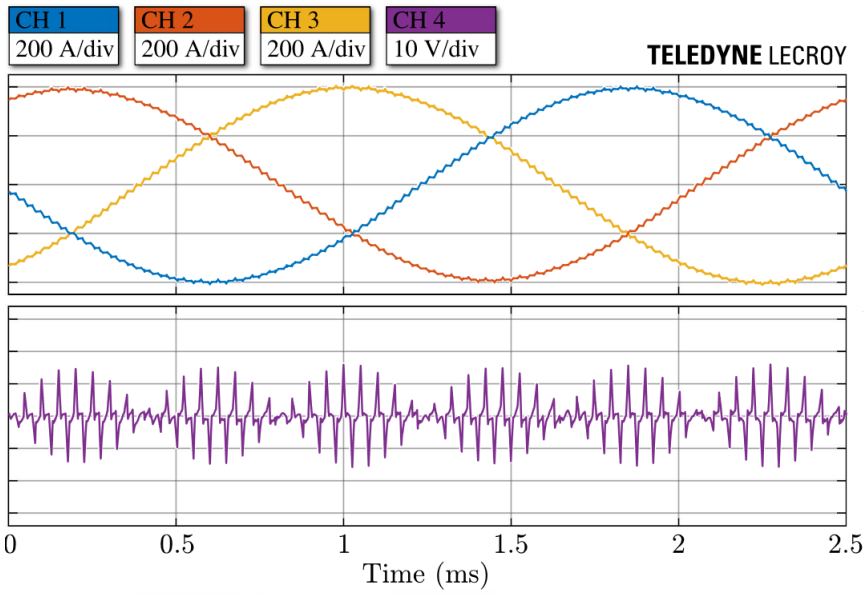


Fig. 4.20 Experimental measurement of the phase currents i_{abc} and DC-Link voltage ripple v_{dc} with I=400A and $V_{dc} = 400V$. To remove the switching noise a digital low-pass filter has been to v_{dc} (i.e. cut-off frequency 1MHz) [201].

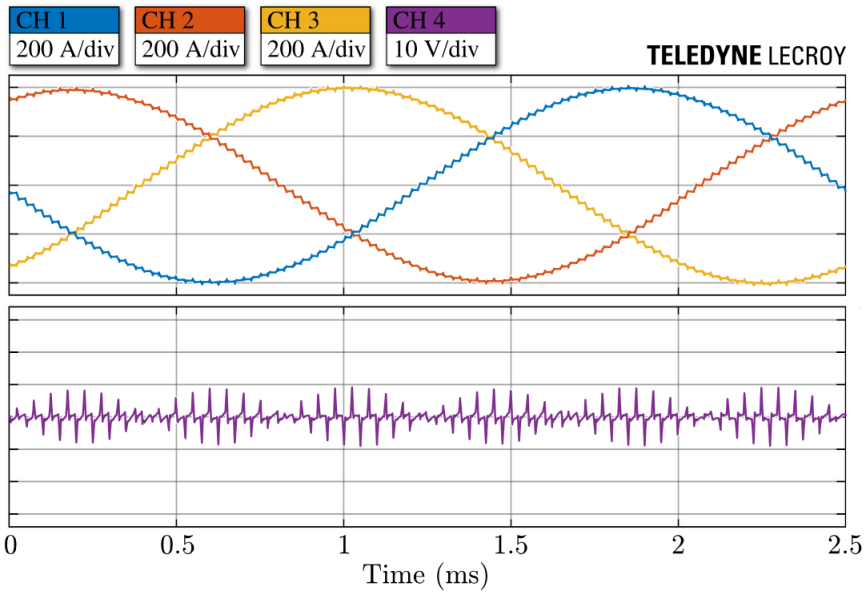


Fig. 4.21 Experimental measurement of the phase currents i_{abc} and DC-Link voltage ripple v_{dc} with I=400A and $V_{dc} = 600V$. To remove the switching noise a digital low-pass filter has been to v_{dc} (i.e. cut-off frequency 1MHz) [201].

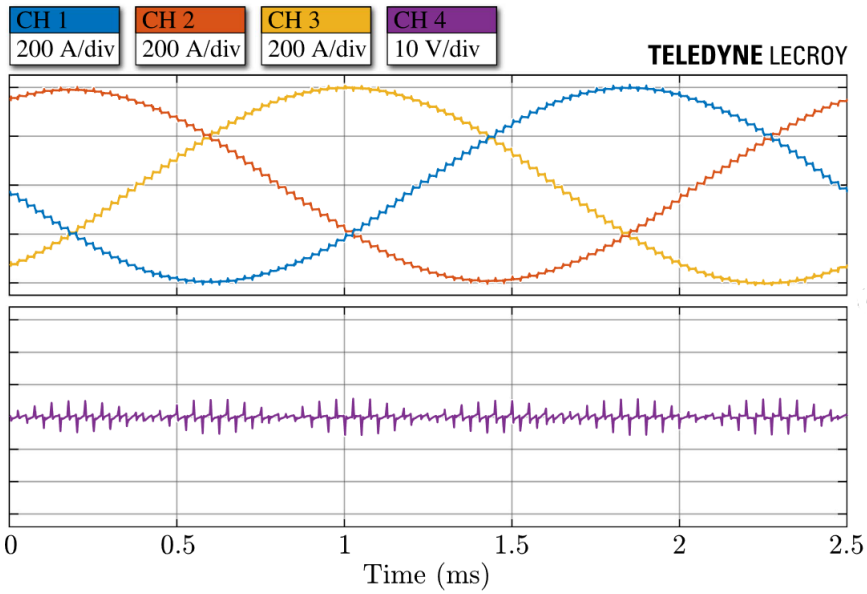


Fig. 4.22 Experimental measurement of the phase currents i_{abc} and DC-Link voltage ripple v_{dc} with I=400A and $V_{dc} = 800V$. To remove the switching noise a digital low-pass filter has been to v_{dc} (i.e. cut-off frequency 1MHz) [201].

DC-Link Voltage Ripple Estimation

The measurements of the DC-Link peak-to-peak voltage ripple must be compared to the result provided by the large-signal ($C_{eq}(\Delta V_{pp})$) relation obtained in Section 4.4. The $\Delta V_{dc,pp}$ model-based estimation procedure illustrated in Fig. 4.3 is divided into the following steps:

- *Step 1*: knowing M and ϕ by the experimental set-up test conditions, the normalized peak-to-peak charge ripple $\Delta Q_{C_{dc},pp}/Q_n$ is obtained by the map shown in Fig. 4.6;
- *Step 2*: $\Delta Q_{C_{dc},pp}$ is then calculated with a de-normalization according to the I and f_{sw};
- *Step 3*: the resulted charge ripple is scaled by the factor C^*/C^*_{dc} to obtain a value related to a single capacitor device;
- *Step 4*: knowing ΔQ_{pp} and V_{dc}, it is possible to extract the C_{eq} value by the experimental characterization performed on single device presented in Section 4.4 and shown in Fig. 4.11 (b);

- *Step 5*: the obtained equivalent large-signal capacitance is then scaled by a factor C^*/C^*_{dc} to be related to the considered DC-Link application;
- *Step 6*: the estimated peak-to-peak voltage ripple is then computed as $\Delta Q_{C_{dc},pp}/C_{dc,eq}$

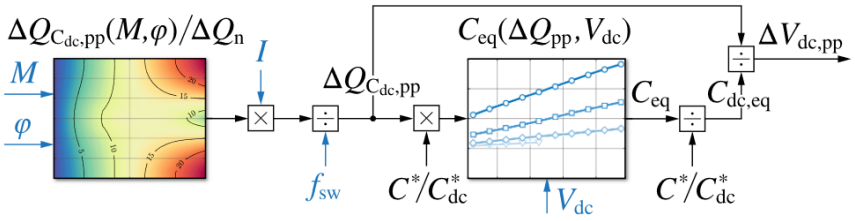


Fig. 4.23 The $\Delta V_{dc,pp}$ model-based estimation procedure depending by M, ϕ, I, f_{sw} and V_{dc} [201].

Comparative Results

The calculated model-based estimation values of the peak-to-peak voltage ripple are compared to the experimental measured counterpart in Table 4.3. The graphical representation of the same results is shown in Fig. 4.24. In particular, Fig. 4.24 (a) reports them as a function of the DC-Link voltage and peak phase current while Fig. 4.24 (b) as function of I and M. It is useful to remind again that M value strongly depends on V_{dc} for these tests performed on a inductive load and fixed output fundamental frequency.

It can be observed that using the method illustrated in Fig. 4.23 combined with the large-signal equivalent capacitance curves experimentally measured in Section 4.4 gives excellent accordance between the measured and the estimated peak-to-peak voltage ripple with a maximum relative error $\approx \pm 8\%$. Moreover, Fig. 4.24 (a) shows a dashed line representing the estimated $\Delta V_{dc,pp}$ considering the small-signal capacitance ($C^*_{dc}(800V)$) provided by the manufacturer. This assumption brings to a consistent voltage ripple underestimation (i.e. $\approx 20-30\%$ for the operating condition considered in figure). The large signal $C_{eq}(\Delta V_{pp})$ curves and the relative peak-to-peak voltage ripple estimation models have been verified. This supports the hypothesis of the DC-Link under-sizing $\approx 11\%$ supposed in Section 4.4. Consequently, the importance in the DC-Link design of the proposed large-signal capacitance estimation adopted is further highlighted.

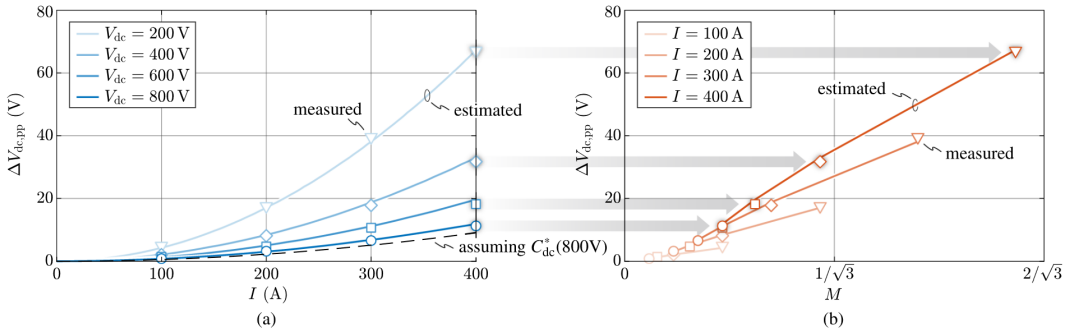


Fig. 4.24 Estimated vs Measured DC-Link Voltage Ripple: (a) as a function of the DC-Link voltage and peak phase current and (b) as function of I and M. [201].

Table 4.3 ESTIMATED VS MEASURED DC-LINK VOLTAGE RIPPLE

V_{dc}	I	M	**Measured** $\Delta V_{dc,pp}$	**Estimated** $\Delta V_{dc,pp}$	**Relative Error**
200V	100A	0.269	4.3V	4.3V	+0.0%
200V	200A	0.538	17.0V	17.0V	+0.0%
200V	300A	0.807	39.0V	38.1V	−2.3%
200V	400A	1.076	66.5V	67.3V	+1.2%
400V	100A	0.135	2.1V	2.1V	+0.0%
400V	200A	0.269	8.1V	8.4V	+3.7%
400V	300A	0.404	17.8V	18.8V	+5.6%
400V	400A	0.538	31.7V	33.0V	+4.1%
600V	100A	0.090	1.4V	1.3V	−7.1%
600V	200A	0.179	4.7V	5.0V	+6.4%
600V	300A	0.269	10.6V	11.2V	+5.7%
600V	400A	0.359	18.2V	19.6V	+7.7%
800V	100A	0.067	0.8V	0.8V	+0.0%
800V	200A	0.135	3.2V	3.0V	−6.3%
800V	300A	0.202	6.6V	6.8V	+3.0%
800V	400A	0.269	11.3V	11.9V	+5.3%

4.6 Conclusion

This chapter has presented a comprehensive DC-Link sizing and experimental validation for a EV 550kVA 800V SiC inverter employing a PLZT ceramic DC-Link. It has demonstrated that this can be considered as a key innovative technology to achieve the more and more tighten quality requirements of the future traction inverters.

The chapter starts with a brief introduction and description of the state-of-the-art film technology and PLZT ceramic capacitors. Then, two benchmarks (i.e. one for each technology) are identified. From a first comparison using relative terms the great theoretical potential of PLZT ceramic capacitors has emerged especially for the capacitance-related and gravimetric/volumetric current density. Afterwards, it has been presented a DC-Link sizing procedure for a two-level inverter. This topology has been selected due to its well-know and simple structure, which can thus allow an easier debug and experimental validation of the PLZT technology benefits. Since the DC-Link stresses are the same for all the voltage source inverter topologies (i.e. also for the three-level flying capacitor converter), the proposed procedure has still a general validity for the three-phase inverters. In particular, the RMS current and the peak-to-peak charge ripple stresses (i.e. fundamental constrain in the DC-Link sizing) are calculated and their dependences with temperature and operating switching frequency are outlined for each technology. From this analysis, it is clear that in opposition to film-based capacitor, the PLZT ceramic technology can achieve a substantial capacitance requirement decrement if the f_{sw} is increased. This represents an important feature the next generation inverters which employ WBG switches (i.e. SiC and GaN devices).

In order to validate the proposed thermal and electrical sizing relation some experimental tests have performed on a single PLZT ceramic capacitor. Hence a large-signal equivalent capacitance curve have been extracted (i.e. it is not provided by the manufacturer). Moreover, the RMS current capability frequency dependence has been verified. The proposed design procedure has been applied to a 550kVA automotive inverter prototype. The realized DC-Link feature one third lower weight and two third lower volume compared to the equivalent film-based counterpart.

Finally, the peak-to-peak voltage ripple estimated with the proposed large-signal equivalent capacitance model has been compared with the measured results on the inverter prototype showing excellent agreement.

Summarizing, it has been shown the superior performances of the PLZT ceramic technology. It can fully benefit by the switching frequency increment due to WBG devices adoption and thus can be considered a key technology to enhance the performances of future inverters.

Chapter 5

Three-Phase Three-level Flying Capacitor Converter

5.1 Introduction

The aim of this thesis is to realize a traction inverter prototype for motorsport applications. As specified many times, the inverter is a fundamental component of the EV power-train and thus is subject to a great pressure of improvements. The direct consequence is the continuous research of enhancement and evolution of the powertrain. The changing standard of the DC-Link voltage rating from 400V to 800V is a proof of this. This contributes to reduce the charging times and the cable size and weight. However, it is clear that to push forward the performance limits of the state-of-the-art solutions, new technologies and structures have to be employed. The improvement requirement focuses mainly on enhancing the converter efficiency and power density, on increasing the operating temperature capability and the switching frequency. The last requirement is important to provide sufficient margin control in low phase inductance load motors (i.e., typical of automotive electric motors with several pole-pairs and high speed [213]) and to reduce the PWM induced losses [169, 170]. The previous chapters analysed some innovative technologies and topologies that represent the scientific research response to these needs. The first technology identified is the GaN semiconductor. Indeed, since Si have reached the maximum theoretical limit with the IGBT and SJ structure, WBG semiconductor such as GaN and SiC with better physical properties have approached the market.

GaN technology has recently penetrated the automotive market promising better performances than Si/SiC devices (i.e., depending by the operating temperature and switching frequency as shown in Chapter 2). However, since it is still a not mature technology, it is limited to 650 voltage rating due to its lateral structure. To realize a 800 DC-Link voltage inverter is thus mandatory to use a multilevel topology. The adoption of GaN devices is not the unique selection criterion. Indeed, multilevel converters feature better performance compare to standard 2-level topologies in terms of synthesized output voltage waveform (i.e., low harmonic content) as it will be better explained later in the chapter. This is mainly due to the combination of a higher switching frequencies (enabled by the adoption of lower voltage rating devices with a better FOM) and of a lower voltage commutated step (that features lower dv/dt stress). In particular it is very important for low inductance high speed motors and in the induced PWM losses reduction. Among all the considered multilevel structure, the three-level flying capacitor converter has been selected as the best candidate for this application (i.e. no mid-point oscillations, modular structure, favourable commutation loop ...). However, this architecture presents some challenges related to the complex control an balancing mechanism.
Finally, also Ceralink PLZT ceramic technology has been identified as a key technology for future inverters. Its specific capacitance and RMS current capabilities allows to effectively benefit by the switching frequency increment (due to the combination of GaN devices and multilevel topology) to reduce the sizing capacitance requirement increasing the converter power density. This is a fundamental aspect for the three-level FC converter which features a large amount of capacitive reactive elements. Moreover, the discrete small package (i.e. with little equivalent series inductance) allows the integration of the DC-Link and FC near the power switches eliminating the need of decoupling capacitors and improving the commutation loop (fundamental for the high commutation derivatives proper of GaN devices). It can be pointed out that all the selected key innovative elements present complement features. The aim of this chapter is to exploit all these benefits to design an innovative inverter which is able to face the future challenging requirements of the motor-sport application.
Summarizing, a three-level FC converter employing GaN devices and Ceralink PLZT ceramic technology will be designed. The target prototype specifications are illustrated in Table 5.1 and the topology scheme is shown in Fig. 3.18.

Table 5.1 THREE-LEVEL FC INVERTER PROTOTYPE SPECIFICATIONS

Parameter	**Description**	**Value**
S	Apparent Power	100kVA
I	Peak Phase Current	145A
V_{dc}	DC-Link Voltage	800V
f_{sw}	Switching frequency	100 kHz

The current chapter is organized as follows. Firstly, the three-level component stresses are identified. Then, the component design and selection is described. Finally, the realized prototype is presented. The contents of this chapter are partially published in [140].

5.2 Component Stresses

This section analyses the stresses for the active and passive converter elements which represent the basis for the design and component selection presented later. The following analysis supposes the presence of a constant DC-Link voltage and a sinusoidal output current (i.e. the voltage and current ripples are neglected). Moreover, it is assumed that the switching frequency is sufficiently higher than the synthesized output frequency (i.e. $f_{sw}/f > 20$).

5.2.1 Semiconductor Devices Losses

Due to the three-level flying capacitor (3LFC) modular structure, each cell can be assimilated and modelled as a two-level leg which has to commutate only half of the DC-Link voltage. Consequently, the RMS current flowing in the device is not affected by the modulation strategy and it is equal to [191]:

$$I_{RMS} = \frac{I}{2} \tag{5.1}$$

where I is the peak value of the phase current. The current flowing determine the conduction and switching losses described in the following subsections.

Conduction Losses

Considering unipolar GaN devices, the conduction losses are proportional to square of the RMS current and represent the resistive behaviour of the device. For a single power switch:

$$P_{cond} = R_{ds,on} I_{RMS}^2 \tag{5.2}$$

The total conduction losses for a 3LFC converter result (i.e. identical power switches are assumed):

$$P_{cond,TOT} = 3R_{ds,on} I^2 \tag{5.3}$$

Switching losses

The switching losses can be calculated by the ON/OFF commutation energies curves provided by the switch manufacturer with the following expression:

$$p_{sw} = f_{sw}[E_{on}(i_{sw} + E_{off}(i_{sw})] \tag{5.4}$$

where i_{sw} is the instantaneous current and f_{sw} is the operating switching frequency. Following the hypothesis of fast switching transitions (i.e. neglecting the losses due to the current and voltage overlap and assuming $Q_{rr} \approx \tau_{rr} I_{sw}$), the switching energies have the following relation:

$$E_{sw}(i_{sw}) \approx V_{sw} Q_{oss}(V_{sw}) + V_{sw} Q_{rr}(i_{sw}) = k_0 + k_1 i_{sw} \tag{5.5}$$

Summarizing, under the assumption of fast-switching devices, the switching energies present a linear by the instantaneous current [140](i.e. for $i_{sw} < 0$, $E_{on} = E_{off} \approx 0$ and for $i_{sw} > 0$, $E_{on} \approx k_{0,on} + k_{1,on} i_{sw}$, $E_{off} \approx k_{0,off} + k_{1,off} i_{sw}$). The switching loss power related to a single device during a fundamental period can be thus expressed as:

$$P_{sw} = f_{sw} \left[\frac{1}{2}(k_{0,on} + k_{0,off}) + \frac{I}{\pi}(k_{1,on} + k_{1,off}) \right] \tag{5.6}$$

The resulting switching losses for a 3LFC are:

$$P_{sw} = 6 f_{sw} \left[\frac{1}{2}(k_{0,on} + k_{0,off}) + I \frac{2}{\pi}(k_{1,on} + k_{1,off}) \right] \tag{5.7}$$

5.2.2 Machine Phase Flux Ripple

The phase flux ripple $\Delta\psi$ represents a machine stress indicator for the following reason:

- it translates into a machine current ripple (i.e. inversely proportional to the motor phase inductance) related to the electric motor winding high frequency losses;
- it defines the high frequency flux swing applied to the machine core and magnet if present and thus it is proportional to the relative losses.

Summarizing, $\Delta\psi$ is an indicator of the PWM induced losses on the electric motor [170]. Since high speed and low phase inductance motor are usually employed in motor-sport applications, this represents an important performance index to compare the FC multilevel topology with a standard two-level inverter. In grid connected converter it consequently represents a qualitative performance index related to the loss/size of the output filter [191]. $\Delta\psi$ is generated by the high frequency component of the voltage applied to the motor. Fig. 3.21 shows the Matlab simulation of (a) output phase voltage and (b) phase flux ripple (i.e. simulated for a three-level flying capacitor inverter featuring 800V DC-bus voltage, 145A output peak phase current, 100 kHz switching frequency and 1 kHz output fundamental frequency). Considering a generic phase x, the phase flux ripple can be calculated as:

$$\Delta\psi_x = \int_0^t v_{x,HF}\, dt \; [x = a, b, c] \tag{5.8}$$

where $v_{x,HF}$ represents the phase voltage high frequency components.
The RMS value of $\Delta\psi$ is calculated as [140]:

$$\Delta\psi_{RMS}^2 = \frac{6}{T} \int_0^{T/6} \frac{\Delta\psi_a^2 + \Delta\psi_b^2 + \Delta\psi_c^2}{3}\, dt \tag{5.9}$$

Since it consider all the three phases contributions, $\Delta\psi_{RMS}$ is then assumed as a overall performance index. Assuming a third harmonic injection PWM technique, it has the following analytical expression:

$$\Delta\psi_{RMS} = \Delta\psi_n \sqrt{\frac{M^2}{384} - \frac{M^3}{288}\left(\frac{\sqrt{3}}{\pi} + \frac{17809}{8505\pi}\right) + \frac{M^4}{576}} \tag{5.10}$$

where the normalization factor is defined as $\Delta\psi_n = V_{dc}/f_{sw}$. A $\Delta\psi_{RMS}$ graphical normalized curves is compared to the two-level inverter counterpart in Fig. 5.1.

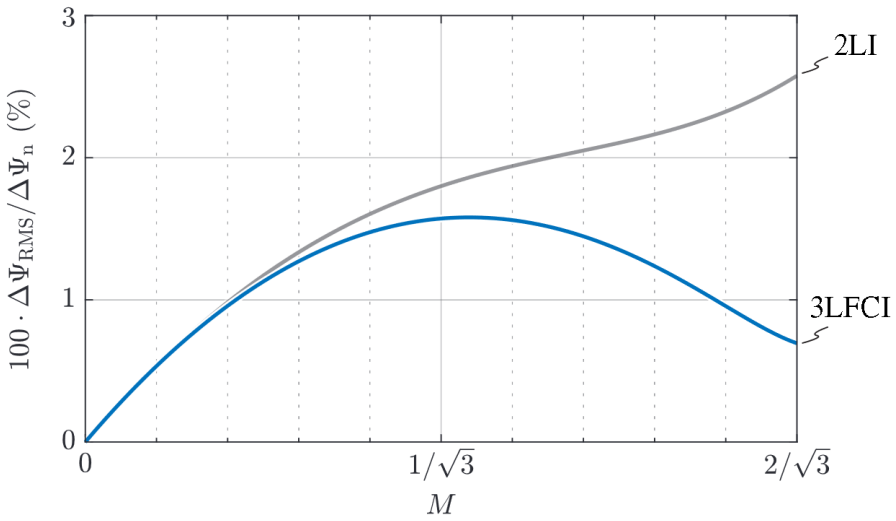


Fig. 5.1 Comparison between the three-level flying capacitor inverter (3LFCI) and two-level inverter of the normalized RMS flux ripple in relation to the modulation index M. $\Delta\psi_n = V_{dc}/f_{sw}$ [140].

The peak of equation 5.10 is at $M \approx 0.62$ leading to $\Delta\psi_{RMS,max} \approx 0.016\Delta\psi_n$. The worst-case for the two-level inverter is obtained at the maximum modulation index and corresponds to a maximum RMS flux value of $\approx 0.016\Delta\psi_n$ [191] and thus 60% higher than the 3LFC case.

Considering that the PWM induced losses in the electric motor are proportional to the $\Delta\psi^2_{RMS}$, it can be concluded that the 3LFC converter reduces these losses especially at high modulation indexes. In particular, compared to a two-level inverter the maximum reduction of $\approx 90\%$ is obtained at the maximum modulation index (i.e. considering the same DC-Link voltage and switching frequency). It is clear that further improvements can be achieved by higher switching frequencies (i.e. due to the adoption of lower voltage rated devices with a better FOM).

Summarizing, this analysis shows the benefit of the output voltage synthesized by the 3LFC (thanks to a reduced harmonic content) and consequently it shows the limitations of the tradition two-level inverter. A similar analysis can be performed for the other multilevel topologies (with the consideration that they do not feature the output doubling frequency effect). However, this represents a not negligible advantages in motor sport applications where the employed motors usually present low phase inductance and several pole-pairs.

5.2.3 DC-Link Capacitors

The instantaneous DC-Link current i_{dc} is calculated taking into consideration only the three phase currents (i.e. i_a,i_b and i_c) and the correspondent switching signal of the external bridge-leg (i.e. relative to cell 2 in Fig. 3.19), as shown in the following equation:

$$i_{dc} = i_{dc,a} + i_{dc,b} + i_{dc,c} = s_{a,ext} i_a + s_{b,ext} i_b + s_{c,ext} i_c \tag{5.11}$$

where it is assumed a pure sinusoidal phase currents three-phase system. Fig. 3.22 shows the Matlab simulation of (a) the DC-Link capacitor current and (b) the DC-Link capacitor charge ripple for one operating point (i.e. simulated for a three-level flying capacitor inverter featuring 800V DC-bus voltage, 145A output peak phase current, 100 kHz switching frequency and 1 kHz output fundamental frequency). The RMS current value flowing in the DC-Link capacitors is the obtained by removing to the DC-Link current its own mean value:

$$I^2_{C_{dc},RMS} = I^2_{dc,RMS} - I^2_{dc,avg} \tag{5.12}$$

where $I^2_{C_{dc},RMS} = 6/T \int_0^{T/6} i^2_{dc}\, dt$ and the DC-Link current mean value can be calculated as [209]:

$$I_{dc,avg} = \frac{3}{4} M I cos\phi \tag{5.13}$$

As reported in the previous chapter, the DC-Link capacitor RMS current stress for a 3LFC converter is equal to the two-level case and it has the following expression [209]:

$$I_{C_{dc},RMS} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi} + cos^2\phi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right]} \tag{5.14}$$

Fig. 5.2 shows the $I_{C_{dc},RMS}$ current stress as a function of the modulation index and of the load power factor angle for a 3LFC converter with the specification illustrated in Table 5.1. As specified for the two-level converter in Section 4.3, the worst-case value corresponds to $I_{C_{dc},RMS,max} \approx 0.46I$ and it is found for $M = 10\sqrt{3}/9\pi$ and $\phi = 0$.

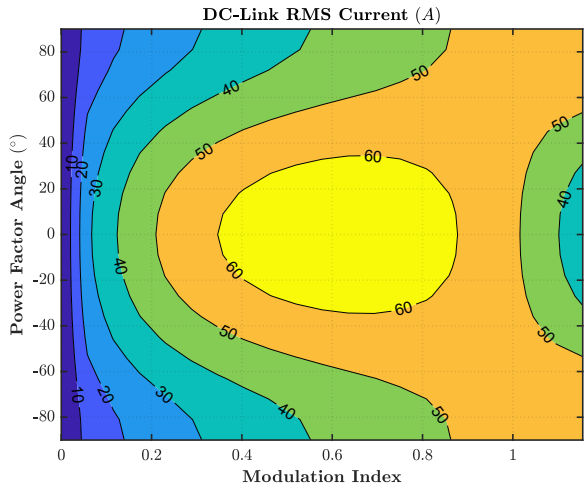


Fig. 5.2 DC-Link RMS current $I_{C_{dc},RMS}$ as a function of the load power factor angle and of the inverter modulation index for a 3LFC featuring 100kVA, V_{dc} = 800V and I = 145A.

By the integration of the high-frequency DC-Link current-time area component is obtained the capacitor charge ripple:

$$\Delta q_{C_{dc}} = \int_0^t i_{C_{dc}}\, dt \tag{5.15}$$

It is related to one of the two important DC-Link sizing constrains. Indeed its peak-to-peak value is proportional to the peak-to-peak DC-Link voltage ripple amplitude (i.e. $\Delta q_{C_{dc}} = C_{dc}\Delta V_{dc,pp}$). Also in this case, there is a strict parallelism with the two-level inverter case such that there is no analytical expression because

$\Delta q_{C_{dc}}$ strictly depends on the chosen modulation technique and on M and ϕ. Fig. 5.3 shows the $\Delta q_{C_{dc},pp}$ stress as a function of the modulation index and of the load power factor angle for a 3LFC converter with the specification illustrated in Table 5.1. As for the 2LI the worst case condition corresponds to $\Delta q_{C_{dc},pp,max} = 1/4\Delta Q_n$ (i.e. $\Delta Q_n = I/f_{sw}$). It is obtained for $M = 2/\sqrt{3}$ and $\phi = \pm\pi/2$.

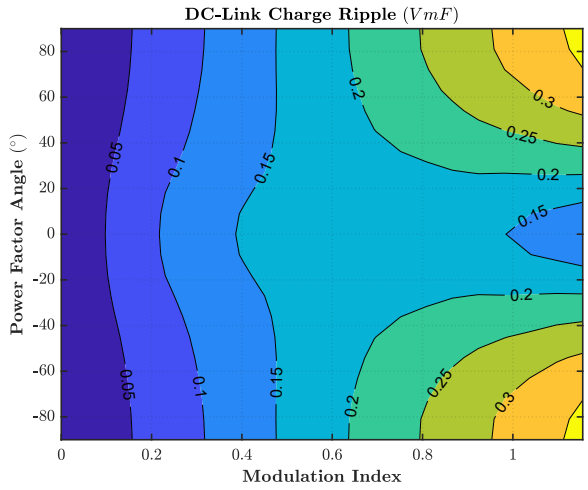


Fig. 5.3 DC-Link peak-to-peak charge ripple $\Delta Q_{C_{dc},pp}$ as a function of the load power factor angle and of the inverter modulation index for a 3LFC featuring 100kVA, V_{dc} = 800V and I = 145A.

5.2.4 Flying Capacitors

The instantaneous flying capacitor current features an average value of zero ($I_{fc,avg} = 0$) due to the phase-shift modulation technique illustrated in Section 3.2.4. Fig. 3.23 shows the Matlab simulation of (a) the FC current and (b) the flying capacitor charge ripple for one operating point (i.e. simulated for a three-level flying capacitor inverter featuring 800V DC-bus voltage, 145A output peak phase current, 100 kHz switching frequency and 1 kHz output fundamental frequency). Each flying capacitor current is obtained considering its own phase current and the switching signal of both cells according to:

$$i_{C_{fc}} = i_{fc} = (s_{x,int} - s_{x,ext})i_x, \quad x = a,b,c \tag{5.16}$$

The RMS current flowing in the flying capacitor is then obtained as:

$$I_{C_{fc},RMS}^2 = I_{fc,RMS}^2 = \frac{2}{T}\int_0^{T/2} i_{fc}^2\, dt \tag{5.17}$$

The analytical expression depends on the modulation technique. Choosing the third harmonic injection modulation, it results [140]:

$$I_{C_{fc},RMS} = I\sqrt{\frac{1}{2} - M\left(\frac{37}{45\pi} - \frac{7}{15\pi}cos^2\phi\right)} \tag{5.18}$$

However, the FC RMS worst-case current stress does not depend on the modulation technique. It can be obtained for the condition M=0 resulting:

$$I_{C_{fc},RMS,max} = \frac{1}{\sqrt{2}}I \approx 0.71I \tag{5.19}$$

Fig. 5.4 shows the $I_{C_{fc},RMS}$ current stress as a function of the modulation index and of the load power factor angle for a 3LFC converter with the specification illustrated in Table 5.1.

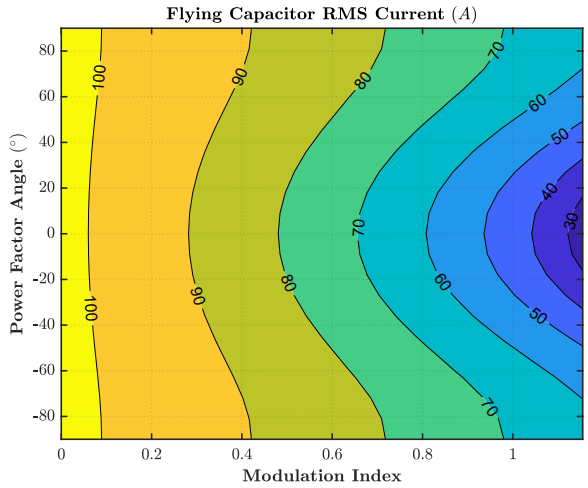


Fig. 5.4 DC-Link RMS current $I_{C_{fc},RMS}$ as a function of the load power factor angle and of the inverter modulation index for a 3LFC featuring 100kVA, V_{dc} = 800V and I = 145A.

Similarly to the DC-Link case, the FC charge ripple can be expressed as:

$$\Delta q_{C_{fc}} = \int_0^t i_{C_{fc}}\, dt \tag{5.20}$$

Also in this case, there is no analytical expression and numerical calculation must be performed. The flying capacitor peak-to-peak charge ripple $\Delta Q_{C_{fc},pp}$ is proportional to the peak-to-peak FC voltage ripple $\Delta V_{fc,pp}$. Fig. 5.5 shows the $\Delta Q_{C_{fc},pp}$ current stress as a function of the modulation index and of the load power factor angle for a 3LFC converter with the specification illustrated in Table 5.1. The worst-case value is obtained for M=0 resulting in:

$$\Delta Q_{C_{fc},pp,max} = \frac{\Delta Q_n}{2} \tag{5.21}$$

where the normalized factor is $\Delta Q_n = I/f_{sw}$. It can be pointed out that the maximum FC stresses are higher than the DC-Link case.

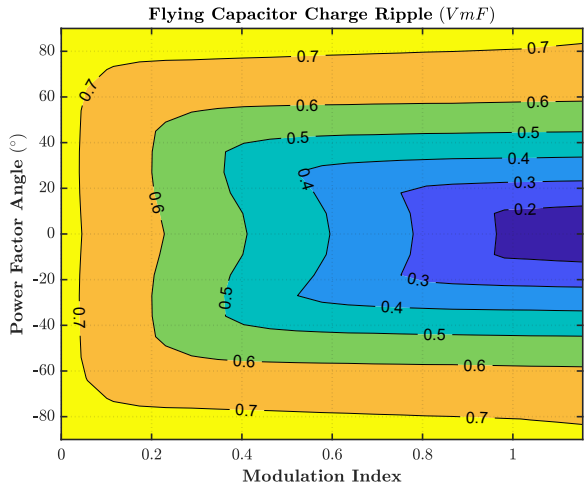


Fig. 5.5 DC-Link peak-to-peak charge ripple $\Delta Q_{C_{fc},pp}$ as a function of the load power factor angle and of the inverter modulation index for a 3LFC featuring 100kVA, V_{dc} = 800V and I = 145A.

5.3 Component Design/Selection

Considering the main stresses outlined in the previous Section, the selection and the design of the main converter component are now presented. The inverter specification are illustrated in Table 5.1.

5.3.1 Semiconductor Devices

Among all the GaN and SiC 600/650V devices performance comparison presented in Chapter 2, the V08TC65S2A has been selected for the realization of the 3LFC inverter prototype. Indeed, it has shown the best trade-off between the absolute on-resistance ($7.8m\Omega$ at 25^oC, $16m\Omega$ at 150^oC), the conduction/switching performances and the package features ($0.1K/W$ junction-to-case thermal resistance and electrically insulated cooling pad). An overview of the V08TC65S2A package is shown in Fig. 5.6.

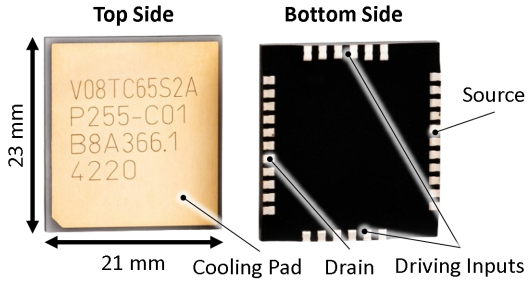


Fig. 5.6 Top and bottom view of the V08TC65S2A device form VisIC employed in the realized 3LFC prototype.

Fig. 5.7 shows (a) the conduction characteristic and (b) the ON/OFF loss energy curves extracted by the V08 datasheet. From Fig. 5.7 (b) the parameters useful calculate the switching losses expressed in equation 5.6 are thus obtained. In particular, $k_{0,on} = 44.3\mu J$, $k_{0,off} = 86.5\mu J$, $k_{1,on} = 3.18\mu J/A$ and $k_{1,off} \approx 0\mu J/A$.

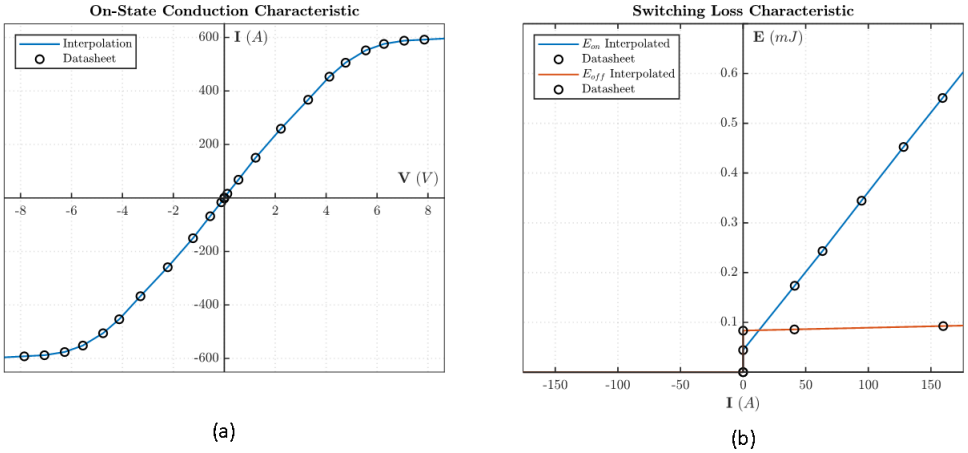


Fig. 5.7 (a) On-state conduction characteristic and (b) switching loss curves for the V08TC65S2A device form VisIC. The dots are the data obtained by the component datasheet and the line depicts the interpolation curve.

Assuming a cooling liquid temperature of $T_f = 40^oC$, the semiconductor losses and the consequent converter efficiency are illustrated in Fig. 5.8 for the nominal operating point (i.e. $V_{dc} = 800V$, $I = 145A$ and $M = 2/\sqrt{3}$). The design of the switching value imposes to consider a optimization trade-off. Indeed, a higher f_{sw} correspond to higher semiconductor losses, lower capacitance requirement (i.e. due to the obtained lower charge ripple) and lower PWM-induced losses in the motor load. Considering all these aspects, the selected switching frequency is $f_{sw} = 100kHz$. Defined the operating switching frequency, Fig.5.9 shows the converter efficiency related to the semiconductor as a function the peak phase current I and of the modulation index M (i.e. considering $T_f = 40^oC$ and $V_{dc} = 800V$).

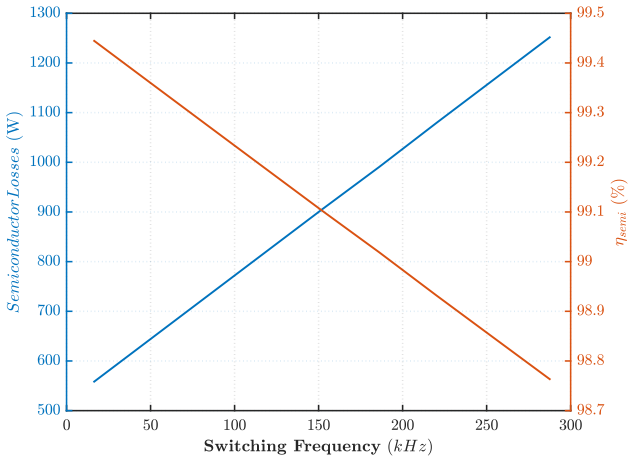


Fig. 5.8 Power loss (conduction and switching) and efficiency related only to semiconductors as a function of the switching frequency in nominal operating conditions (i.e. $V_{dc} = 800V$, $I = 145A$ and $M = 2/\sqrt{3}$). A liquid cooling temperature equal to 40^oC is assumed.

5.3.2 DC-Link and Flying Capacitors

As reported in the previous chapter, the PLZT ceramic technology presents excellent specific capacitances and RMS current capabilities. These features allow to effectively benefit by the rising switching frequency due to the combination of GaN devices and the multilevel topology, reducing the capacitance requirements compared to standard film technology. In particular, Ceralink capacitors from TDK are selected to realize both the DC-Link and the flying capacitors. Another important benefit is their low inductive package which results easier to integrate in the commutation loop as it is shown in the following section.

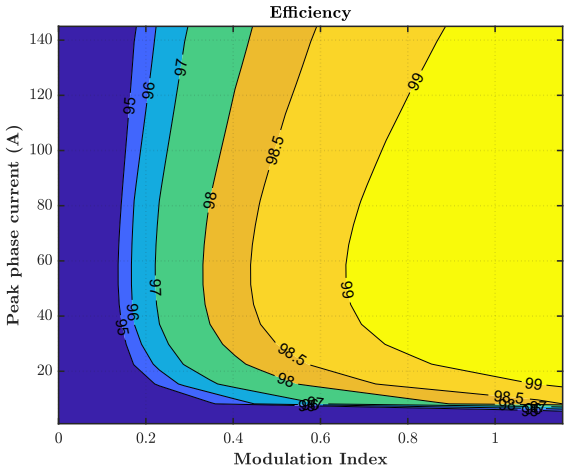


Fig. 5.9 Simulated efficiency (i.e. related only to semiconductors) a s function of the peak phase current I and of the modulation index M. A liquid cooling temperature equal to 40^oC, $f_{sw} = 100kHz$ and $V_{dc} = 800V$ is assumed.

Using the sizing equations described in the previous section, the maximum RMS current and peak-to-peak charge ripple are illustrated in Table 5.2 for both DC-Link and flying capacitors. The sizing procedure imposes to satisfy the two requirements at the same time. At the time of the design, it was not performed the PLZT ceramic characterization presented in Section 4.4, thus the small-signal value provided by the manufacturer has been used in the sizing procedure. In particular, the Ceralink FA3 900V $0.39\mu F$ and the Ceralink FA3 500V $1.8\mu F$ [208] have been selected.
In order to limit the possible commutated voltage by the devices, the maximum allowed peak-to-peak voltage ripple ha been set to $\Delta V_{pp,max,dc} = 5\%V_{dc} = 40V$ for the DC-Link capacitance C_{dc} and $\Delta V_{pp,max,fc} = 10\%V_{dc}/2 = 40V$ for the flying capacitors C_{fc}. This surely represents the more stringent requirement compared to the required RMS current constrain resulting in $C_{dc} \geq 9\mu F$ and $C_{fc} \geq 18\mu F$. In the final converter prototype more capacitance has been added according to the maximum space exploitable resulting $C_{dc} = 12.9\mu F$ (i.e. $\Delta V_{pp,max,dc} = 28V$) and $C_{fc} \geq 19.8\mu F$ (i.e. $\Delta V_{pp,max,fc} = 37V$). This solution complies with the prospected design constrains.
It must be pointed out that the PLTZ technology offers unique advantages, especially when multiple capacitors are connected in parallel. The highest capacitance is achieved at a temperature of 75 ^oC [208], with further temperature increases leads to decreased capacitance and subsequently lower current flow through the capacitor. Furthermore, for working temperatures above 75 ^oC, the ESR of the device stabilizes

[208]. Therefore, the losses will depend only on the current sharing between the capacitors which in turn depends on the parasitics and the capacitance. In other words, if one device heats up more than the others, its reduced capacitance leads to less current sharing, resulting in lower losses.

Table 5.2 DC-LINK AND FLYING CAPACITOR MAXIMUM DESIGN CRITERIA REQUIREMENTS.

Parameter	Description	Value
$I_{C_{dc},RMS,max}$	Worst-case DC-Link RMS current stress	66.7A
$\Delta Q_{C_{dc},pp,max}$	Worst-case DC-Link peak-to-peak charge ripple stress worst-case	$363\mu F$
$I_{C_{fc},RMS,max}$	Worst-case FC RMS current stress worst-case	103A
$\Delta Q_{C_{fc},pp,max}$	Worst-case FC peak-to-peak charge ripple stress worst-case	$725\mu F$

5.3.3 Heat Dissipation System

In order to dissipate the semiconductor losses, the devices are located on a liquid cooled heat-sink by means of a heat conducting thermal interface material TIM (i.e. the VisIC power switch presents electrically insulated top surface pad). The aim is to limit the junction temperature rising. Fig. 5.10 shows the scheme of the adopted thermal circuit. In particular, T_f is the fluid temperature, T_{hs} is the heat-sink temperature temperature, T_c is the case temperature and T_j is the junction temperature.

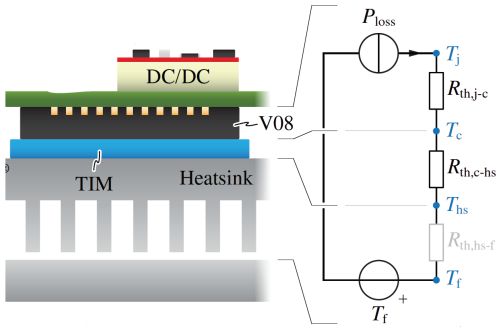


Fig. 5.10 3LFC schematic cross section and related thermal dissipation circuit (i.e. steady-state condition is considered). Considering the hypothesis $T_{hs} \approx T_f$ (i.e. the amount of loss per unit of the heatsink surface are low), $R_{th,hs-f}$ is greyed since it is neglected [140]. The DC/DC label refers to the selected Murata isolated DC/DC auxiliary power supply for the gate drivers (i.e., the higher component in the PCB top face).

The selected TIM is the Tflex HP34 graphite-based 2mm thick by Laird which leads to a case-to-heatsink thermal resistance equal to $R_{th,c-hs} \approx 0.15^oC/W$ (i.e. featuring a thermal conductivity of $\approx 70mm^2 \cdot^o C/W$ at 15 psi). The junction-to-case thermal resistance is $R_{th,c-hs} \approx 0.1^oC/W$ provided by the device manufacturer. In the end, it is assumed that the fluid temperature is close to the heatsink one $T_{hs} \approx T_f$ (i.e. due to the large heatsink surface and low semiconductor losses). Thus the heatsink-to-fluid thermal resistance $R_{th,hs-f}$ can be neglected. The liquid-cooled heatsink is composed by a main body where the liquid channel is dig and a cover both in aluminium as shown in Fig. 5.11. The physical constrains are fixed by the manufacturer in order to limit the cost production. As a matter of fact, it has been decided to produce a first heat-sink to perform the preliminary prototype validation in the laboratory. With this consideration, it results oversized and the temperature fluid is set to $T_f = 40^oC$ (i.e. maximum temperature achieved by the laboratory instrumentation). After these preliminary tests, a second optimized heatsink (i.e. in both volumetric and gravimetric power density) will be designed to operate at a higher fluid temperature more coherent with the motor-sport application ($T_f = 70^oC$). The maximum semiconductor losses are then set to $P_{semi,loss,max} = 1100W$ (i.e. corresponding to a $f_{sw} = 200kHz$) to take some design margin and to enable the maximum possible tests typologies. It is clear that this set-up flexibility and over-sizing requirements will be leaved out in the second design. Some CFD simulation has been performed in Solidworks to check the fluid temperature rise as shown in Fig. 5.12.

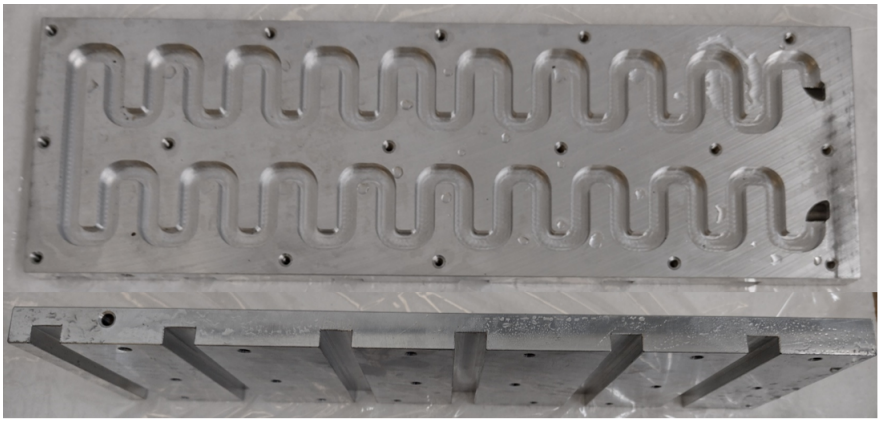


Fig. 5.11 Bottom case of the realized first heatsink prototype where are visible the designed liquid path (top) and the special profile to house the Ceralink capacitors (bottom).

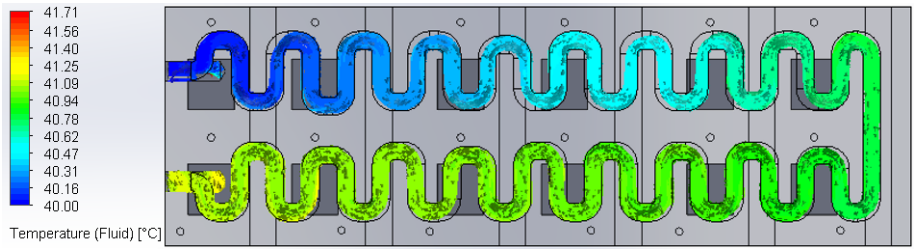


Fig. 5.12 CFD liquid flow simulation of the the realized first heatsink prototype assuming $T_f = 40^oC$, $P_{semi,loss,max} = 1100W$ and $10l/min$ liquid flow rate

Fixed the maximum losses and the thermal resistances, the junction temperature achieved by the power switch is then simulated. The maximum operating junction temperature is set at 125^oC to ensure enough margin (i.e. due to the inaccuracy of the thermal model). Fig. 5.13 shows that $T_{j,max}$ is well below 100^oC, this wide operation margin will be drastically reduced in the second design (i.e. the fluid temperature will be set to 70^oC).

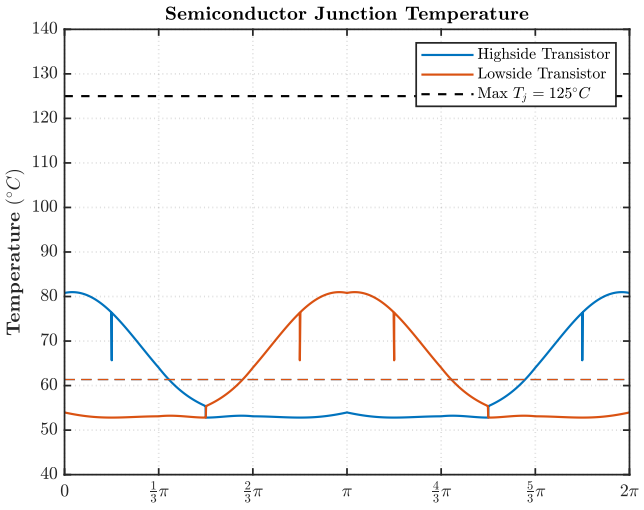


Fig. 5.13 Simulation of the maximum junction temperature ($T_{j,max=81^oC}$) of the semiconductor device considering a fluid temperature of $T_f = 40^oC$.

5.4 Prototype Description

This section aims to describe the realized 800V 100kVA 3LFC three-phase inverter prototype. Fig. 5.14 shows the 3D rendering of the multi-board assembly. In

particular, the inverter is composed by a three-phase power board which is fixed on the heatsink. Then, the inverter driver board (i.e. one for each phase) is located on the top of the power board. A dedicated PCB to measure the DC-Link voltage and the phase currents completes the assembly. Fig. 5.15 shows different views of the board assembly.

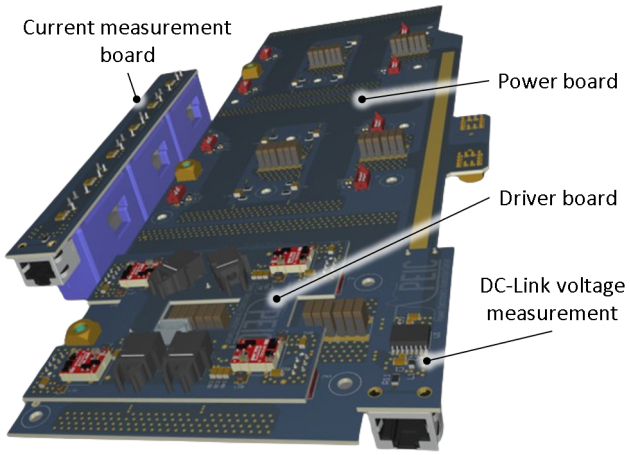


Fig. 5.14 3D rendering of the complete converter multi-board assembly. The power, driver and measurement board are outlined.

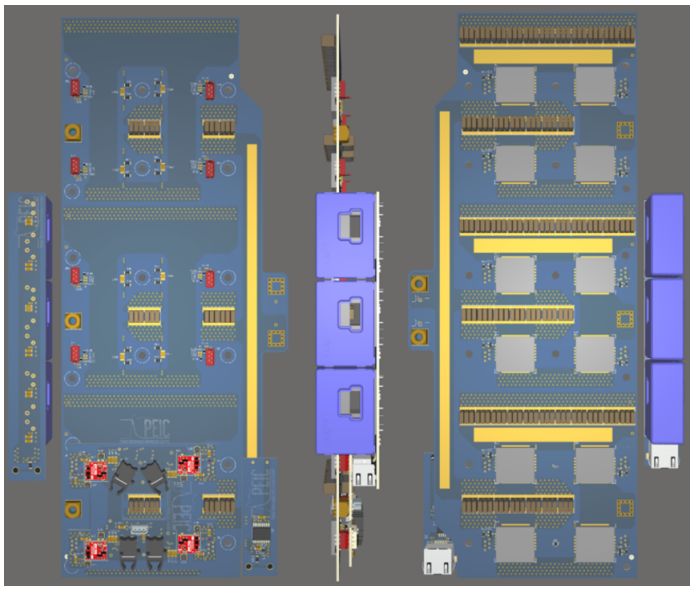


Fig. 5.15 Top, lateral and bottom 3D views of the realized 800V 100kVA 3LFC inverter.

Fig. 5.16 shows the main three-phase power board. It contains the power switches, the DC-Link and flying capacitors. On their face, the PCB is fixed on the heatsink (i.e. it presents a special profile to house the Ceralink capacitor which are

higher than VisIC V08TC65S2A). On the other face, the connectors to place the driver boards (i.e. one for each phase) are located. Fig. 5.17 shows the top and the bottom view of the realized driver boards prototype. It houses the gate drivers, the isolated DCDC power supplies and the optical fibres (i.e. used as receiver for the gate driver signals).

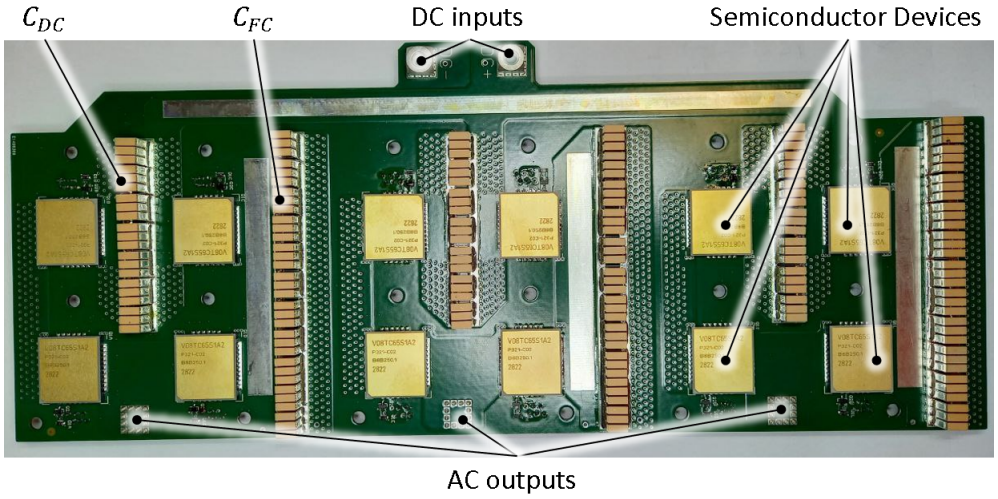


Fig. 5.16 Top overview of the realized main three-phase power boards. Input/output connectors, semiconductor devices, DC-Link and flying capacitors are outlined.

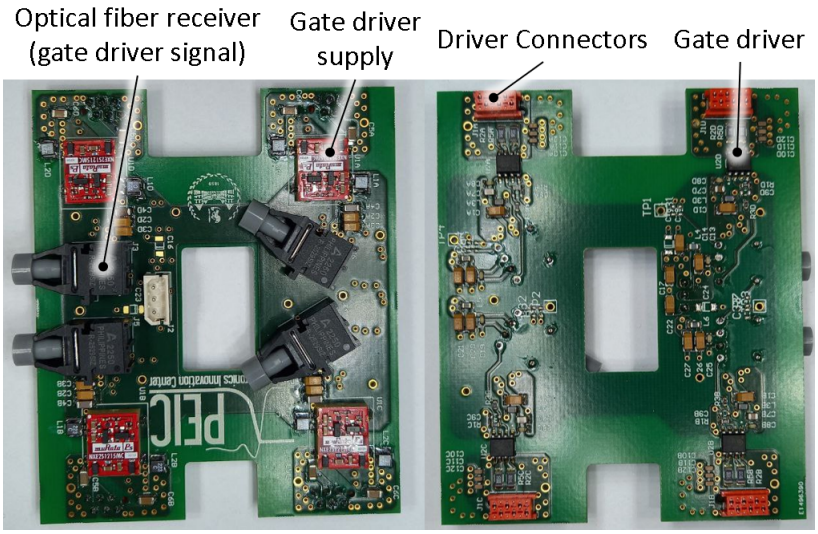


Fig. 5.17 Top (left) and bottom (right) overview of the realized driver boards. Connectors, isolated DCDC power supply, gate driver and optical fibre are outlined.

The converter board assembly dimensions are reported in Fig. 5.18. The total inverter volume results 2.04l. However, the inverter core volume shown in Fig. 5.19

is 1.5l. This volume represents an indication of the minimum volume achievable: the other component can be integrated in a future design. Indeed, in this prototype a modular converter structure is adopted for easiness of debugging.

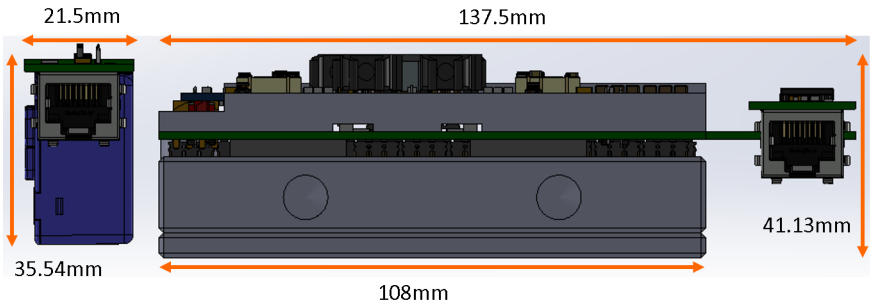


Fig. 5.18 Inverter prototype dimensions. The power board features 338mm depth and the current measurement PCB features 166mm depth.

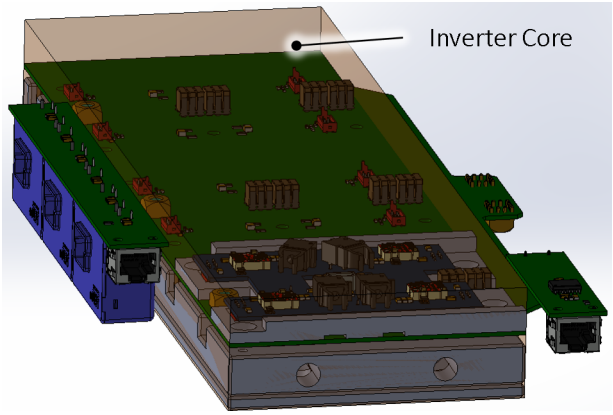


Fig. 5.19 Complete inverter 3D rendering with the inverter core outlined.

The complete inverter and each relevant components weight are specified in Table 5.3. It must be pointed out that the heatsink weight plays an important role on the total amount. It is then crucial to optimize it in the second design.

5.4.1 Commutation Loop

Particular attention has been given to the optimization of the commutation loops which are shown in Fig. 5.20 (a) and (b) respectively for the internal and external 3LFC bridge-leg. It is important to notice that the DC-Link and flying capacitors are integrated in the loop (i.e. no decoupling capacitors are needed). Always with the aim to minimize the commutation loop inductance and thus the semiconductor

Table 5.3 REALIZED 3LFC THREE-PHASE INVERTER PROTOTYPE TOTAL WEIGHT.

Component	Weight [kg]
Power board	0.513
Driver board	0.038x3
Current measurement board	0.140
DC-Link voltage measurement board	0.010
Heatsink	1.705
Plastic support	0.034x3
Total inverter	2.584

over-voltage stress, a vertical loop is then realized exploiting the internal PCB layers as current return path.

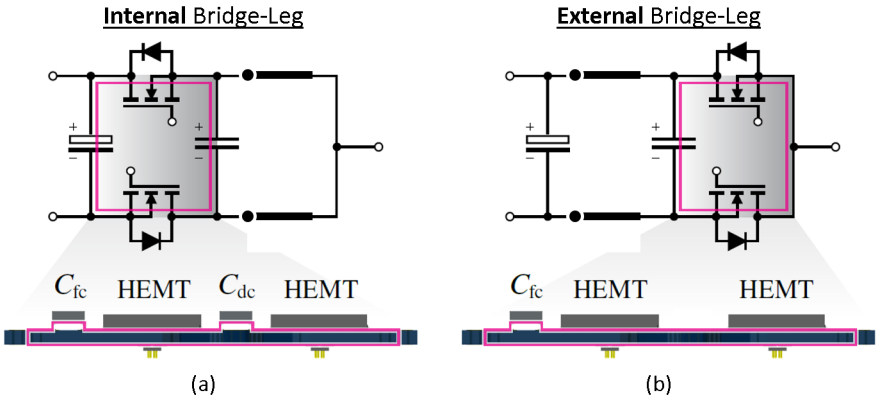


Fig. 5.20 Overview of the vertical commutation loop implemented for the internal (a) and external (b) bridge leg.

5.4.2 Mechanical Consideration

On the single-phase prototype described in the next chapter, it has been noticed that the PCB mounted on the heatsink flexed as shown in Fig. 5.21. This might have caused the board failure in the successive tests due to the excessive mechanical stresses applied on the Ceralink capacitors. In the three-phase converter, some plastic supports to make the PCB more stiff have been designed. Each phase has a dedicated plastic support between the power and the driver board, as shown in Fig. 5.22. Moreover, between the power board and the heatsink, some cylindrical plastic washers have been positioned to guarantee a precise distance.

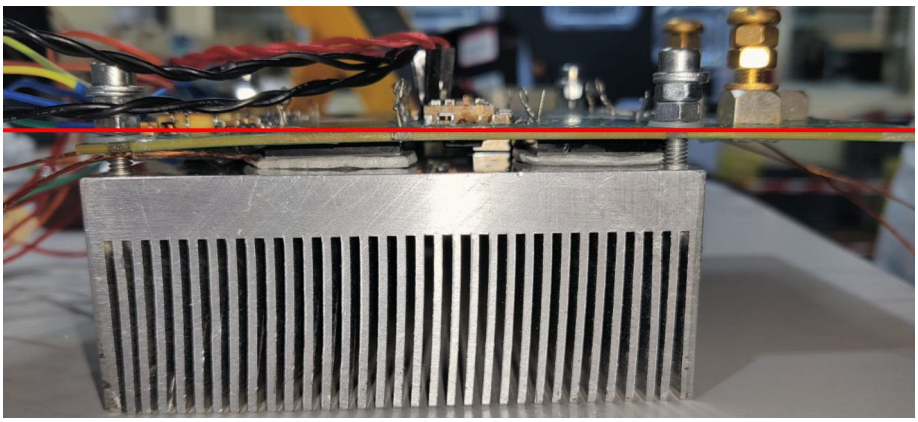


Fig. 5.21 Single-phase 3LFC prototype PCB deformation once mounted on the heatsink.

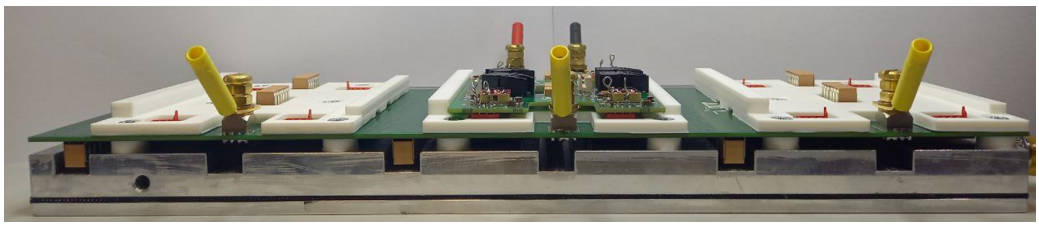


Fig. 5.22 Prototype overview of the realized plastics supports.

5.5 Conclusion

This chapter presents the sizing of an innovative 800V 100 kVA inverter for motor-sport applications. The realized power converter exploits the benefit due to the adoption of the flying capacitor multilevel topology combined with innovative technologies, such as GaN devices and PLZT ceramic capacitors. All these elements are separately analysed in the previous chapters. On the other hand, they present complementary features which can lead to a converter performance enhancement compared to standard two-level SiC/IGBT inverter.

After the presentation of the target inverter specifications, the stresses of the main converter component are analysed. In particular, the phase RMS flux ripple is identified as a performance index to evaluate the PWM-induced losses on the electric motor. From the comparison with a standard two-level inverter, it is demonstrated the superiority of the 3LFC converter in this field (i.e. the motor-sport applications employ high-speed, low inductance motors). Then the DC-Link and flying capacitors stresses are discussed and the design and component selection are presented. Finally, the realized inverter prototype is described focusing on key aspects as the commutation loops and the mechanical assembly.

Chapter 6

Three-Level Flying Capacitor Experimental Validation

6.1 Introduction

This chapter aims to present and analyse all the experimental validations performed on the different realized PCB boards. In particular, a single phase three-level flying capacitor has been firstly built to preliminary test the gate driver configuration and the integration of the GaN devices in the selected multilevel configuration. Thus, several tests have been performed, such as double pulse test, thermal characterization and loss measurements. Then, additional interesting results on the VisIC gate driving circuit are described. In the end, the three-phase prototype designed in the previous chapter has been built and the experimental validation is presented focusing on flying capacitor balancing method and loss measurements.

6.2 Single-phase Three-level Flying Capacitor Converter

A single-phase 3LFC converter has been designed to validate:

- The driving of the VisIC V08 (i.e., tuning of the gate resistance R_g)

- The commutation of the VisIC V08 (i.e., evaluation of voltage overshoot and cross-talk immunity)
- The signal robustness evaluation (i.e., CM noise coupling)

Moreover, a bridge-leg performance evaluation (loss, efficiency, thermal dissipation) is useful to confirm the three-phase design. The realized prototype overview is depicted in Fig. 6.1. The high level of integration can be noticed. Indeed, in the same board the isolated voltage measurement, the current sensors and the gate drivers with the related isolated auxiliary DCDC power supply are included. The experience of the difficulties in the converter debug and experimental tests measurements brought to the multi-board approach design illustrated in the previous chapter for the three-phase converter. Indeed, after the efficiency and structural validation, a second version can be designed optimizing the integration and thus the power density. Due to the preliminary test aims of the single phase board, a forced air cooling system is chosen to limit the cost and complexity.

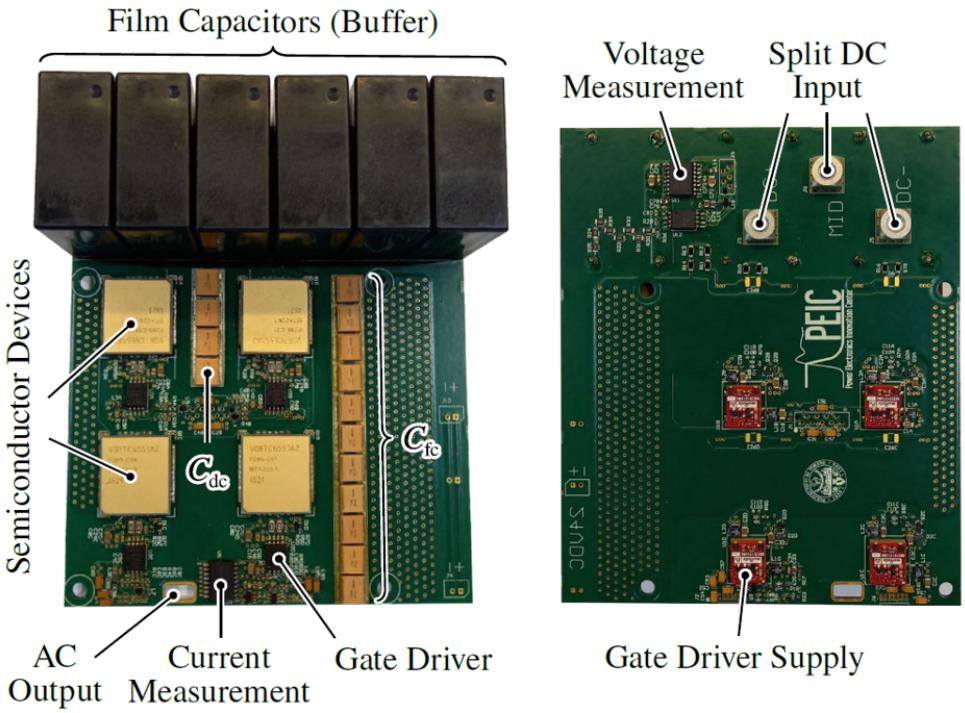


Fig. 6.1 Overview of the realized single-phase 3LFC 800V prototype.

The target specifications are illustrated in Table 6.1. The FC current and charge ripple stresses are calculated similarly as illustrated in the previous chapter. Thus,

eleven j-style CeraLink capacitors rated 500V (B58031U5105M062) are designed to stand a worst-case minimum required RMS current of 72A and a worst-case charge ripple equal to 510 $V\mu F$. Considering the small-signal capacitance of $0.6\mu F$, the maximum voltage ripple on the flying capacitors results 77V. It must be noticed that the low package dimensions and the consequent low equivalent series inductance allow an high integration level in the PCB board. Indeed, they are located near the devices taking part in the power commutation loop and eliminating the need of the decoupling capacitors. On the other hand, since the DC-Link sizing capacitance requirement is noticeable higher for a single phase converter compared to a three-phase one, only a reduced DC-Link capacitance is located on the board. External capacitors will satisfy the overall requirements. On the board, four decoupling capacitors (i.e. Ceralink j-style 900V 0.13uF B58031U9254M062) are placed for the internal leg. It can be pointed out that the power commutation loop will be very similar to the three-phase case as illustrated in Fig. 5.20 Additional Film capacitor are then placed to give a bulk capacitance directly on the PCB.

Table 6.1 SINGLE-PHASE THREE-LEVEL FC INVERTER PROTOTYPE SPECIFICATIONS

Parameter	**Description**	**Value**
I	Peak Phase Current	100A
V_{dc}	DC-Link Voltage	800V
f_{sw}	Switching frequency	100 kHz

6.2.1 Double Pulse Tests (DPT)

Double pulse tests have been initially performed to verify the gate driver design and the commutation of the selected VisIC devices. The two legs are then tested individually, operating them as two independent half-bridge legs. Fig. 6.2 shows the commutations of the external leg at no load (i.e. in zero current switching ZCS condition). Fig. 6.3 illustrates the device gate voltage and the drain-to-source voltages commutate until 200A (i.e. maximum current rating of the device). Finally, Fig. 6.4 shows a zoom of the commutation related to 200A to better visualize the overshoot and the high frequencies ringing. All these tests have been performed for both internal and external legs. During these tests, the dead-time has been set at 100ns. The maximum measured voltage derivative is $\approx 60V/ns$ (i.e. considering 1Ω as ON gate resistance and 0Ω as OFF gate resistance).

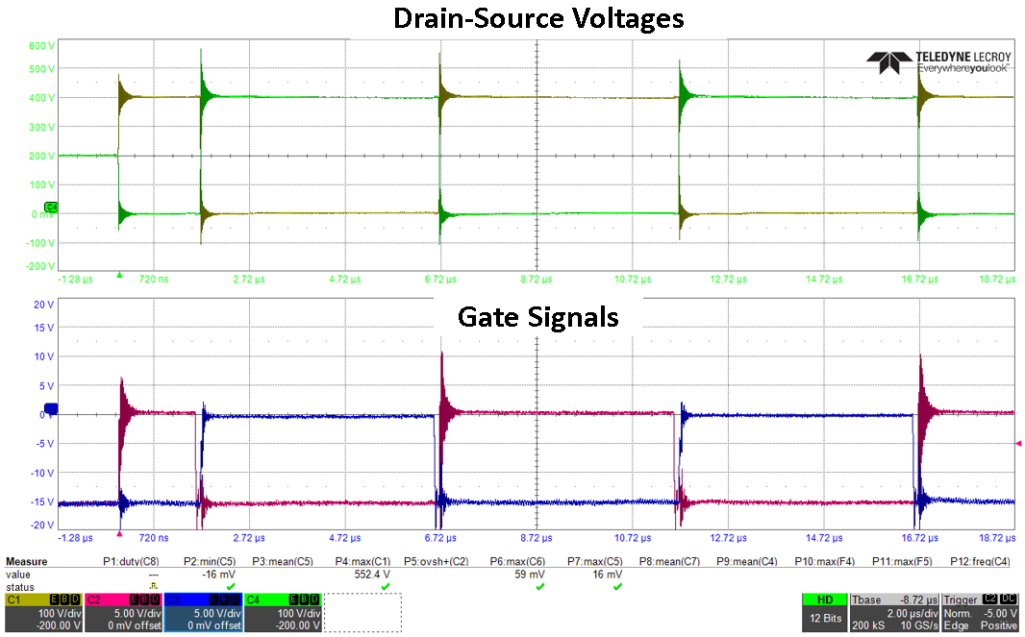


Fig. 6.2 Drain-to-source (up) and gate-to-source (down) voltages commutated at no load for the external leg of the realized single phase 3LFC prototype.

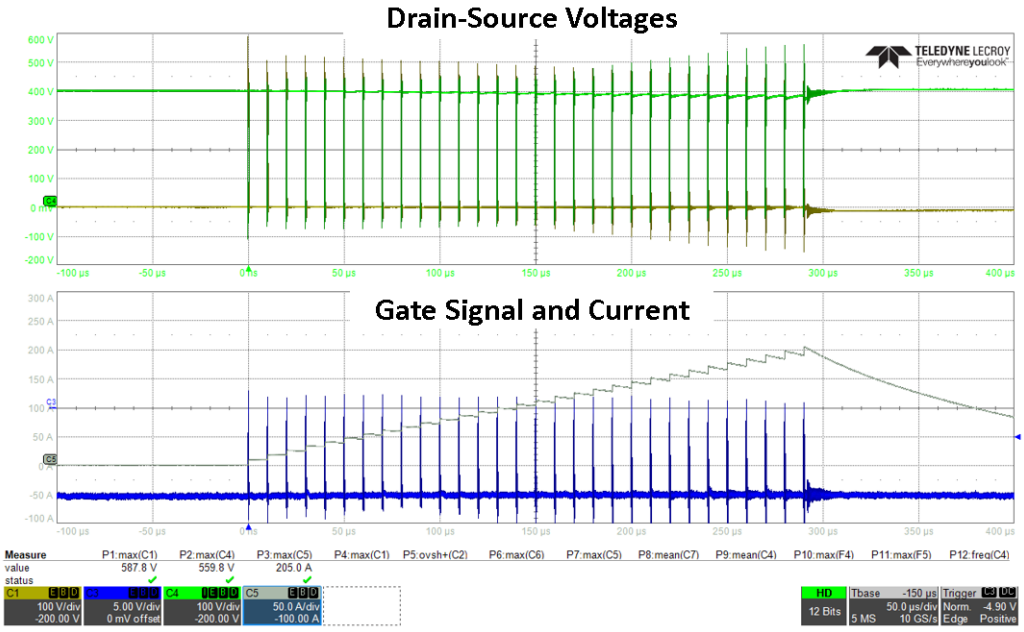


Fig. 6.3 Drain-to-source voltages (up), gate-to-source voltage and commutated current (down) until 200A for the external leg of the realized single phase 3LFC prototype.

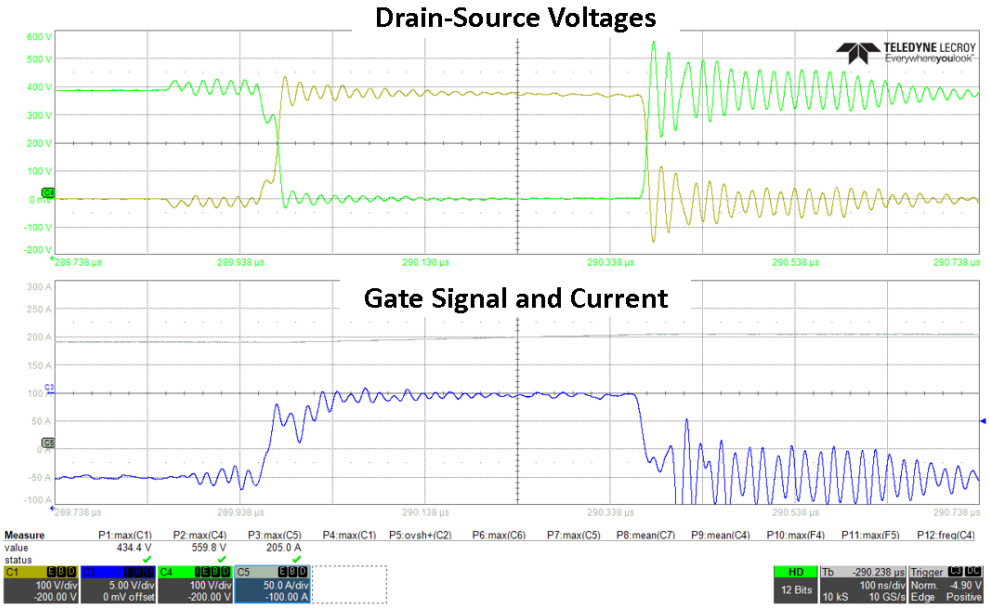


Fig. 6.4 Zoom of the drain-to-source voltages (up), gate-to-source voltage and commutated current (down) at 200A for the external leg of the realized single phase 3LFC prototype.

6.2.2 Thermal Characterization

As stated before, in order to limit the cost and the overall converter complexity, a forced-air cooling system has been designed to dissipate the semiconductor losses. Its structure is shown in Fig. 6.5 along with its thermal dissipation circuit. In particular, T_a is the ambient temperature, T_{hs} is the heatsink temperature, T_c is the gate temperature and T_j is the junction temperature. The selected thermal interface material TIM feature 2mm of thickness (i.e. it is the Tflex HP34 graphite-based by Laird as in the three-phase converter). This allows the Ceralink to be properly spaced from the heatsink. The selected fan is 04020VA-24P-AA-00 featuring 40mm×40mm×20mm dimensions and the heatsink is the Meccal PM+ series (i.e 100mm×100mm×40mm).

Limiting the heatsink temperature to 70^oC in order to not heat up the surrounding converter elements and the maximum ambient temperature to 30^oC (i.e. adapted to the laboratory conditions), the maximum allowed heatsink-to-ambient thermal resistance results:

$$R_{th,max} = \frac{T_{hs,max} - T_{amb}}{P_{loss,tot}} = \frac{70^oC - 30^oC}{236.8W} \cong 0.168\frac{K}{W} \tag{6.1}$$

where the maximum simulated losses $P_{loss,tot}$ are equal to 236.8W. Supposing an air flow 40 m^3/h the designed $R_{th,hs-a}$ is $\approx 0.15K/W$ for the chosen hestsink. Similar considerations as the three-phase converter have been done for the other thermal resistances.

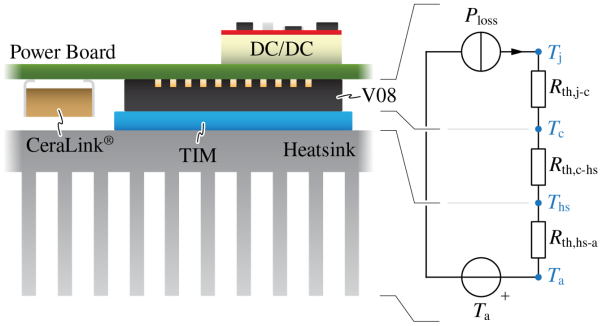


Fig. 6.5 3LFC single phase schematic cross section and related thermal dissipation circuit (i.e. steady-state condition is considered). The DC/DC label refers to the selected Murata isolated DC/DC auxiliary power supply for the gate drivers (i.e., the higher component in the PCB top face).

The performed thermal tests are divided into two separate experiments, which are the device electrical resistance and system thermal resistance characterization. The first test is performed without the heatsink, aiming to achieve the thermal characterization of the device on-state electrical resistance (i.e. measuring current, voltage and temperature). The experimental set-up is shown in Fig. 6.7, where the thermocouple on the devices is highlighted. Fig. 6.6 shows the experimental results. It can be noticed that PCB soldering increases the total device resistance compared to the component datasheet. The devices show little parametric deviation.

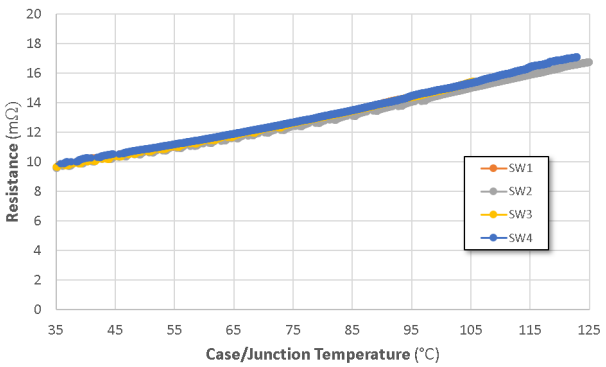


Fig. 6.6 Experimental results of the device on-state electrical resistance thermal characterization.

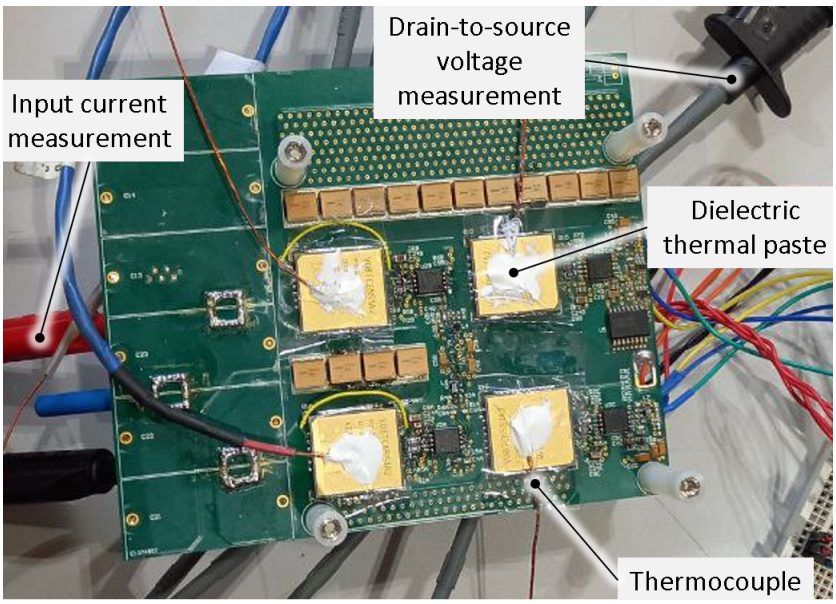


Fig. 6.7 Single phase 3LFC experimental set-up for the thermal characterization of the device on-state electrical resistance.

The second test experimental set-up is shown in Fig. 6.8 and Fig. 5.22, where the single phase 3LFC board is mounted on the heatsink. As said before, with the insertion of the selected gap filler thermal interface material TIM, the total height of device plus the TIM becomes larger than the capacitor one. These thermal tests are performed turning ON all the devices and limiting the dispensed dissipated power through the supply voltage instruments. The board has been tested up to 200W of dissipated power, the experimental measurements in this last case are shown in Fig. 6.9. Considering an ambient temperature of $T_a = 27^oC$, the thermal resistances resulting from thermal tests are:

$$R_{th,c-hs} \approx 0.15 \div 0.20^oC/W \tag{6.2}$$

$$R_{th,hs-a} \approx 0.22^oC/W \tag{6.3}$$

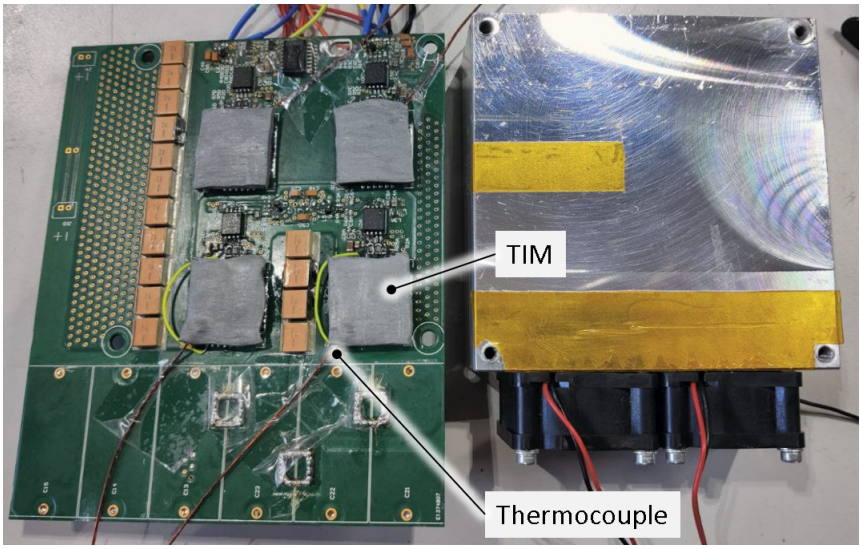


Fig. 6.8 Single phase 3LFC experimental set-up for system thermal resistance characterization.

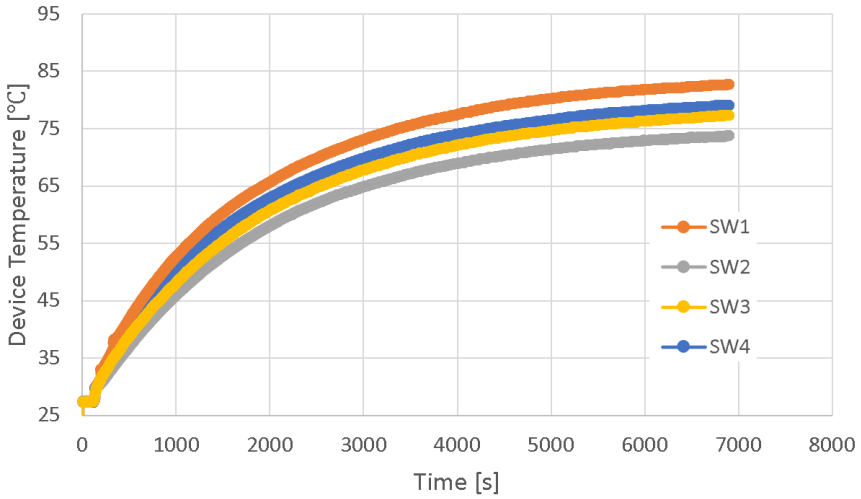


Fig. 6.9 Measured devices temperature rise with 200W dissipated.

6.2.3 Loss and Efficiency

In this section the electrical characterizations of the single phase 3LFC board are shown. Differently from the DPT tests, the board does not operate the two legs separately in two level mode (i.e. maximum of 400 DC-Link voltage). Thus, the following experimental results are obtained operating the two legs simultaneously as expected for the three-level flying capacitor converter (i.e. maximum of 800

DC-Link voltage). Fig. 6.10 shows the experimental measurements of the drain-to-source voltages of both internal and external legs at no load condition. Fig. 6.11 and Fig. 6.12 illustrate the same waveforms in a DPT test at the design current. These impulsive tests are essential to check the commutations of the devices (i.e. over-voltages stress, the voltage derivatives and so on...) and the normal operation of the control signals.

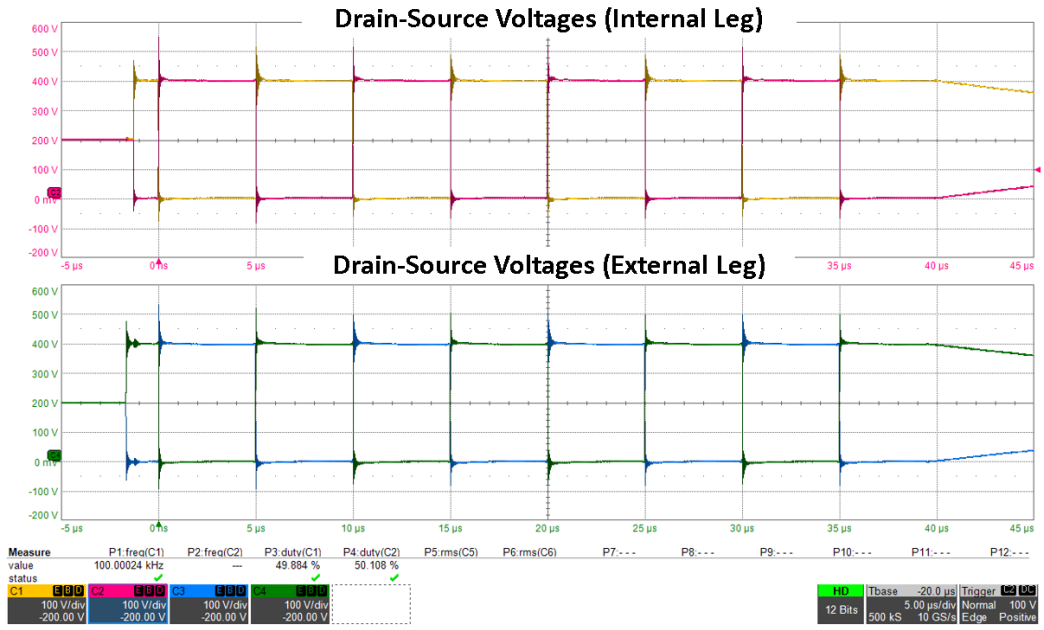


Fig. 6.10 Single phase 3LFC prototype drain-to-source voltages for the internal (up) and external (down) legs operating at no load and 800 of DC-Link voltage.

Fig. 6.13 and Fig. 6.14 show the legs measured drain-to-source and the output current (i.e. measured with two different probes) for the converter buck modes operation. Due to the components over-sizing, it has been possible to test the converter beyond the design targets (i.e. until 100A continuous). Summarizing, with the HBM measurement system and data recording instrument, the system losses with a 40 ms test for different values of DC-Link voltage (i.e. from 200V to 800V) and output current (i.e. $10 \div 100A$) has been measured. These results are reported in Fig. 6.15. The reported losses are higher compared to the calculated semiconductor losses due the several additional resistance due to wires and connections and the losses on the capacitors. For example, at 800V and 60A the measured losses are $\approx 270W$ and the estimated semiconductor losses are $\approx 128W$. No additional tests have been performed because, while the last tests were running to measure the system loss on

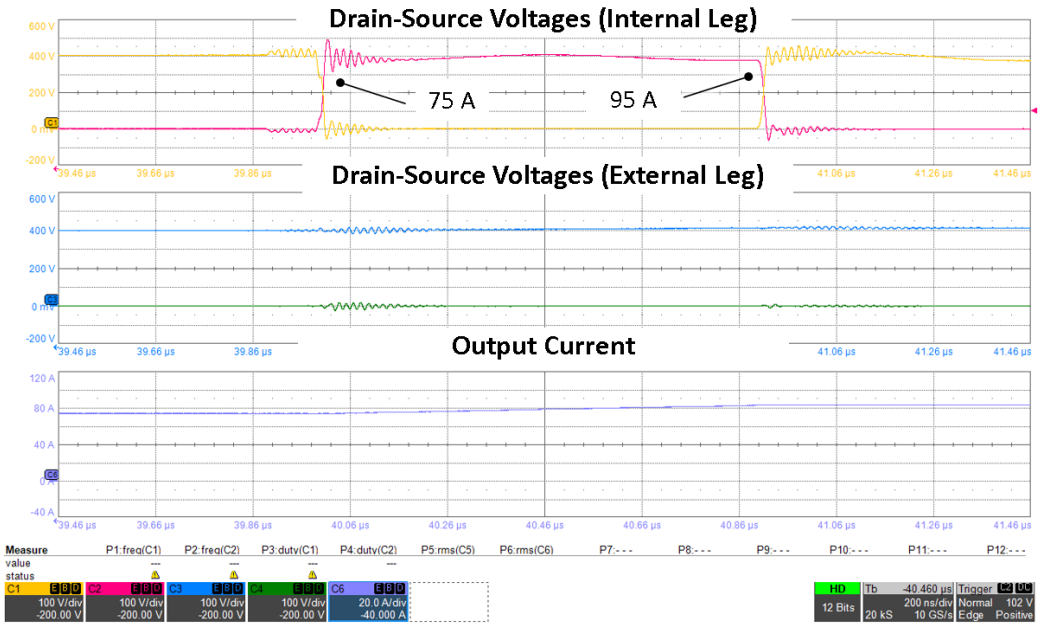


Fig. 6.11 Single phase 3LFC prototype drain-to-source voltages enlargement for the internal (up) and external (mid) legs operating at 800 of DC-Link voltage. The output current ($\approx 100A$) is reported on the bottom diagram.

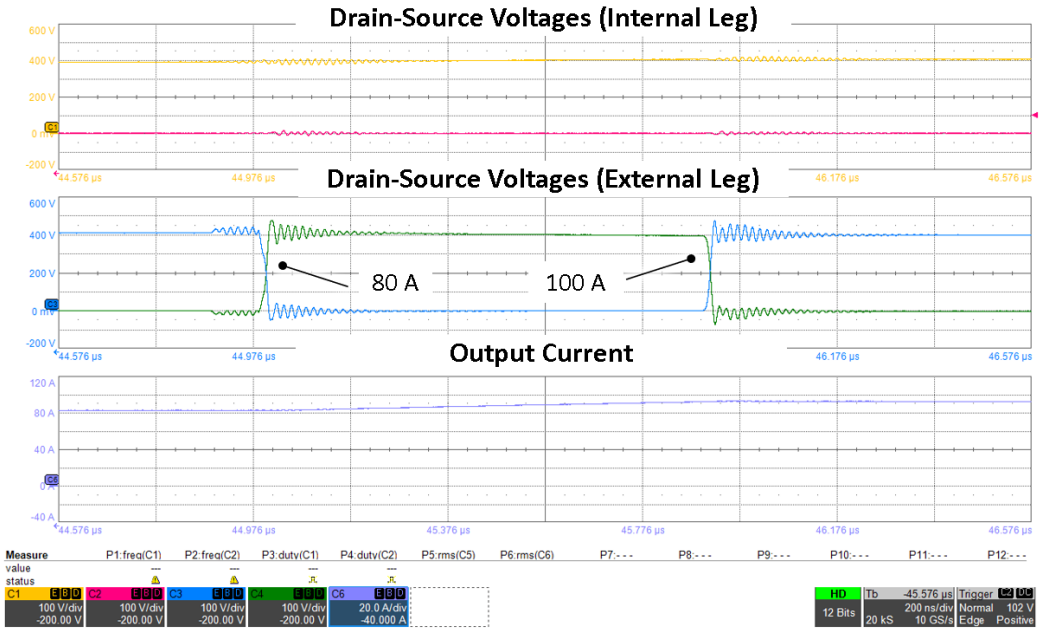


Fig. 6.12 Single phase 3LFC prototype drain-to-source voltages enlargement for the internal (up) and external (mid) legs operating at 800 of DC-Link voltage. The output current ($\approx 100A$) is reported on the bottom diagram.

buck mode, the converter had a catastrophic failure at 800 V 80 A. It is difficult to state the exact cause of the failure. The main reason of the failure could be:

- Ceralink crack propagation due to a non professional soldering;
- Limitation of the power switch device that was guaranteed only for DPT test (we performed several long (i.e. 40 ms) test at high current (i.e. until 100 A) and high voltage (i.e. 800 V)).

This last test is reported in Fig. 6.16 and Fig. 6.17. Since the PCB could not be recovered (i.e. there is an high cost to build a second prototype), it has been decided to move to the three-phase prototype due to the high costs.

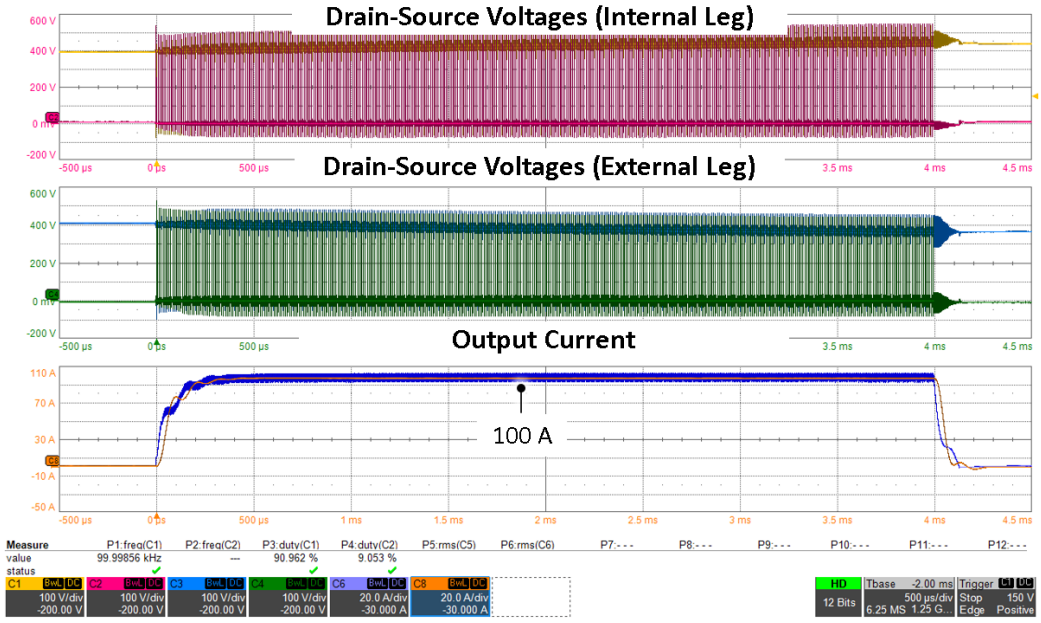


Fig. 6.13 Single phase 3LFC prototype drain-to-source voltages for the internal (up) and external (mid) legs in continuous operating buck mode at 800 of DC-Link voltage. The output current ($\approx 100A$) is reported on the bottom diagram.

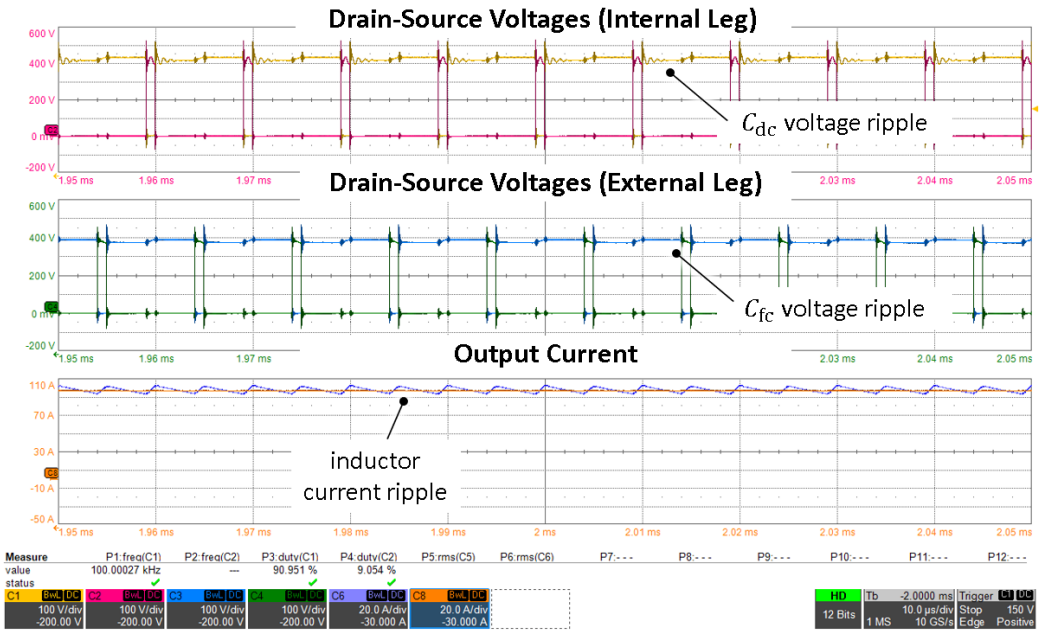


Fig. 6.14 Single phase 3LFC prototype drain-to-source voltages enlargement for the internal (up) and external (mid) legs in continuous operating buck mode at 800 of DC-Link voltage. The output current ($\approx 100A$) is reported on the bottom diagram.

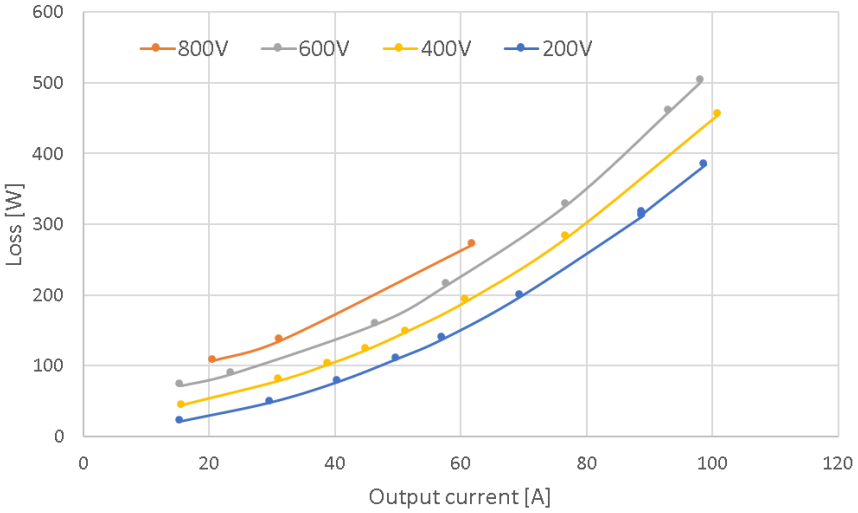


Fig. 6.15 HBM measured system losses with a 40 ms tests in buck mode operation for different values of DC-Link voltages and output currents.

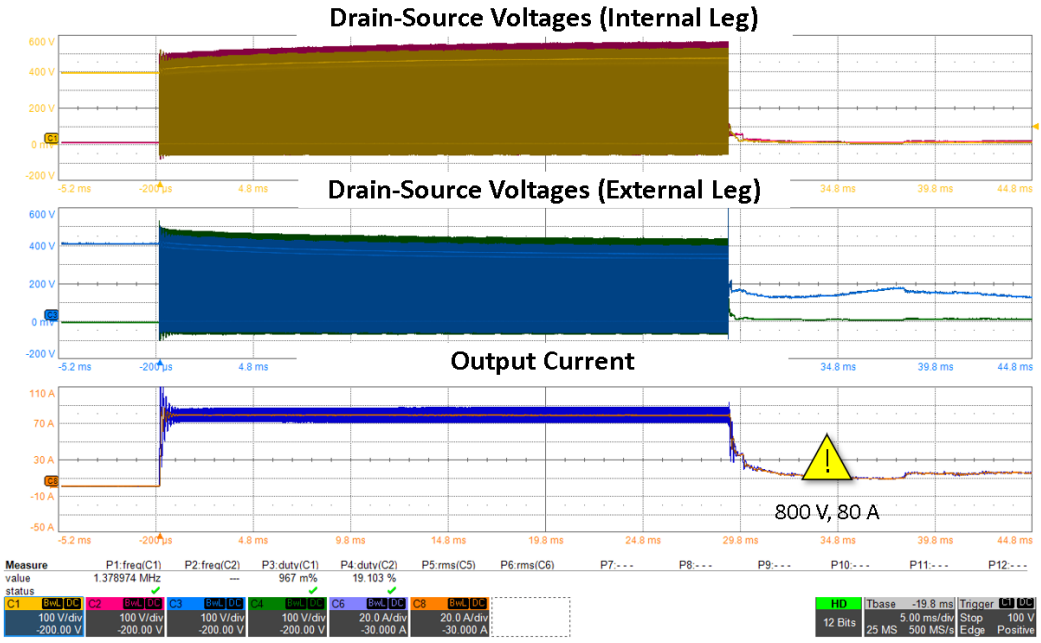


Fig. 6.16 Single phase 3LFC prototype drain-to-source voltages for the internal (up) and external (mid) legs in continuous operating buck mode at 800 of DC-Link voltage during a failure event. The output current ($\approx 80A$) is reported on the bottom diagram.

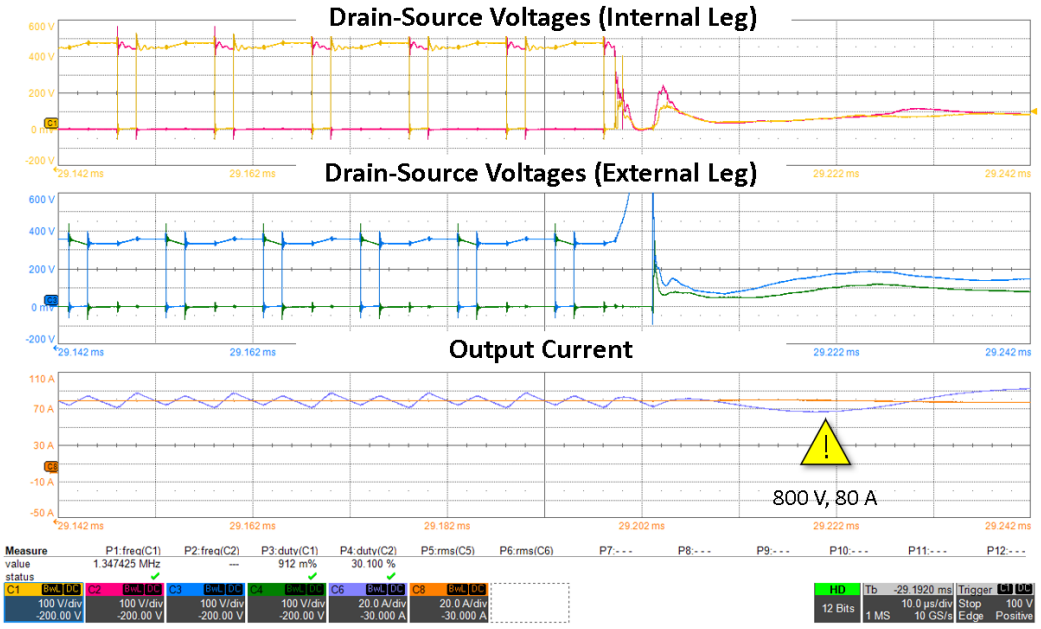


Fig. 6.17 Single phase 3LFC prototype drain-to-source voltages enlargement for the internal (up) and external (mid) legs in continuous operating buck mode at 800 of DC-Link voltage during a failure event. The output current ($\approx 80A$) is reported on the bottom diagram.

6.3 Additional Gate Driver Tests

At the beginning of the single phase 3LFC prototype tests, it has been noticed that the internal bridge-leg achieved a very slow drain-to-source dv/dt and the relative gate driver signals seemed to rise slower (i.e. when voltage is applied) than in the external bridge-leg. Fig. 6.18 shows the comparison between the internal and external legs measured voltages at no load condition. In particular the drain-to-source voltage transition is about 4 times slower. Moreover, Fig. 6.19 shows the same waveform with a commutated current. The internal leg gate signals present a very atypical behaviour which presents a noticeable voltage drop as the current increases. To sum up, the driver circuits in the two bridge-legs are practically identical, the gate driving resistances are the same and the driver loop seems to be influenced by the power loop during voltage transitions. On the other hand, the devices of the internal leg are driven on the opposite side of the package with respect to the external bridge-leg. This raised the doubt that the package was not completely symmetrical as assured initially and thus further investigations were needed.

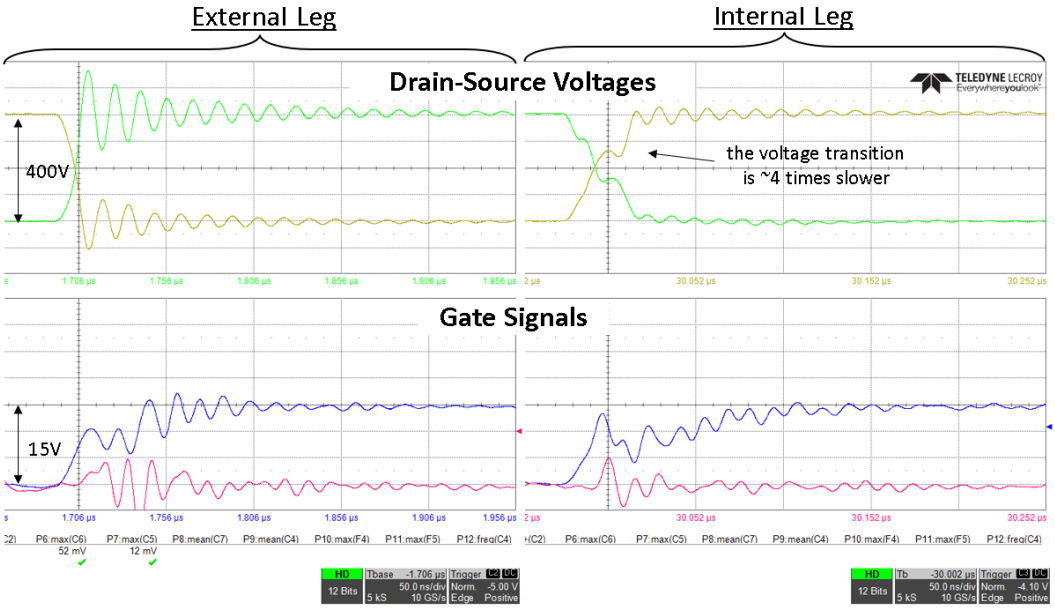


Fig. 6.18 Zoom comparison of the drain-to-source (up) and gate-to-source (down) voltages commutated at no load for the external (left) and internal (right) leg of the realized single phase 3LFC prototype.

To properly address the outlined problem, a new board has been designed. Its main goals are to test the driving circuit for each side of the device and verify if there

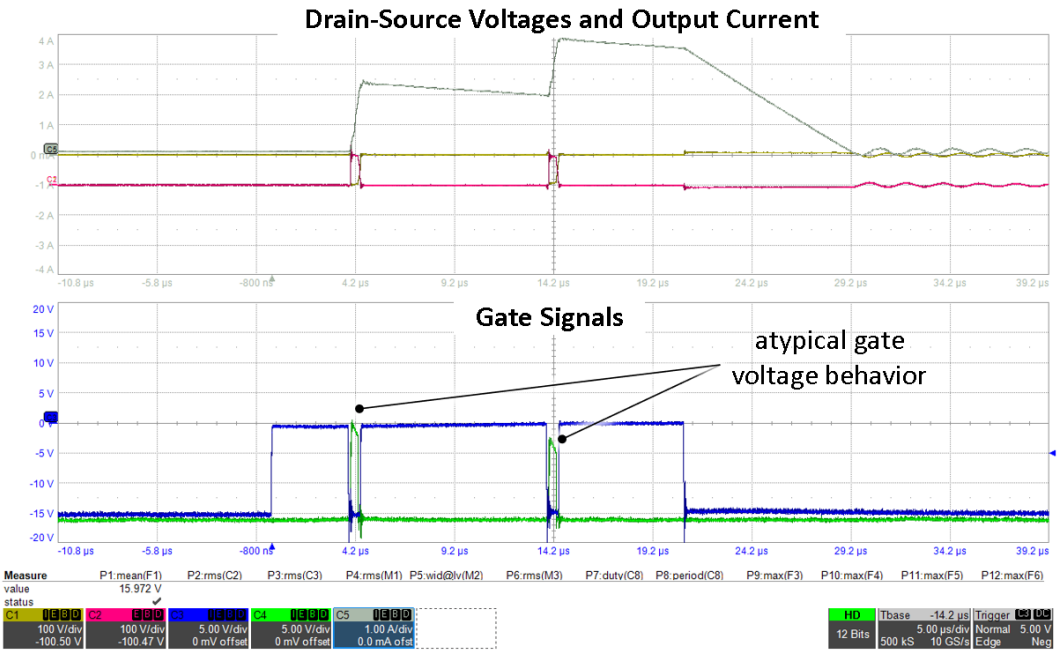


Fig. 6.19 Output current (up), drain-to-source (up) and gate-to-source (down) voltages commutated at 4A for the internal leg of the realized single phase 3LFC prototype.

is any difference in short-circuiting the device pins. Fig. 6.20 shows the realized prototype overview. It features a two-level configuration without any voltage and current measurements. Moreover, it has the possibility to test the driving circuits for the device paralleling. At the time of writing, these tests are not performed yet and thus it represents an interesting future research topic.

The test results performed on the new described board confirmed the hypothesis of asymmetrical internal gate driving circuit, as shown in Fig. 6.21. Unfortunately, the floating enable pin of the internal bridge-leg of the 3LFCC still allowed the device to turn-on and turn-off (i.e., through capacitive coupling), therefore the problem went unnoticed in a first moment. In retrospective, this was the cause of switching waveform asymmetry between internal and external bridge-legs and voltage unbalance of the 3LFCC. The connection between the two enable pins is not part of the gate loop and can thus be obtained with a slim trace.

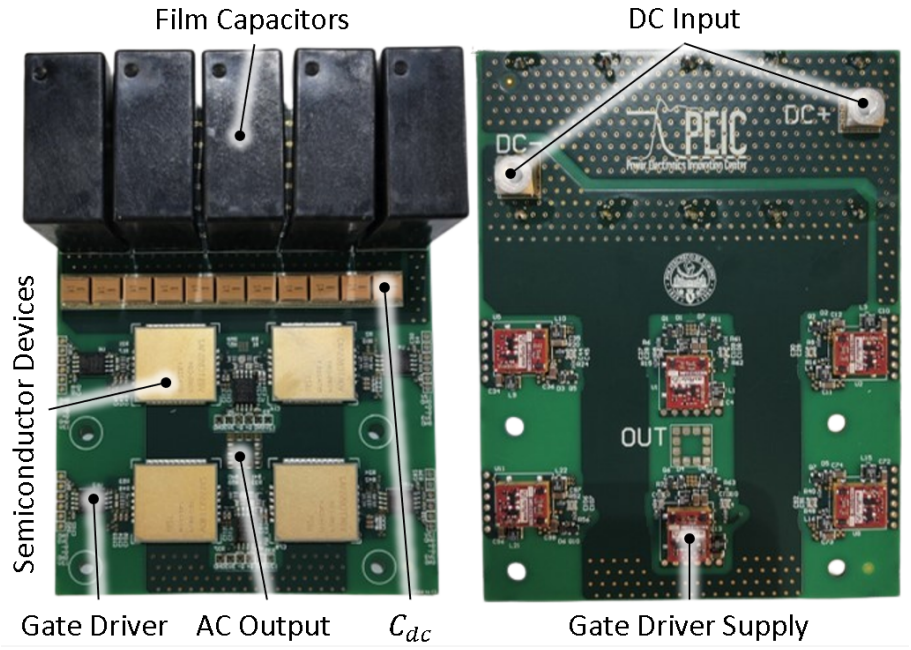


Fig. 6.20 Overview of the single-phase two-level 400V bridge-leg prototype realized to investigate the gate driving circuits.

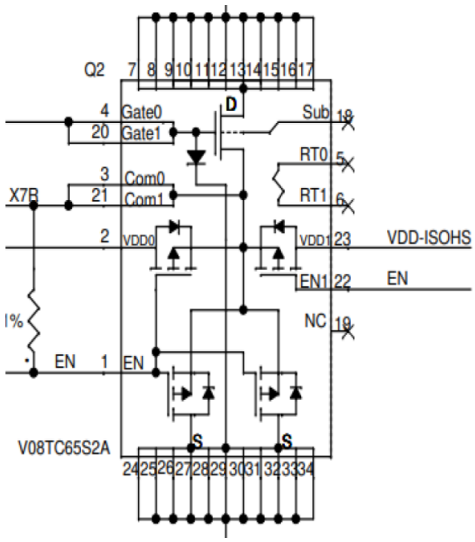


Fig. 6.21 Schematic of the VisIC V08TC65S2A device where it is visible that the two enable pin present different internal connection [98].

6.4 Three-Phase Three-level Flying Capacitor Converter

This section aims to present the experimental validations of the three-phase three-level flying capacitor converter designed in the previous chapter and shown in Fig. 5.22. Firstly, DPT tests have performed in order to check the driver signals and the commutation overshoot. Thus, the two bridge-leg have been tested individually due to their different structure up to 200A, 400V (i.e. in two-level operating mode). Identical tests have been performed for all the phases, similar results have been obtained in terms of dV/dt and commutation behaviour. Slower commutation derivatives compared with the single phase board prototype have been detected (i.e. maximum measured value from 60 V/ns to 40 V/ns). This is mainly due to different gate commutation loops.
The realized control architecture is shown in Fig. 6.22. It features a dSpace (rapid prototyping system) which generates the switching functions and acquire all the cur measurements. Between the control unit and the converter, an interface board has been developed. The gate signals are reported at the inverter through optical fibres.

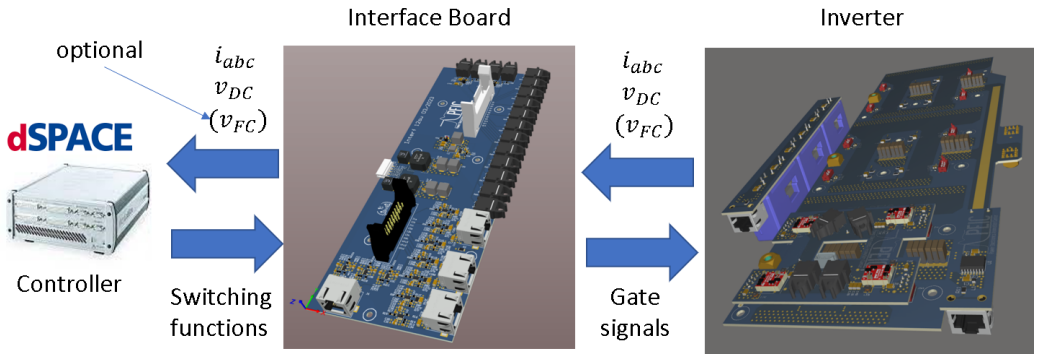


Fig. 6.22 Schematic of the realized test set-up architecture featuring dSpace as control unit, an interface board and the inverter prototype.

The DC-Link voltage and Fling Capacitors (i.e. not mandatory for the converter operation) voltages and output phase currents measurement boards have been tested at full-scale. All the dSpace acquisitions have been tested separately. At the time of writing, the converter has been tested in current closed-loop control configuration to test the dSpace firmware, the current and voltages sensors in steady state converter operation and the overall experimental set-up communication and robustness. These tests have been performed with an RL load (i.e. 300 µH three-phase inductors and

2 Ω three-phase resistors) up to 300 DC-Link voltage and 20A output phase peak current. However, since a precautionary approach is adopted, the converter is firstly tested at the full DC-Link voltage and current in open loop on a pure inductive load. This is the set-up shown in Fig. 6.23, where the dSpace control unit, the converter and the chiller are outlined.

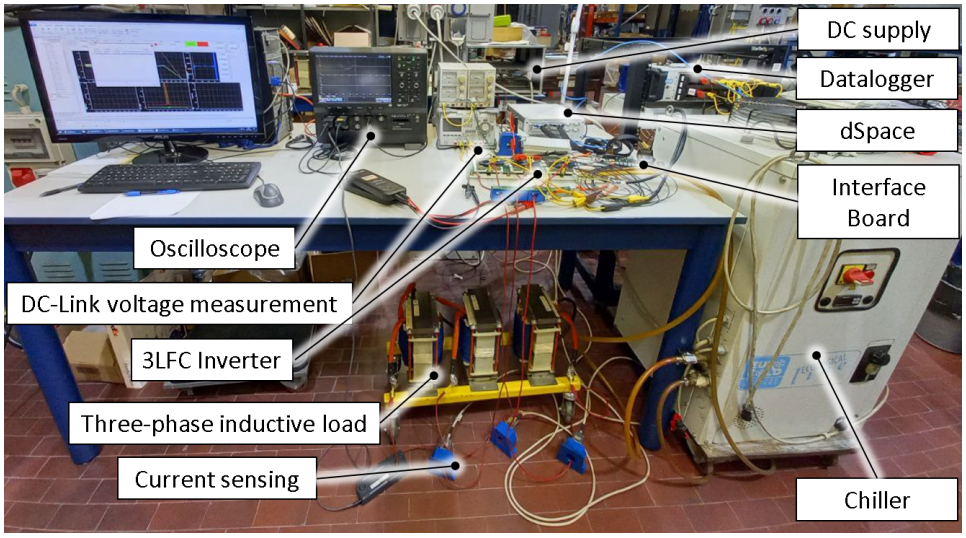


Fig. 6.23 Realized experimental set-up to test three-phase three-level flying capacitor converter at full DC-Link voltage and current in open loop control on a three-phase inductors.

6.4.1 Flying Capacitor Balance Mechanism

As explained before, the flying capacitor balance is essentially for the converter operation (i.e. in both transient and steady state operating condition). Indeed, it assures that the voltage commutated by the switch does not exceed the power device ratings. Although it is ensured by the phase-shift PWM technique, here it is proven that the output capacitance of the switch C_{oss} has a not negligible effect on the FC balancing [214]. This effect is clearly visible in Fig. 6.24, which shows the dSpace acquisition of the measured FC voltages for two phases of the realized three-phase 3LFC inverter prototype in a open loop test. It is possible to observe the acquisitions from 200 to 500 DC-Link voltage cases. The phase b (left diagram) FC voltage value is generally closed the the $V_{dc}/2$ compared to phase c (right diagram), which achieves a steady-state FC voltage value of 220V for $V_{dc} = 500V$ and thus presents $\approx 30V$ discrepancy from theory. If a linear voltage dependence is hypothesised, it

results a not negligible 50V unbalance voltage at $V_{dc} = 800V$ that could cause a potentially device disruptive over-voltage.

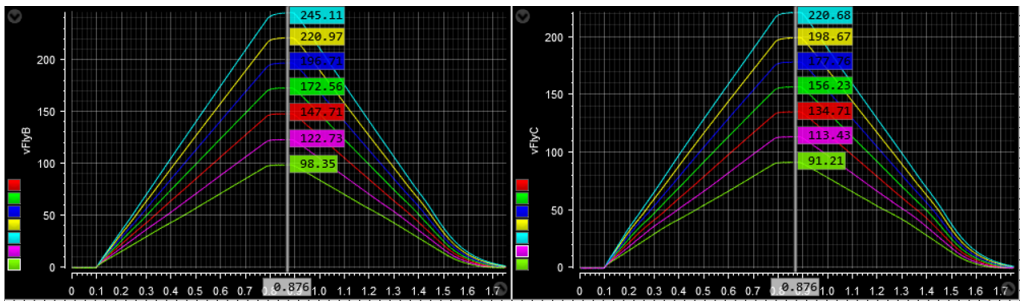


Fig. 6.24 dSpace acquisition of the measured FC voltages of phase b (left plot) and of phase c (right plot).

Taking into consideration the notation of Fig, 3.18, in the flying capacitors converter S_1 and S_4 block $V_{dc} - V_{fc}$ and S_2 and S_3 block V_{fc}. Considering a constant value associated to the devices, the output parasitic capacitance results:

$$Q_{oss}(V_{dc} - V_{fc}) = C_{oss}V_{dc} - C_{oss}V_{fc} \tag{6.4}$$

$$Q_{oss}V_{fc} = C_{oss}V_{fc} \tag{6.5}$$

During one switching period the net charge transferred to the flying capacitor results:

$$dQ_{fc} = 2C_{oss}(V_{dc} - 2V_{fc}) \tag{6.6}$$

The evolution in time domain results:

$$C_{fc}\frac{dV_{fc}(t)}{dt} = -4f_{sw}C_{oss}V_{fc}(t) + 2f_{sw}C_{oss}V_{dc} \tag{6.7}$$

Therefore, in Laplace domain:

$$V_{fc}(s) = \frac{1}{1 - s\dfrac{C_{fc}}{4f_{sw}C_{oss}}}\frac{V_{dc}}{2} \tag{6.8}$$

The time constant of the C_{oss}-related balancing mechanism is $\tau = C_{fc}/(4 f_{sw} C_{oss})$. For the realized three-phase 3LFC inverter prototype, it is equal to 47.2ms, as confirmed in the PLECS simulation result shown in Fig. 6.25.

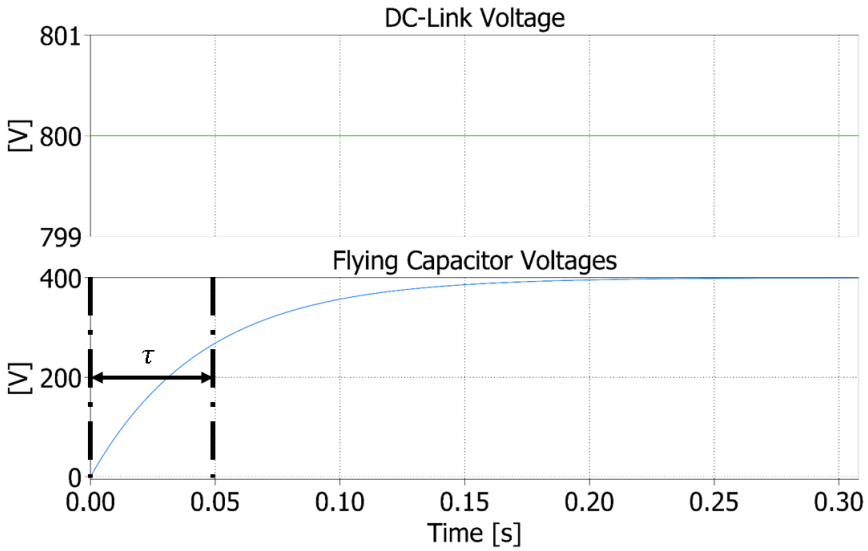


Fig. 6.25 PLECS simulation of the C_{oss}-related balancing mechanism time constant for the realized three-phase 3LFC inverter prototype.

The steady state conditions are achieved once that the net amount of charge transferred to C_{oss} is zero:

$$Q_{oss,S1}(V_{dc} - V_{fc}) + Q_{oss,S4}(V_{dc} - V_{fc}) = Q_{oss,S2}(V_{fc}) - Q_{oss,S2}(V_{fc}) \tag{6.9}$$

$$(C_{oss,S1} + C_{oss,S4})(V_{dc} - V_{fc}) = (C_{oss,S2} + C_{oss,S3})V_{fc} \tag{6.10}$$

Assuming that:

- $C_{oss,S1} = C_{oss,S4} = (1-x)C_{oss}$;
- $C_{oss,S2} = C_{oss,S3} = C_{oss}$.

It results that:

$$V_{fc} = \frac{1-x}{2-x} V_{dc} \tag{6.11}$$

If there is a C_{oss} mismatch x between the inner and the outer bridge-leg, there will be a consequent steady state unbalance. Thus, the device parameter tolerance must be taken into account in the balance mechanism. Fig. 6.26 shows the PLECS simulation results of the realized 3LFC converter shows the FC voltages behaviour for a C_{oss} unbalance (20% decrement for the internal leg) considering $V_{dc} = 800V$ and the phase peak current of 20A.

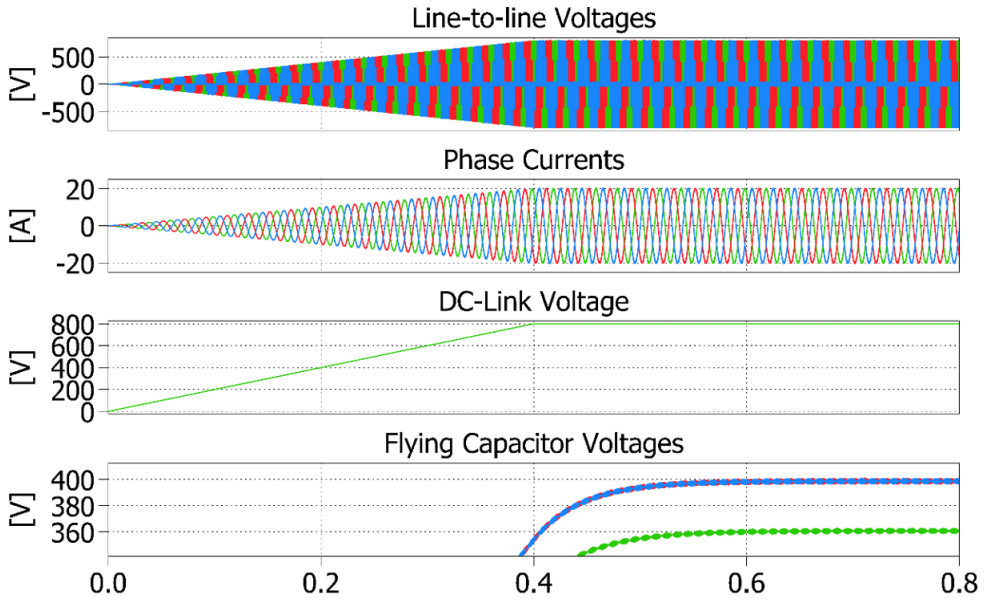


Fig. 6.26 PLECS simulation of the realized three-phase 3LFC inverter. Considering $V_{dc} = 800V$, the output peak phase current of 20A and a 20 % decrement for the internal leg C_{oss}, it can be observed the FC voltages unbalanced behaviour.

To sum up, a FC voltage unbalance has been observed for only one of the three phases of the 3LFC converter. With an additional capacitance in parallel to the internal leg devices, we noticed an improvement according to the presented simulation and theory. Fig. 6.27 (a) shows the experimental results with the addition of 100pF. As illustrated, the converter has been tested until $V_{dc} = 600V$. If a linear voltage dependence is hypothesised as shown in Fig. 6.27 (b), it results a 32 voltage drift at $V_{dc} = 800V$, which is still potentially over-voltage disruptive. Fig. 6.28 (a) shows the experimental results for the addition of 200pF capacitance, in this condition the converter has been tested until $V_{dc} = 800V$ showing a 18V FC unbalance. Since it has been considered a non-critical value (i.e. considered the device measured over-voltage), the additional capacitance is not further increased.

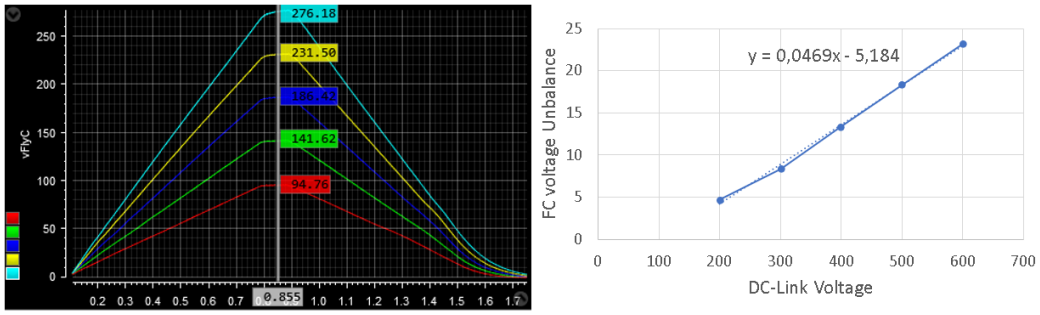


Fig. 6.27 (a) dSpace acquisition of the measured FC voltages of phase c with an additional 100pF capacitance in parallel to the internal leg devices and (b) linear dependence of the FC voltage unbalance which lead to a 32V drift at $V_{dc} = 800V$.

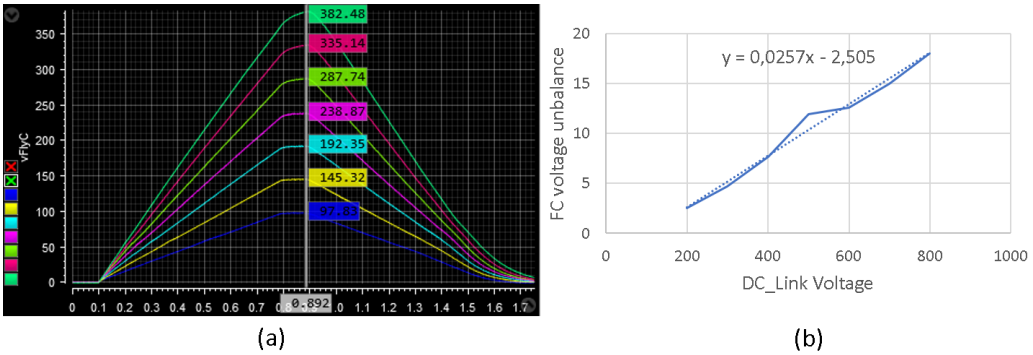


Fig. 6.28 (a) dSpace acquisition of the measured FC voltages of phase c with an additional 200pF capacitance in parallel to the internal leg devices and (b) linear dependence of the FC voltage unbalance which lead to a 18V drift at $V_{dc} = 800V$.

6.4.2 Loss Measurements

Fig. 6.29 illustrates the open loop test structure performed on a 300 μH three-phase inductor load. The DC-Link voltage takes 700ms to ramp up/down in order to maintain balanced the flying capacitors. During the minor base of the trapezoid a step current load is commanded. The converter has been tested up to 800V (DC-Link voltage) and 145 A (output phase peak current).

In order to have an efficiency estimation, an HBM data acquisition system has been configurated has shown in Fig. 6.23. It features a DC-Link voltage and current measurement and a phase output current sensing. The output load resistance has been evaluated by a LCR meter. Then, the load losses are subtracted to the input measured power. Due to the high inductor value of 300 μH, the current is filtered,

consequently the output currents high frequency harmonics are negligible and not considered in the loss model.

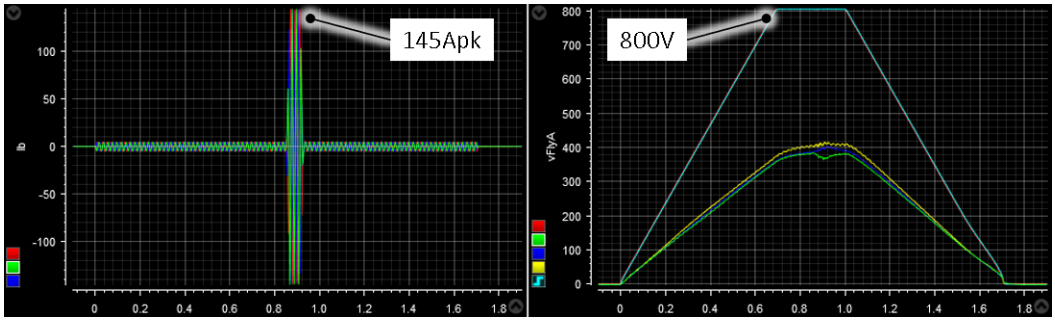


Fig. 6.29 Example of open loop 3LFC converter test dSpace acquisitions. The test feature 800 DC-Link voltage (i.e. represented in the right graph with the flying capacitors voltages) and 145 output peak phase current illustrated in the left graph.

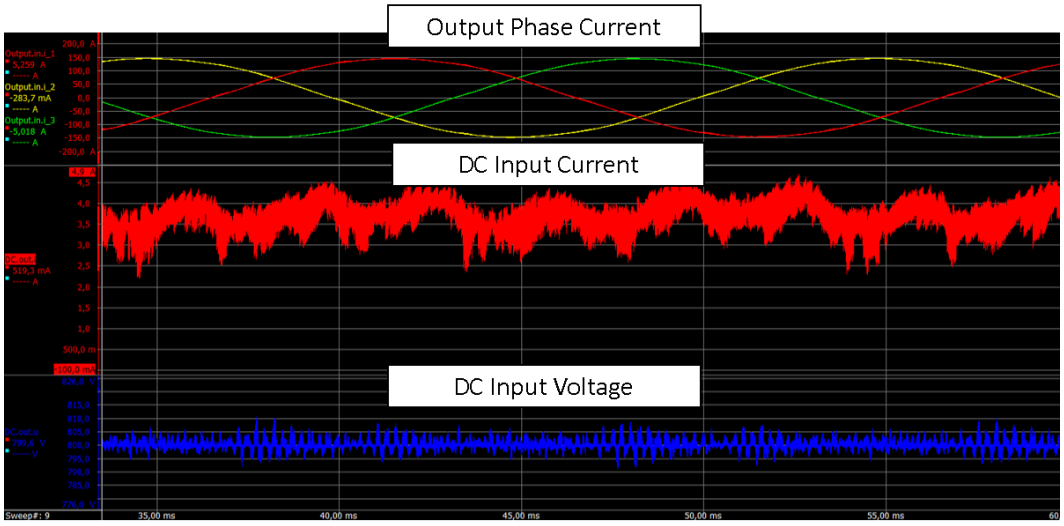


Fig. 6.30 Example of open loop 3LFC converter test HBM acquisitions. The test feature 800 DC-Link voltage and 145 output peak phase current.

Fig. 6.31 shows the HBM measured loss for different DC-Link voltages (i.e. 700-800V) and operating switching frequencies (i.e. 100-150 kHz) with the same test structure. These loss curves can be analytically expressed with a second order formula (with some approximations) in relation with the RMS output current (i.e. $P_{loss} = K_0 + K_1 I_{rms} + K_2 I_{rms}^2$). The conduction losses can be mainly attributed to the quadratic terms, while the switching ones to the constant (i.e. related to charge/discharge of the parasitic device output capacitances) and linear components. The obtained results are:

$$P_{loss}(700V, 100kHz) = 249.93 + 1.26I_{rms} + 0.15I_{rms}^2 \tag{6.12}$$

$$P_{loss}(800V, 100kHz) = 295.62 + 1.47I_{rms} + 0.16I_{rms}^2 \tag{6.13}$$

$$P_{loss}(800V, 150kHz) = 423.06 + 2.33I_{rms} + 0.17I_{rms}^2 \tag{6.14}$$

The conduction losses remain nearly the same among the tests. The switching losses are scaled according to the voltage ratio (i.e. $800V/700V \approx 1.14$) and the frequency ratio (i.e. $150kHz/100kHz \approx 1.5$). This is confirmed by the K_0 and K_1 curves coefficients:

$$K_0(800V/700V, 100kHz) \approx 1.18 \quad \text{and} \quad K_1(800V/700V, 100kHz) \approx 1.16 \tag{6.15}$$

$$K_0(800V, 150kHz/100kHz) \approx 1.43 \quad \text{and} \quad K_1(800V, 150kHz/100kHz) \approx 1.59 \tag{6.16}$$

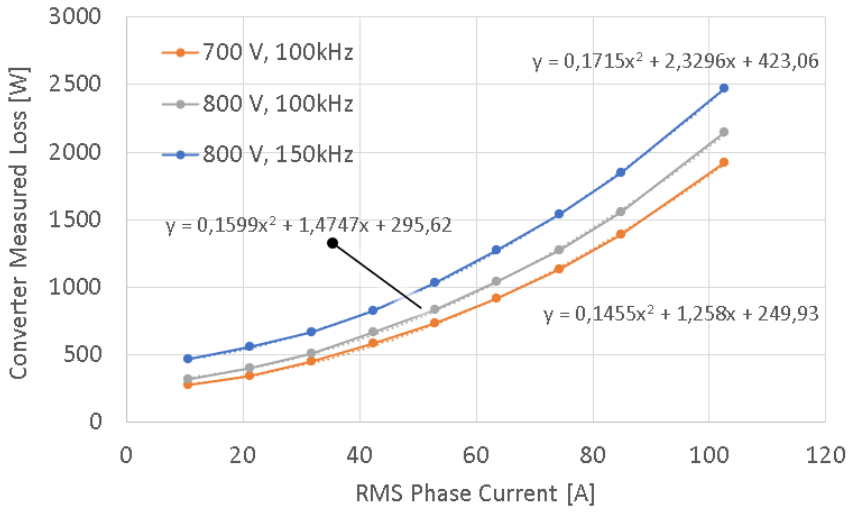


Fig. 6.31 HBM loss measurement curves in relation with the RMS output current for different DC-Link voltages and operating switching frequencies.

An interesting aspect to investigate is the losses related to dead-time. As explained before GaN, devices have different reverse conduction behaviour compared to the traditional Si/SiC MOSFETs. This originates a high reverse conduction offset voltage that worsen the dead-time losses making them more relevant compared to the traditional converters. For these reasons, some tests with different dead-time intervals have been performed. The relative HMB measured loss curved in relation with the RMS current are shown in Fig. 6.32. Taking into consideration the DC power measurement uncertainty (32.46 W at 2300 W), the dead time losses at 800V 145A (peak value) are 159W. It is important to notice that these losses can be minimized/eliminated with a proper adaptive dead-time control.

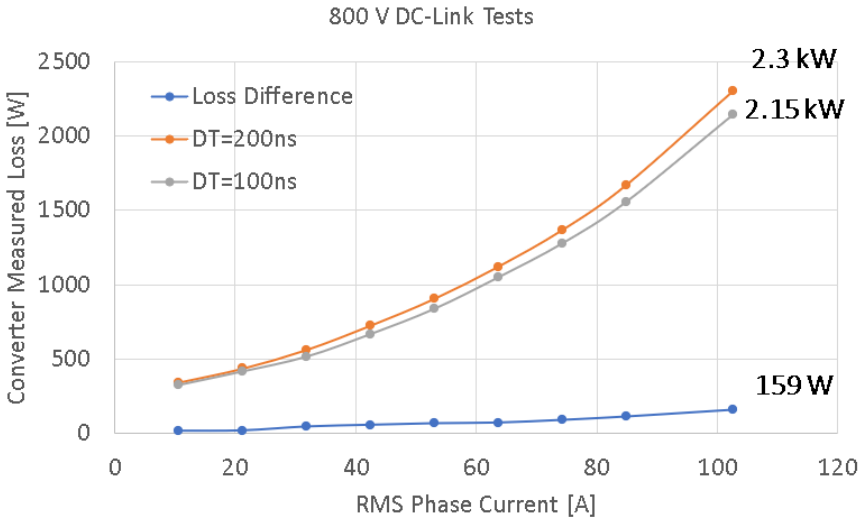


Fig. 6.32 HBM loss measurement curves in relation with the RMS output current for different dead-time intervals.

Table 6.2 shows the simulated losses components compared to the measured ones for $V_{dc} = 800V$, $I_{rms} = 102.5A$ and $f_{sw} = 100kHz$ converter operating point. It can be noticed a loss gap between the total values. One of the main uncertainty is the conduction flying capacitors loss model which is extremely dependent on the devices operation temperature. Due to the impulsive structures of the test, the CeraLink capacitors remain substantially at ambient temperature. For this reason, future tests include steady state operating condition to allow the FC to achieve thermal stability and to verify the steady-state operation of the converter. At the time of writing, the converter has been tested at $V_{dc} = 800V$, $I_{pk} = 30A$ and $f_{sw} = 100kHz$ operating point for ten minutes. No problems have been reported but the FC were still cold. After eliminating the dead time losses than can be minimized by a proper control

adoption, the remaining measured losses (i.e. $\approx 2000W$) would correspond to 98% overall (i.e. semiconductor, FC...) efficiency considering an hypothetical transfer power of 100kW. However, it is important to specify that the test on a inductive load (i.e. high power factor and low modulation index) represents the worst loss condition for the flying capacitors that is not representative for a traction inverter. Along with future endurance test, the converter will be tested in back-to-back configuration with the possibility to operate at arbitrary modulation indexes and thus showing a lower losses FC contribution and a higher overall converter efficiency.

Table 6.2 SIMULATED LOSS COMPONENTS COMPARED TO THE MEASURED ONES CONSIDERING $V_{dc} = 800V$, $I_{rms} = 102.5A$ AND $f_{sw} = 100kHz$

Parameter	**Description**	**Value**
P_{cond}	Simulated conduction losses	515W
P_{pcb}	Simulated additional conduction losses realted to PCB resistances	117W
P_{sw}	Simulated switching losses	256W
P_{dt}	Measured dead-time losses	159W
P_{FC}	Simulated FC losses	487W
$P_{sim,tot}$	Total simulated losses	1534 W
$P_{meas,tot}$	Total measured losses	2146 W

Another element that could influence negatively the efficiency is a non optimal commutation. At the time of writing, this aspects has started to be investigated on a two-level half-bridge leg prototype (i.e. simpler configuration compared to the FC multilevel topology) presented later and shown in Fig. 7.1. Several tests have been performed to find out the best combination of gate-to-source capacitance C_{gs} (i.e. 2nF are advised by the manufacturer) and gate resistances $R_{g,ON/OFF}$. Abnormal oscillations seem to be damped and the gate spike is reduced (i.e. probes limitation need to be considered) rising the C_{gs}, as shown in Fig. 6.33. From the preliminary commutation considerations, the gate-to-source capacitance must be increased to have a more reliable operation. To complete this analysis, future tests will be performed in continuous operation mode to check the reliability of the converter and the loss comparison between different driving circuits. The aim is to find out if the gate driver has influenced the losses on the 3LFC converter prototype.

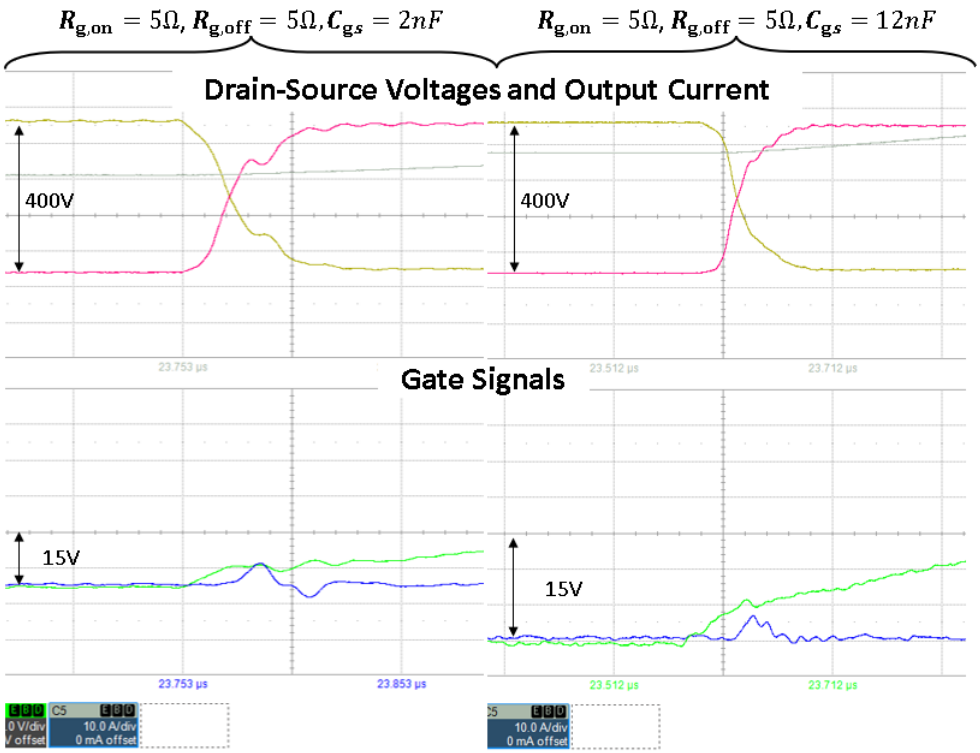


Fig. 6.33 Two-level half-bridge prototype commutation tests comparison with different gate driving circuit parameters.

6.5 Conclusion

This chapter presents the experimental results obtained from different prototypes. Firstly, the single-phase three-level flying capacitors converter is described. It represents an intermediated step to study the gate driving circuit, the devices commutations and the overall signal robustness before the three-phase inverter. After some preliminary double pulse tests, it has been performed a thermal characterization of the power switches on resistance and the system thermal resistances. Then, the loss measurements are illustrated for the converter operated in buck mode up to $V_{dc} = 800V$, $I = 100A$ and $f_{sw} = 100kHz$.

The VisIC V08 device gate driving circuit is thus deeply analysed on a separate board. It resulted that the device package in not symmetrical for the gate driving.

It is then shown the experimental set-up for the three-phase 3LFC converter. Firstly, the flying capacitors balance model through the parasitic output capacitors is theoretically expressed. The simulations results are thus experimentally verified. This

aspect results very important in the case of GaN devices where the manufacturing parametric dispersion is still high due to the low technological maturity. Then, the tests structure and the loss measurements curves in relation to the RMS current are presented up to $V_{dc} = 800V$, $I = 145A$ and $f_{sw} = 100 - 150kHz$. It is outlined the loss correlation with the DC-Link voltage, the switching frequencies and the dead-time intervals (i.e. this aspect can be relevant for GaN devices due to their non-standard reverse conduction behaviour). The measured losses are superior to the simulated ones. One of the main causes can be attributed to the FC loss model inaccuracy. Moreover, these test conditions represent the worst case for the FC losses. Indeed, the tests performed on an inductive load impose low modulation index and high power factor which is not representative of a traction application and represents the worst case condition for the FC RMS current and charge ripple stresses. In addition, due to the low operating time, the FC remains at ambient temperature where the CeraLink shows the worst resistance behaviour. To sum up, even if $\approx 2kW$ correspond to a 98% for an hypnotized 100kW transferred power, higher efficiencies are expected in future back-to-back continuous operation tests where the FC are less stressed and can achieve thermal balance. At the time of writing, the converter has been tested up to $V_{dc} = 800V$, $I = 30A$ and $f_{sw} = 100kHz$ for ten minutes.

Chapter 7

Fast Over-current Protection for VisIC Devices

7.1 Introduction

In the study of the flying capacitor multilevel configuration, some GaN behaviours have been marginally deepen. This raised the need to have a converter with a simple configuration where it is possible to easily debug these aspects. For this reason, it has been designed and realized the two-level half-bridge featuring a maximum DC-Link voltage of 400V and employing VisIC V08TC65S2A devices shown in Fig. 7.1. To be more robust, versatile and reliable, the PCB integrates the micro-controller, the gate drivers, the isolated DCDC supplies, isolated communication and the current sensors with the relative conditioning circuits. The complete converter assembly is shown in Fig.7.2. Due to its prototype nature, a forced air cooling system and TIM similar to the single phase 3LFC inverter analysed before has been chosen. The main GaN aspects to study in deep with this board are:

- the fast hardware implemented over-current protection;
- comparing the performance of two current sensors mounted on the board;
- investigating the dead-time influence on losses.

At the time of writing, the prototype has been assembled, however only the over-current protection has been tested. Then, the section discuss only this argument,

bearing in mind that the other prospectives of the converter will be deepen in future works.

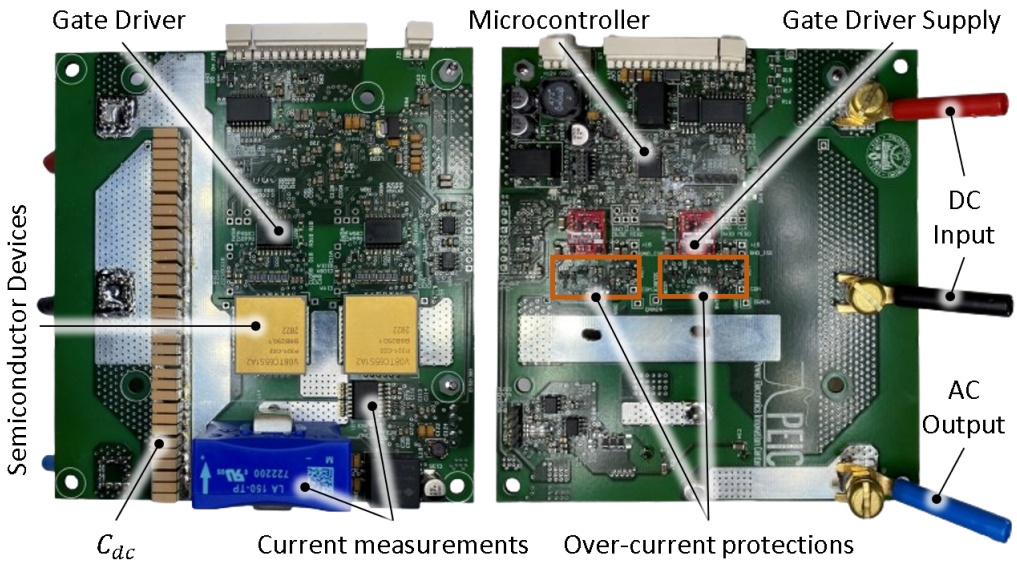


Fig. 7.1 Overview of the single-phase two-level 400V bridge-leg prototype PCB realized to investigate over-current protection.

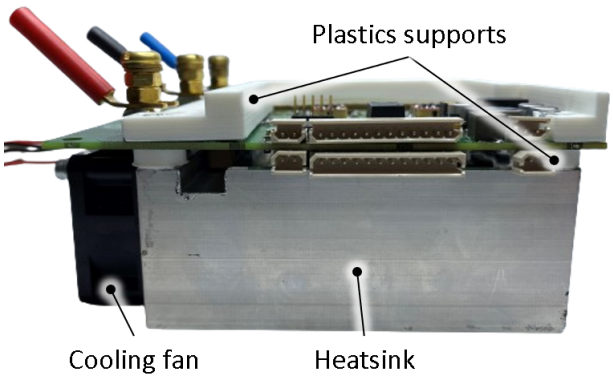


Fig. 7.2 Final converter assembly of the single-phase two-level 400V bridge-leg prototype PCB realized to investigate over-current protection.

The GaN technology is now approaching the semiconductor market. One of the main obstacle related on its adoption is the reliability. About this topic, it is important to be able to implement an effective fast over-current protection to ensure safe and robust converter operation. Even if the current sensors constitute an accurate current protection in overload occurrences, they are ineffective against current impulsive events due their low bandwidth. In these cases (i.e. short-circuit events), the device can achieve a catastrophic failure due to the instantaneous current level.

The short-circuit withstand time (SCWT) is then a fundamental device characteristic to design a fast over-current protection. For Si IGBT, it can achieve more than $10\mu s$ [215], while for SIC MOSFET it is around $2\mu s$ [216]. On the other hand, thanks to the featured high-power dense die area, the SCWT becomes less than $1\mu s$ for GaN devices [217]. Usually, SiC MOSFET and Si IGBT are safely turned OFF in case of instantaneous current increase through desaturation (DESAT) protection which sense the device conduction voltage $V_{DS,on}$ (i.e. it is an indicator of the flowing current) [216]. When the measured voltage overcomes a fixed threshold, after a designated blanking time, the switch is turned OFF softly, which means that it is turned OFF with a reduced speed to prevent catastrophic over-voltages. Several commercial gate drivers integrate this protection enabling the turn OFF of the device in few microseconds. Unfortunately, these protections are less effective for GaN devices considering their critical SCWT design requirements. Moreover, GaN devices feature an highly temperature dependent conduction characteristics and large parametric dispersion due to the low technological maturity compared to SiC and Si devices. This makes extremely difficult to design the threshold values for the different operating conditions. In literature, there are many different solutions specifically designed for the different GaN structures (i.e. there is no standard yet due to the low technological maturity). An example is [218] where the gate voltage is used to estimate the drain current for GIT GaN devices. There are lots of efforts to integrate this protection directly in the device package enhancing the precision and the intervention rate [219]. With the exception of [220], the majority of the studies apply to e-mode devices.
This work aims to realize a fast over-current protection for VisIC V08 direct-drive switches using commercial driver with few additional components. The proposed architecture simplified scheme is shown in Fig. 7.3. The selected commercially available gate driver is the UCC21750 by TI. It features an high common mode immunity, input PWM signal glitch filter and DESAT with soft turn-off. On the contrary of the standard DESAT protection, in the presented scheme, the voltage of the LV cascode Si MOSFET Q2, which substantially act as a shunt resistors inside the device package is monitored. The main benefits of this solution are:

- An existing component is exploited, thus no additional parasitics are added by external elements;

- There is no need of a high voltage diode to protect the measurement system since the voltage across the Q2 MOSFET remains low during the converter operations;
- The cascode Si MOSFET features an overall lower parametric dispersion and better thermal stability compared to the d-mode GaN;
- Since the cascode has the function of enable for power switch, it is always kept turned ON. Consequently, there is less necessity to filter the noises due to the device commutation.

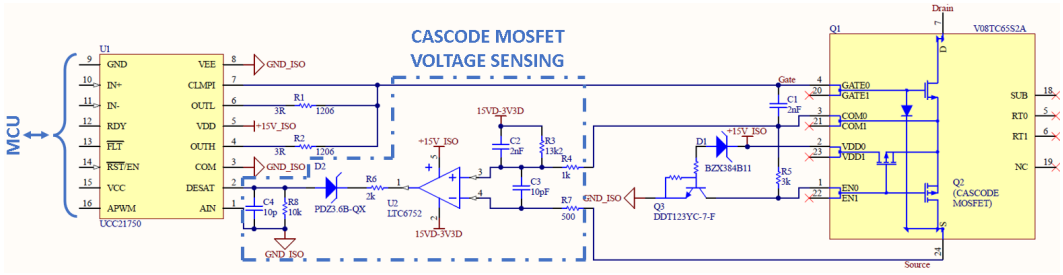


Fig. 7.3 Simplified scheme of the proposed fast over-current protection architecture.

The cascode MOSFET voltage is then measured by LTC6752. It is a fast and precise comparator of which the intervention level is designed considering the current flowing in the MOSFET. Once it has been triggered, the gate driver is enabled to softly turn-off the device. All the measurement chain inserts some intervention delays such as the DESAT propagation delay and leading edge blank time introduced by the gate driver and the comparator delay. These are summarized in Table 7.1. They are particularly important due to the stringent SCWT requirements of GaN devices.

Table 7.1 DELAY TIMES COMPONENTS INTRODUCED BY THE PROPOSED OVER-CURRENT PROTECTION VOLTAGE MEASUREMENT CHAIN

Parameter	**Description**	**Value**
$t_{DESAT,OFF}$	Driver DESAT Propagation Delay	300ns
t_{LEBT}	Leading Edge Blank Time	200ns
t_{comp}	Comparator Propagation Delay	20ns

7.2 Simulation and Experimental Validation

Before the realization of the prototype, some simulations have been performed using LTSPICE. They employ models of the power switch (i.e. VisIC V08TC65S2A), the comparator (i.e. LTC6752) and the gate driver (i.e. UCC21750). This last model is particularly important because it is able to simulate the complex logic relative to the internal DESAT protection and the soft turn-off. Tuning the resistors R2 and R4 in Fig. 7.3, the comparator voltage threshold has been set at 326mV, which corresponds to a device drain current of 240A. Fig. 7.4 shows the simulation results in the case where an inductance of 5 μH is short-circuiting the lower switch of the two-level switch leg.

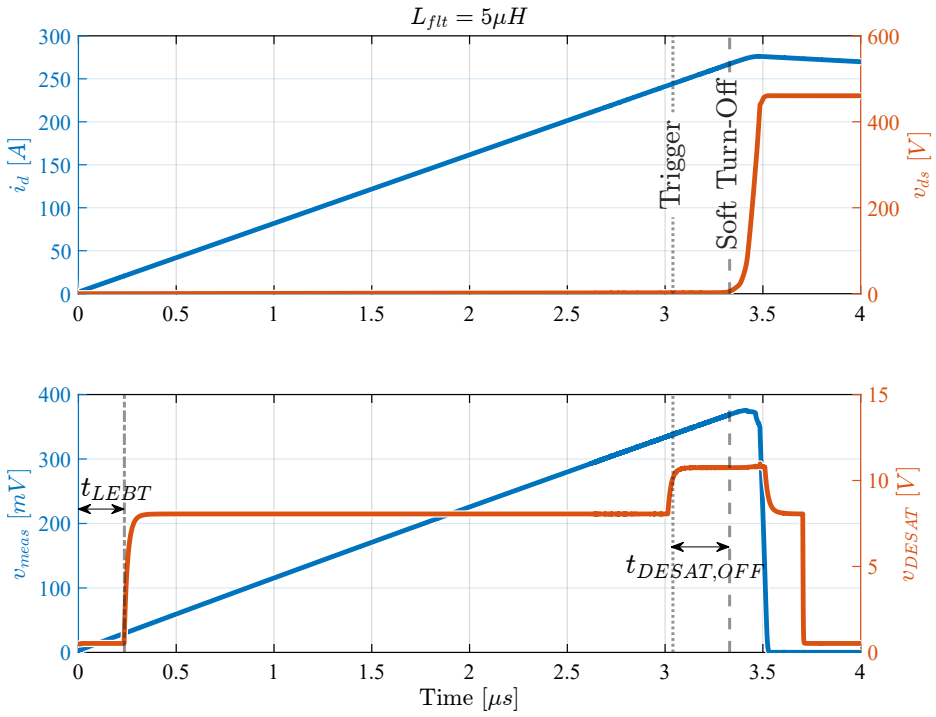


Fig. 7.4 LTSPICE simulation of the proposed fast over-current protection architecture. The device drain-to-source voltage (v_{ds}) and drain current (i_d), measured voltage on the cascode MOSFET (v_{meas}) and the gate driver DESAT pin voltage (v_{DESAT}) are simulated in the case of a fault inductance of 5 μH short-circuiting the lower switch.

In particular, the device drain-to-source voltage (v_{ds}) and drain current (i_d) are shown in the upper graph and the measured voltage on the cascode MOSFET (v_{meas}) and the gate driver DESAT pin voltage (v_{DESAT}) are illustrated in the lower graph. Clearly, the voltage measured across the LV cascode MOSFET is proportional to

the current flowing through the device. Due to its internal logic, the gate driver DESAT pin is forced to 0V during the leading edge blank time (t_{LEBT}). Then, its voltage value is stabilized at 7.5V. Only when v_{meas} achieves 326mV, the comparator triggers the gate driver protection bringing the DESAT pin voltage at 10.5V (i.e. the threshold trigger value is 9.15V). However, the soft turn-off is performed only after the driver propagation delay ($t_{DESAT,OFF}$). This period is the resulting sum of the de-glitch filter time (i.e. 140ns) and the execution time delay (i.e. 160ns in the worst case). The soft turn-off of the device allows to avoid disruptive over-voltages due to the high commutated current. Then, the FLT pin of the gate driver is lowered to GND and consequently the fault event is reported to the control unit.
The experimental validation has been performed on the converter prototype shown in Fig. 7.1. As illustrated in the simulation, the fault is simulated by turning on the high switch (SWH) with an equivalent fault inductance load (L_{flt}) in parallel to the low side switch (SWL). All the presented tests are performed with the DC-Link voltage equal to 400V. Fig. 7.5 shows the experimental test of the proposed over current protection circuit. In particular, the top graph illustrates the drain-to-source voltages of the high and low side switches, while the bottom graph reports the measured gate driver DEASAT pin voltage v_{DESAT} and the half-bridge leg output current i_d. In this case, to emulate the fault a L_{flt} equal to $17.6\mu H$ has been selected. As a consequence, when the SWH is turned ON, the output current presents a rise slope of $22A/\mu s$. Similarly to the described LTSPICE simulations, the gate driver protection mechanism is triggered when the measured voltage across the cascode MOSFET reaches about 326mV and the DESAT pin voltage varies from 7.5V to 10.5V. As explained before, the comparator delay and the $t_{DESAT,OFF}$ can be externally reduced because are manufacturing features of the selected devices. After the device is turned OFF softly, the fault is reported to the control unit. The maximum i_d value reached during the test is 243A.

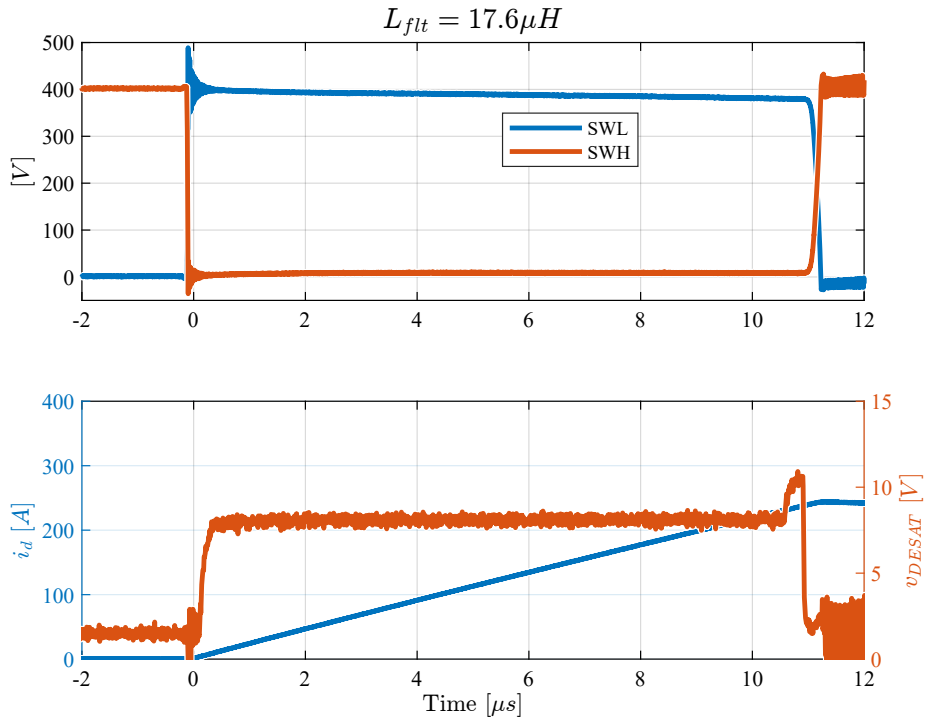


Fig. 7.5 Proposed architecture over current protection experimental tests emulating the fault condition with a $L_{flt} = 17.6\mu H$ short-circuiting the lower switch. The top plot reports the drain-to-source voltages for the high and low side switches. The lower plot illustrates the measured voltage at the DESAT pin of the gate driver (v_{DESAT}) and the switch leg output current (i_d).

Fig. 7.6 shows the same test performed before emulation a more severe failure condition ($L_{flt} = 2.1\mu H$). In this case, the measured output current slope is sensibly higher (i.e. $157A/\mu s$). On the other hand, the gate driver protection is triggered at 213A. This discrepancy can be attributed to the parasitic inductance $L_{\sigma,MOS}$ relative to the cascode MOSFET. When there is a high current slew rate, this parasitism causes an additional voltage drop measured by the comparator following the formula:

$$v_{meas} = R_{ds,ON} + L_{\sigma,MOS}\frac{di_d}{dt} \tag{7.1}$$

Considering the low voltage cascode MOSFET on resistance $R_{ds,ON}$ equal to $1.25m\Omega$ (i.e. from component datasheet), the estimated device parasitic inductance is around 1nH. The maximum i_d value reached during this test is 227A.

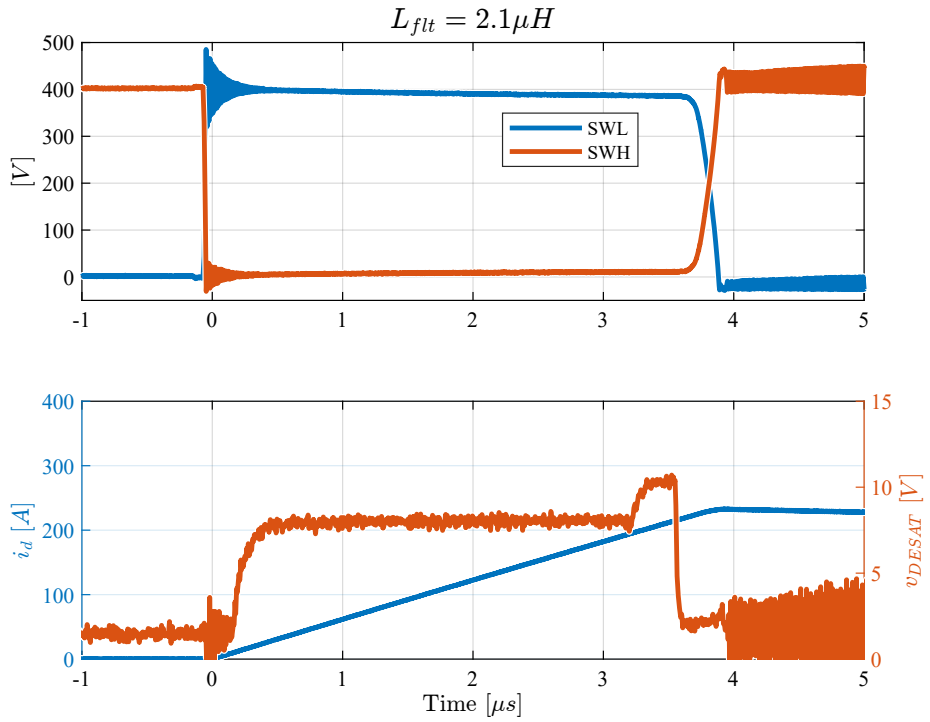


Fig. 7.6 Proposed architecture over current protection experimental tests emulating the fault condition with a $L_{flt} = 2.1\mu H$ short-circuiting the lower switch. The top plot reports the drain-to-source voltages for the high and low side switches. The lower plot illustrates the measured voltage at the DESAT pin of the gate driver (v_{DESAT}) and the switch leg output current (i_d).

Fig. 7.7 shows the same previous tests structure with a $L_{flt}0.7\mu H$. In this case the comparator is trigger instantaneously considering a current rise slope of $380a/\mu s$. It can be noticed that v_{DESAT} is kept to 0V for 200ns at the beginning of the test due to the driver leading edge blanking time. After this event, the driver protection is triggered and the soft turn-off is performed after around 300ns (i.e. according to the $t_{DEAST,OFF}$ delay explained before). The resulting maximum measured output current for this test is 380A.

Several tests have been done with the same illustrated structure by varying the fault inductance value. The results are summarized in Table 7.2 where it is reported the output current slew rate di_d/dt, the maximum measured output current in the test $I_{flt,max}$, the driver trigger time t_{trg} and its relative current level I_{trg}. It can be pointed out that when the current rise slope is higher than $326A/\mu s$ the comparator is triggered instantaneously, as described in the $L_{flt}0.7\mu H$ test. To sum up, there is still a residual intervention time delay (i.e. $t_{LEBT} + t_{DESAT,OFF}$) which cannot be eliminated.

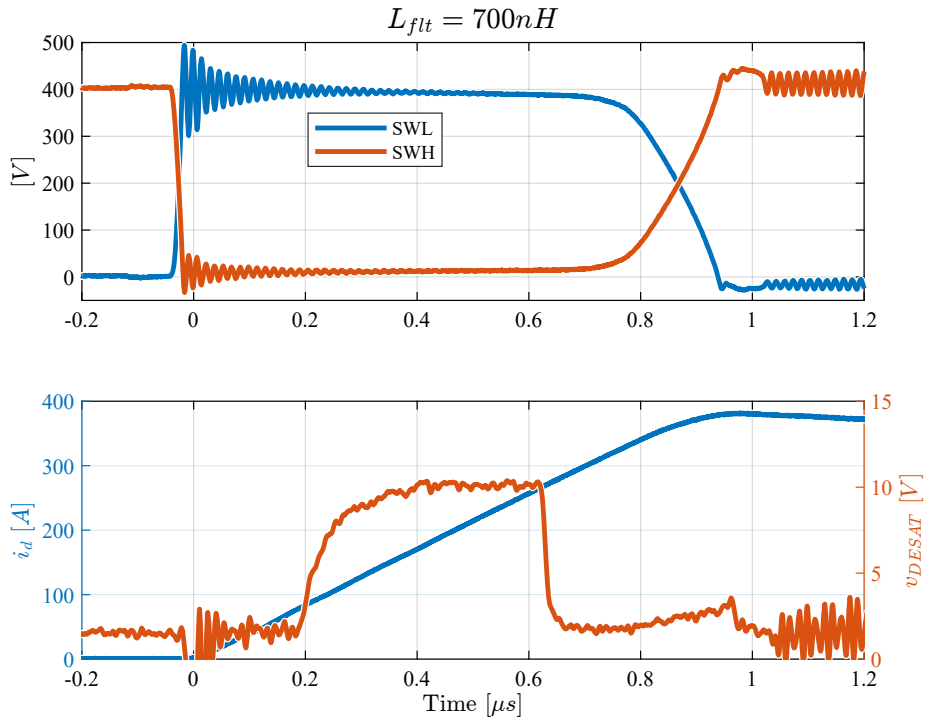


Fig. 7.7 Proposed architecture over current protection experimental tests emulating the fault condition with a $L_{flt} = 0.7\mu H$ short-circuiting the lower switch. The top plot reports the drain-to-source voltages for the high and low side switches. The lower plot illustrates the measured voltage at the DESAT pin of the gate driver (v_{DESAT}) and the switch leg output current (i_d).

Lower test inductance than 700nH test have been performed but the designed over current protection failed to protect the device failure. The reason is unclear, their event can be attributed to multiple causes such as the potential failure of other components (i.e. as the gate driver or the isolated DCDC power supply), the overcoming of the device SCWT or the device degradation due to the multiples short-circuit tests.

Table 7.2 Designed Over Current Protection Intervention Time for Different L_{flt}

L_{flt}	di_d/dt	t_{trg}	I_{trg}	$I_{flt,max}$
$17.6\mu H$	$21.7A/\mu s$	$10.7\mu s$	$231A$	$243A$
$10.5\mu H$	$36.0A/\mu s$	$6.0\mu s$	$216A$	$236A$
$6.3\mu H$	$60.1A/\mu s$	$3.3\mu s$	$195A$	231
$2.1\mu H$	$156.7A/\mu s$	$0.73\mu s$	$114.5A$	$227A$
$1.4\mu H$	$238.0A/\mu s$	$0.33\mu s$	$72.5A$	$239A$
$0.7\mu H$	$380A/\mu s$	$0\mu s$	$0A$	$380A$

7.3 Conclusion

This chapter describes some additional experimental tests related to GaN devices fast over-current protection performed during the PhD activity. The proposed architecture is specifically designed for VisIV V08 GaN direct-drive cascode devices. In particular, the main differences with the standard DESAT protection are outlined and the new two-level converter prototype for the experimental validation is presented. The proposed fast over current protection scheme is described, it is simulated through LTSPICE and it is experimentally verified up to 700nH of equivalent output leg short-circuit inductance. The main benefit of the presented architecture includes the voltage measurement on the LV Si cascode MOSFET. It is substantially used as shunt resistor (i.e. avoiding the introduction of additional parasitics by external devices), which presents less parametric dispersion and lower temperature dependence compared to GaN technology. Moreover, it eliminates the need of the high voltage diode proper of standard DESAT protections. Its parasitic inductance is exploited to speed up the protection intervention time in the case of fast current derivatives (i.e. proper of short-circuit events). The system is more noise robust since the cascode MOSFET does not commutate with the GaN semiconductor.

Chapter 8

Conclusion

This chapter concludes the thesis summarizing the presented works and underlining the main obtained results. Finally, some interesting future research activities are prospected.

8.1 Summary of the Thesis

The main goal of the thesis is to develop an innovative traction inverter for motorsport application. In order to achieve the tightened requirements of efficiency and power density imposed by the automotive sector and overcome the state-of-the-art solution, the adoption of new technologies and non-standard architectures are mandatory. This works identify the GaN devices, the PLZT ceramic capacitors and multilevel topologies as key elements to push forward the traction inverter performances. Each argument is analysed separately underlining the main strengths and drawbacks. Then, a three-phase three-level flying capacitor converter is realized and experimentally validated. The main results are summarized for each chapter:

- **Chapter 2: Wide Band-Gap Power Devices**
  The growing demand of lower specific conduction resistances and faster commutation brings the semiconductor market to the continuous research of materials that present better intrinsic physical properties than silicon. In this field, gallium-nitride semiconductor devices has recently showed up promising excellent properties. The chapter firstly presents its features and the normally

ON depletion structure. Then, all the main normally OFF architecture are described highlighting the main benefits and drawbacks. Since the technology is still not mature, no winning standard is currently affirmed in the market. The analysis continues presenting some unusual behaviours that distinguish GaN devices from the Si/SiC counterpart. They are the breakdown mechanism, the current collapse phenomenon and particular reverse conduction behaviour. This GaN state-of-the-art analysis ends illustrating some possible interesting future research trends according to the author view.
The second part of the chapter aims to provide an useful method to effectively compare different semiconductor technologies for the considered application. Firstly, a simplified loss model of a two-level half-bridge inverter is analytically expressed. As explain later, it is applicable also to some multilevel topologies such as flying capacitor architecture. Then, the concept of figure of merit is introduced as a powerful tool to compare power switches. After a literature review, a new FOM type is analytically derived. It effectively compares different semiconductor technologies for the target application, considering the converter and device operating point (i.e. the DC-Link voltage, the junction temperature and the switching frequency), which turn out to be fundamental in the semiconductor choice.

- **Chapter 3: Multilevel Converter Topology**
  The new automotive DC-Link voltage standard (i.e. 800V) is considered for this application. The two-level topology requires high-voltage rating devices (i.e. 1200V). The multilevel topology enables the usage of GaN devices (i.e. currently limited to 650V) in this field. Employing lower voltage rating devices with a better FOM, these structures can achieve better efficiencies and power densities. Moreover, these architectures synthesized an excellent output voltage quality waveform (i.e. with low harmonic content). The combination of higher switching frequencies and lower voltage steps commutated contribute to reduce the PWM losses and the dv/dt stress on the motor, which is appreciated for the considered application. The main drawback lays in the higher device numbers and the consequent more complicated control structure. The chapter proceeds analysing the main multilevel architectures. Taking into consideration the device requirements, the modularity and the power commutation loop, the flying capacitor converter results the optimal choice to realize the target converter.

- **Chapter 4: Capacitor Technology**
  This chapter focuses on the optimization of the DC-Link, which is one of the bulkiest inverter components. State-of-the-art film technology is then compared to the PLZT ceramic capacitors. The last components present an higher specific capacitance, maximum operating temperature and RMS capabilities. Moreover, while films capacitors are manufactured in big custom blocks, they are available in small packages with a reduced ESL (i.e. thus an higher resonance frequencies) that are more easily integrated in the commutation loop eliminating the need of decoupling capacitors. These features perfectly matches with the high switching frequencies and critical power loop design of WBG devices.
  Then, a DC-Link sizing procedure for a two-level inverter is described taking into consideration temperature and the switching frequency dependencies of both capacitor technologies. From this analysis, it is shown that PLZT ceramic capacitors can achieve a substantial capacitance requirements compared to film-based counterpart exploiting the higher f_{sw} of WBG devices. The chapter proceeds illustrating some experimental tests performed on a single PLZT capacitor device. The thermal and electrical behaviour are verified. Moreover, it is experimentally extracted a large-signal equivalent capacitance curve that is not provided by the manufacturer. It can be used to perform a precise DC-Link sizing.
  Since the RMS current stresses and the charge ripple DC-Link sizing requirement are the same for the 3LFC converter, the proposed DC-Link sizing procedure has been validated on an two-level inverter prototype. This structure is well-known and established and thus easier to test experimentally. With this consideration an EV 550kVA 800V SiC inverter has been designed and realized. The full PLZT ceramic DC-Link features two third lower volume and one third lower weight compared to an equivalent film-based solution. Finally, the measured peak-to-peak voltage ripple is compared with the proposed model results showing excellent agreement.

- **Chapter 5: Three-Phase Three-Level Flying Capacitor Converter**
  A detailed design procedure is described for a three-phase three-level flying capacitor converter employing GaN devices and PLZT ceramic capacitors. The selected innovative technologies and non-standard multilevel architecture present complementary features. The goal of the thesis is to exploit all these

advantages and integrate them in a single inverter prototype ables to achieve the future challenging requirements of the motor-sport sector. In particular, all the stresses are analytically expressed for the main active and passive converter elements. Among them, the phase flux ripple is identified as a key parameter indication of the PWM induced losses generated in the load machine (i.e. important for the considered application). A comparison with the standard 2LVSI is analysed showing the superiority in this field of the selected structure. The chapter continues describing the realized prototype with some focuses on important aspects such as the commutation loop and the mechanical assembly.

- **Chapter 6: Experimental Validation**
  The chapter describes all the experimental results obtained from different boards that employ GaN devices. Firstly, a single-phase three-level flying capacitor has been realized to preliminary test the gate driver circuitry, the power commutation loop and the converter structure operational basics. About this prototype, some DPT tests and a thermal characterization are presented. In particular, a thermal characterization of the device electrical resistance and of the system thermal resistances has been performed. The converter is operated in buck mode up to $V_{dc} = 800V$, $I = 100A$ and $f_{sw} = 100kHz$, the relative loss measurements are presented.
  Then, the asymmetrical gate driving of the selected VisIC GaN device is experimentally analysed on a separate board. Indeed, a not optimal gate driving can bring to a device abnormal commutation.
  The paragraph continues with the experimental tests on the three-phase prototype designed in the previous chapter. Firstly, the flying capacitor voltage balance influence by the device output parasitic capacitance is analysed. The theoretical proposed model is validated by simulation and experimental results. This represents an important issue for nowadays GaN devices which present a relative still high parameter dispersion compared to the Si/SiC counterpart. Then, the loss measurement curves are illustrated in relation to the RMS current in different DC-Link voltage and switching frequency conditions and the relative relation is highlighted. Moreover, also an experimental characterization of losses in relation with the dead-time is described. This aspect is important for GaN devices which do not present conventional reverse conduction behaviour. The converter is operated up to $V_{dc} = 800V$, $I = 145A$ and $f_{sw} = 100 - 150kHz$. The discrepancy between the simulated and measured

losses can be attributed to the extreme temperature dependent behaviour of the FC.

- **Chapter 7: Fast Over-current Protection for VisIC Devices**
  In this chapter a fast over-current protection designed for VisIC GaN cascode using commercially available components is analysed. Contrary to the classical DESAT protection, the designed circuit measures the voltage across the LV cascode MOSFET that acts as a shunt resistor. Consequently, no high voltage diode is needed and the commutation does not influence the measurement. The proposed architecture is simulated with LTSPICE and experimentally validated up to 700nH (i.e. to simulate an equivalent output short-circuited condition).

8.2 Future Developments

This thesis represents the first initial step to investigate the potentialities of GaN devices, PLZT ceramic capacitor, multilevel topologies and most importantly their interaction in a single inverter prototype. A more integrated and optimized design approach will be used in the second version of the inverter prototype. Some aspects such as the influence of the variation of parasitic parameters of ESL/ESR PLZT capacitors' bank on the inverter design now neglected will be analysed with a software such as Ansys. The main topics to be deepen in future research activities are:

- *Three-phase inverter prototype characterization in back-to-back configuration* is necessary to test the converter in arbitrary modulation index and power factor in order to reproduce operating condition more similar to motor-sport application;
- *Parallel device operation* needs to be carefully studied in order to enable the design of higher power rated converters;
- *Losses related to dead-time characterization* is fundamental for GaN devices that present a non standard reverse conduction behaviour that could compromise the converter efficiency especially for high switching frequencies values.

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