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Hyperbolic Segmentation of Gate Driver Output Transistors for a Clean Switching of 650V GaN HEMTs Half Bridges

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Abstract

This paper deals with the mitigation of the overvoltages and the high frequency oscillations resulting from the fast switching of high voltage e-mode GaN HEMTs. The investigation is carried out referring to a half bridge including the power transistors package parasitics and the printed circuit boards stray inductances. The impact of the gate drivers strength on the above mentioned quantities is evaluated through time domain analysis by changing the width of the transistors composing the gate driver output stage. A criterion to perform the partitioning of such transistors that allow for a fine control of overvoltages and ringing is proposed, then used to design a segmented gate driver.

1 Introduction

Common gate drivers for high voltage (HV) e-mode GaN HEMTs are usually designed to turn on (off) as fast as possible and to avoid self immunity issues, meaning the spurious turn on due to the output fast switching. Wanting to address these issues, and to cover a broad range of power GaN HEMTs, the nMOS and the pMOS transistors composing the output stage of commercial gate drivers are usually over sized.

However, the strength of the gate driver, meaning its sourcing (sinking) capability, often needs to be reduced to avoid unwanted overshoots, undershoots and oscillations affecting both voltages and currents of the gate loops and the power loops.

This point can be better explained referring to the half-bridge (HB) shown in Fig. 1. It is made up of two high voltage e-mode GaN transistors T1, T2 each one driven by an isolated gate driver whose output transistors M_p and M_n are connected off chip to the power transistor gate terminal through the resistors $R_{G,xx}$, $R_{G,yy}$, respectively. The former limits the current sourced to the gate terminal at the turn on, the latter the current sunk from the gate terminal at the turn off. The values of such resistors is usually selected case-by-case through a trial and error approach, since they are tightly related to the gate loop and the power loop stray inductances, as well as to the power transistors stray capacitances. This approach is time consuming, since the magnitude of overvoltages, undervoltages and spurious voltage spikes affecting the power transistor drain-source and gate-source voltages depend on the operating conditions (load current, power rail voltage, dead time, etc.,) as well as on the devices temperature.

A better solution to address the problem requires the use of segmented gate drivers, meaning devices which output transistors width can be set by the user on a case by case basis. In them, each output transistor is made up of N elementary transistors of the same type connected in parallel that can be turned-on and turned-off independently. Their widths are usually scaled by the power of two so that the relationship between the binary code used to set the drain-source resistance of each transistor and the input code is straightforward [1], [2], [3].

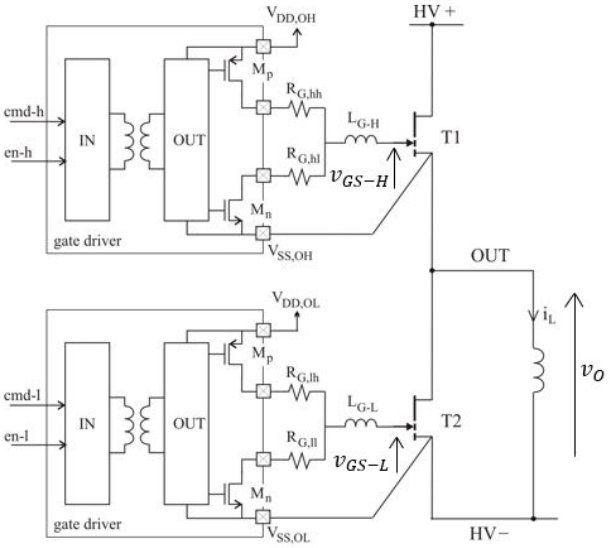

Figure 1 Half-bridge based on e-GaN HEMTs with the gate driver output stage transistors (Mp, Mn) highlighted.

This paper shows that the dichotomous segmentation of the gate driver output transistors is not the most appropriate to mitigate unwanted undershoot, overshoot, oscillations and spurious spikes affecting the gate-source and drain-source voltages of the GaN HEMT. A novel approach to do that is proposed and its effectiveness is proved through time domain simulations.

The paper is organized as follows. Section II shows the

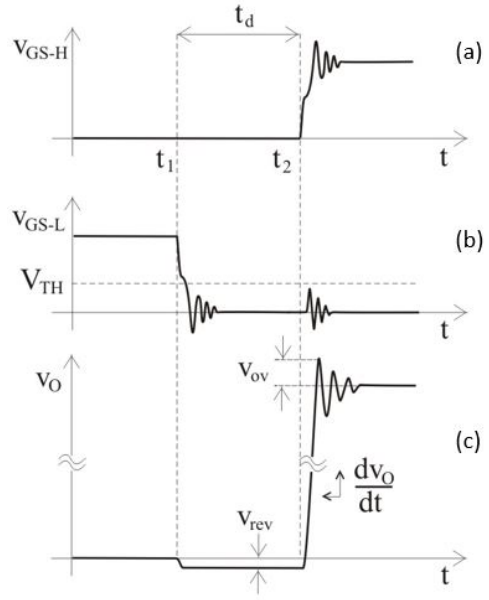

Figure 2 Waveforms of the gate-source voltages and the output voltage of the half bridge affected by spurious oscillations and spikes.

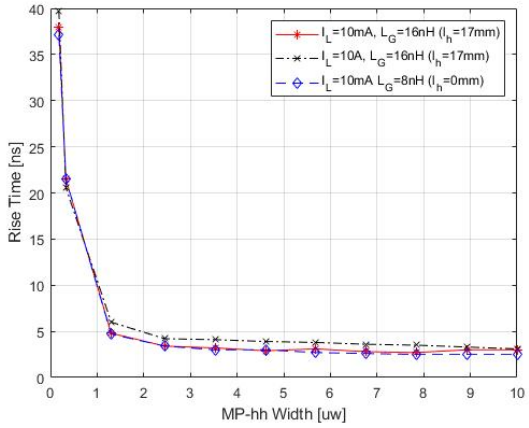

Figure 3 Rise time of the output voltage versus the W_{P-hh}.

causes at the basis of the spurious effects resulting from the fast switching of the GaN HEMTs. Section III summarizes the results of the analysis carried out on a HB to evaluate the impact of the gate driver output stage transistor width on the cleanness of the switching waveforms. Section IV proposes a hyperbolic segmentation of the output stage transistors and Section V shows a possible implementation of a segmented gate driver. Some concluding remarks are shown in Section VI.

2 Half-Bridge Hard Switching

Most of high voltage power switching circuits like those used in DC-DC and DC-AC converters are based on switching legs like that shown in Fig. 1. Besides the power switches, it comprises of two isolated gate drivers, which in turn include an input device or low voltage IC (IN) and an output one, known as high voltage IC (OUT). A microcontroller (not shown in Fig. 2) provides the input IC with the commands to switch the related power transistors cyclically. The information (cmd-x) is transferred to the HV IC over a galvanic isolation, which can be a transformer based circuit like that shown in Fig. 1. The output IC drives the gate driver output transistors M_p, M_n in a coherent fashion to switch the related power transistor on and off. Furthermore, the power supply needed for the operation of each gate driver is provided by isolated DC-DC converters followed by linear voltage regulators (LDO) that allows for a fine tuning of the power supply voltages. Such auxiliary circuits are not shown in Fig. 1 for the sake of simplification. The nominal operation of a switching leg can be presented referring to the waveforms shown in Fig. 2. T1 and T2 are initially off and on, respectively. Wanting to drive an inductive power load, T2 is switched off at t_1, but due to the load current, T2 runs in reverse conduction mode as long as the high side (T1) remains switched off. At the end of the dead time (t_d), i.e., at t_2, the turn on of T1 brings the output voltage (v_O) to the high voltage level (HV+) as sketched in Fig.2a. The slew rate of such transition depends on the power transistor switching speed and on the stray capacitance loading the output node, i.e., the output capacitance of the power switch (C_{OSS}) and the stray capacitance of the load.

Close to t_2 the output voltage shows an overshoot followed by oscillations as sketched in Fig. 2c. This is due to the power loop stray inductance (not shown in Fig. 1) that resonates with the stray capacitance loading the output node. Usually this is dominated by the switched off power transistor output capacitance, that of T2 in this case. Depending on the power loop damping resistance, meaning the sum of the ESR of the DC link capacitors and the on resistance of T1, the overshoots can exceed the DC link voltage even of 40 - 50%. The continuous violation of the maximum voltage applicable to the drain-source terminals of the power devices lowers its lifetime causing reliability issues at the application level. Furthermore, the oscillations contribute to enrich the electromagnetic emission delivered by the power circuit, therefore, it is beneficial to remove them as well. Given that, both the overshoot and the oscillations that follow t_2 deal with the slope of the output voltage, and being this related with the current injected into the gate terminal of T1, both issues can be addressed by trimming R_{G-hh} properly.

About the gate source voltages of the two power transistors, they are also affected by overshoots, undershoots and oscillations at each switching, as sketched in Fig. 2a and 2b. Those affecting v_{GS-H} (v_{GS-L}) at t_2 (t_1) deals with the stray inductance L_{G-H} (L_{G-L}) of the wiring connecting the gate driver output pins to the power transistor, which resonates with the input capacitance (C_{ISS}) of T1 (T2). If the gate source voltage exceeds the minimum or the maximum value specified in the data sheet, the device is damaged permanently. Also in this case, the problem can be addressed by lowering the strength of the gate driver with the external resistor $R_{G,xx}$. In particular, the oscillations affecting v_{GS-H} at t_2 (see Fig. 2a) can be damped by $R_{G,hh}$, those

affecting v_{GS-L} at t_1 (see Fig. 2b) by $R_{G,ll}$.
In addition, the gate-source voltage is affected by the spurious spike resulting from the fast switching of the output voltage. This effect is highlighted in Fig. 2b where the gate source voltage of T2 (v_{GS-L}) is affected by a voltage spike at t_2 although T2 is driven to stay off. Such a voltage spike is due to the high dV/dt of the output voltage that propagates through the voltage divider composed of the low side gate-drain stray capacitance (C_{GD}) and the gate-source input capacitance (C_{GS}), which is in parallel with the gate driver output impedance.

3 Impact of Gate Driver Strength on HB Switching Performance

As mentioned in the introduction, unwanted overvoltages, oscillations and spikes affecting the gate-source and drain-source voltages of the power transistors can be better managed using segmented gate drivers rather than external resistors ($R_{G,xx}$). Aiming to that, an HB like that shown in Fig. 1 comprising two HV e-mode GaN HEMTs [5] driven by their respective CMOS push-pull output stage was considered. The cases of the power transistors and the gate drivers hosted in the same printed circuit board and in separate boards were considered. The stray inductances of the power loop and gate loops were extracted referring to the application boards presented in [6], then included in the simulation setup.
Parametric time domain analyses were carried out to evaluate the impact of the width of the gate driver output transistors on the rise time (t_r), on the overshoot (v_{ov}) of the output voltage (see the waveform in Fig. 2c), as well as on the magnitude of the overshoot (v_{GS-ov}) and the spurious spike (v_{sp}) affecting the gate source voltage (see the waveforms in Fig. 2a,b).
The variation of the rise time (t_r) versus the width of the high side driver output transistor (W_{P-hh}) is shown in Fig. 3. The analyses were repeated for load current of 10 mA (continuous line) and 10 A (dash-dotted line), having the gate drivers and the power transistors hosted in the same board (dashed line) and in separate boards (continuous line). These plots show that the rise time is not affected neither by the load current magnitude nor by the gate loop stray inductance. Furthermore, it is worth highlighting that the rise time changes remarkably for $W_{P-hh} < 3\ uw$ to saturate to about $t_r = 3ns$ above that value.
The overshoot experienced by the output voltage (v_{ov}) versus W_{P-hh} is shown in Fig. 4. It appears for $W_{P-hh} > 2.5\ uw$ and its magnitude rises with W_{P-hh} non-linearly.
Also the overshoot experienced by the gate source voltage of the high side transistor depends on W_{P-hh}. Its magnitude v_{GS-ov} versus W_{P-hh} is shown in Fig. 5.
Furthermore, the magnitude of the spurious spike v_{sp} affecting the gate-source voltage of the low side transistor versus W_{P-hh} is shown in Fig. 6. Similarly to the rise time, also the magnitude of the spurious spike changes significantly for $W_{P-hh} < 2.5\ uw$ to saturate to the power transistor threshold for $W_{P-hh} > 3.5\ uw$. Indeed, the magnitude of such spikes depends on the slew rate of the output voltage at t_2 (see Fig. 2). Therefore, wanting to

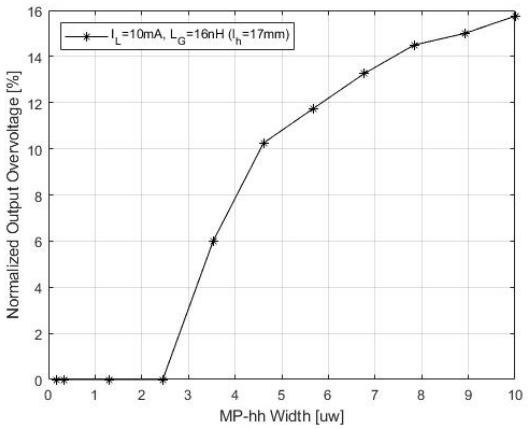

Figure 4 Magnitude of the overshoot affecting the HB output voltage (see the plot on the bottom in Fig. 2c) versus the W_{P-hh}.

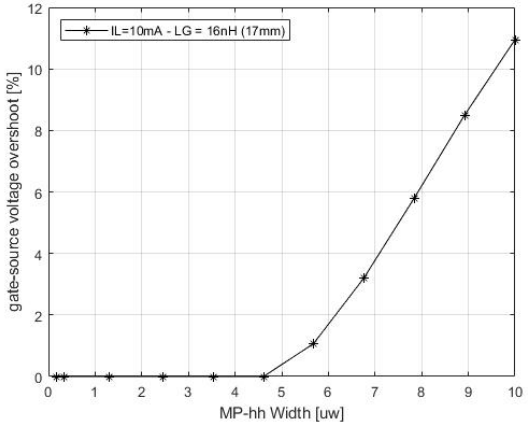

Figure 5 Normalized overshoot affecting the high side gate-source voltage at t_2 (see the plot on the top in Fig. 2a) versus the W_{P-hh}.

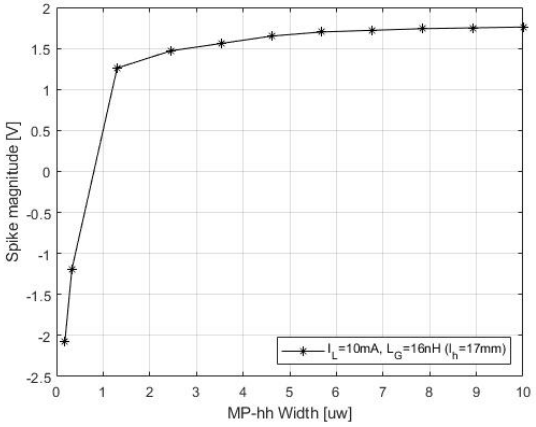

Figure 6 Magnitude of the spurious spike affecting the gate-source voltage of the low side transistor versus the W_{P-hh}.

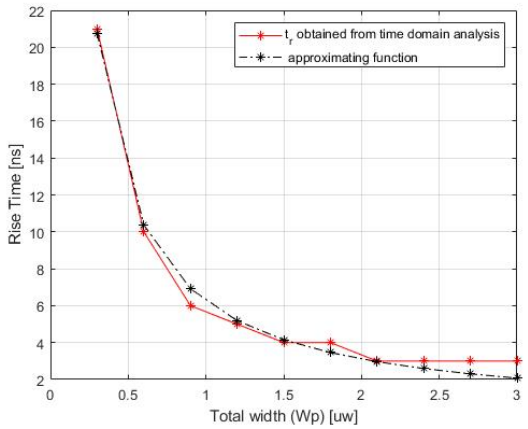

Figure 7 Rise time of the output voltage versus W_{P-hh} resulting form time domain analysis (red) and from a hyperbolic fitting (black).

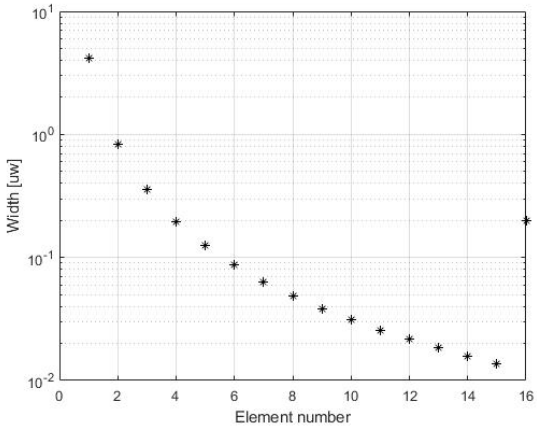

Figure 8 Width of the elementary transistor composing M_P resulting from the hyperbolic approximation.

sweep the rise time and the spike magnitude completely, the upper limit for W_{P-hh} can be set to 3 uw. This makes the overshoot affecting the output voltage (v_{ov}) and the high side gate-source voltage (v_{GS-ov}) negligible.
Finally, the simulations carried out on the HB highlighted that the dichotomous segmentation of the output transistors provides a coarse variation of t_r in the range $5-30$ ns, therefore magnitude of the spurious spike v_{sp} ranges from -2 V to 1.5 V, unless the number paralleled transistors is increased significantly. However, this would increase the gate driver complexity, significantly.
Similar considerations apply to the falling edge of the output voltage and are not included in the paper for brevity.

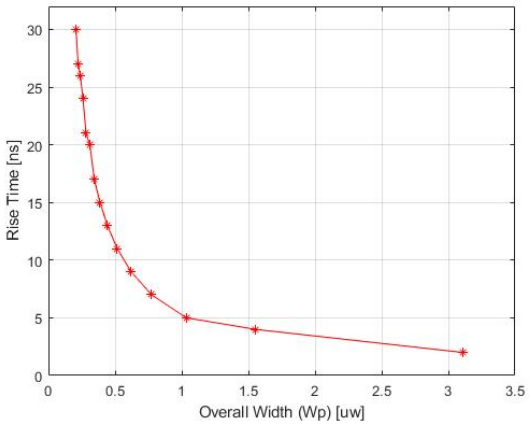

Figure 9 Rise time of the output voltage versus W_{P-hh}, as resulted from the time domain analysis of the HB comprising hyperbolic segmented gate drivers.

4 Hyperbolic Segmentation of the Output Transistors

Parametric simulations of the HB introduced in the previous section were repeated for W_{P-hh} in the range $0.18-3$ uw obtaining the rise time values shown in Fig. 7 (red line). The shape reminds a hyperbola branch, therefore the simulation results were fitted with the function $t_r = a/W_{P-hh}$ obtaining $a = 6.2uwps$. The cumulative value needed to get a uniform distribution of the rise time was calculated, then used to evaluate the width of each output transistor composing the main one ($M_{P,hh}$). The width of the sixteen (N=16) segments composing the output transistor are reported in Fig. 8. Such a hyperbolic segmentation of the output transistors allows one to obtain a uniform distribution of the rise time.
To check the effectiveness of the proposed approach, a new schematic comprising the HB used in the previous analysis and the hyperbolic segmented gate drivers was composed. Time domain analyses of the circuit were carried out to evaluate the rise time of the output voltage for rising values of W_{P-hh}, obtaining the points reported in Fig. 9.
Similarly, the magnitude of the spurious spike (V_{sp}) due to the fast switching of the output voltage was evaluated obtaining the points reported in Fig. 10. In both plots, most of the points drops in the high slope range, so that a fine regulation in the range of interest can be obtained with a reduced number of elementary transistors, thus reducing the complexity of the segmented gate driver.

5 Segmented Gate Driver

Based on the above, a gate driver implementing the hyperbolic segmentation of the output transistors was designed referring to a HV 130nm BCD technology. The design was tailored to drive e-mode GaN HEMTs featuring input capacitance of about 100 pF and voltage input range $-3,+6$ V. The block diagram of the hyperbolic gate driver is shown in Fig. 11. Both the high side (Mp) and the low side (Mn) are segmented. Mp is made up of 2^N elements, Mn of 2^M, where, N and M are the number of bits composing the respective configuration codes. Each elementary transistor is driven by a custom pre-driver, which in turn receives the switching command (pwm-h for the high side, pwm-l for the low side) from the dead time generator. The configuration input signals cfg-h and cfg-l allow

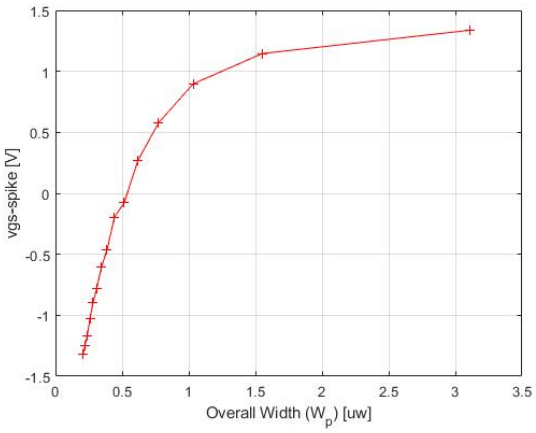

Figure 10 Magnitude of the voltage spike affecting the LS gate source voltage at t_2 versus the W_{P-hh}, as resulted from the time domain analysis of the HB comprising hyperbolic segmented gate drivers.

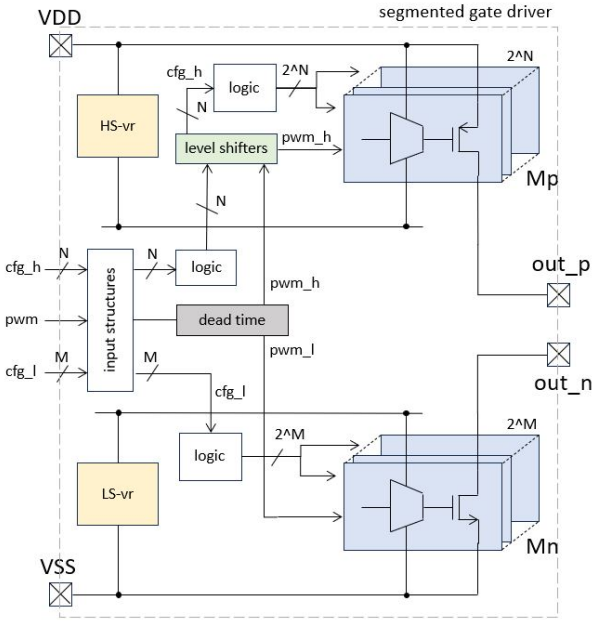

Figure 11 Block diagram of the IC implementing the hyperbolic segmented gate driver.

for enabling the switching output transistors. Two voltage regulators, HS-vr and LS-vr, provide the power supply to the high side and to the low side sections of the gate driver.

6 Conclusions

In this work the use of segmented gate drivers for a clean switching of HV e-mode GaN HEMTs was investigated. A half bridge comprising the power transistors, the respective gate drivers as well as the gate loops and the power loop stray inductances was considered. The time domain simulations showed that the oscillations affecting the drain-source and gate-source voltages at each switching as well as the spurious voltage spike affecting the gate-source voltage of the non-switching power transistor can be mitigated changing the driving strength of the gate drivers. This is obtained partitioning the gate driver output transistors in elementary ones connected in parallel, which can be selected by a configuration input code. The analysis carried out showed that the hyperbolic segmentation of such transistors allows for a fine control the overshoots, undershoots and oscillations affecting the drain-source and gate-source voltages of HV e-mode GaN HEMTs.

7 Literature

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