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12 September 2024

Efficient Saturation Control for Fully Differential Integrator in Continuous-Time Sigma-Delta Modulators

Matteo De Ferrari[1], Francesco Stilgenbauer[1][2], Edoardo Botti[2],
Cristiano Meroni[2], Paolo Crovetti[3], Edoardo Bonizzoni[1] and Piero Malcovati[1]
[1]Dept. of Electrical, Computer and Biomedical Engineering, University of Pavia, Pavia, Italy
[2]STMicroelectronics, Cornaredo (MI), Italy
[3]Dept. of Electronics and Telecommunications, Politecnico di Torino, Italy

***Abstract*—This paper presents an alternative approach to saturation control in an integrator, that occurs in Sigma-Delta modulators (ΣΔMs). This solution simplifies the design process with a 1.2-V power supply and consumes significantly less power than conventional saturation control methods. Additionally, this solution provides a good phase margin, that guarantees the stability, without requiring additional compensation techniques, and it has the added benefit of reducing the gain of the integrator as the system enters saturation, while also maintaining integrator inputs fixed at the proper common-mode voltage. This innovative approach offers a promising solution for efficient and stable saturation control in ΣΔM integrators, preventing distortion in the output signal, with potential applications in a wide range of electronic systems, such as audio systems. The circuit has been designed in a 90-nm CMOS technology.**

I. Introduction

Sigma-delta modulation is a widely used technique in modern audio processing, that enables high-resolution conversion of analog signals into the digital domain. This method involves a feedback loop that compares the input signal with the quantized output signal, resulting in a stream of high-frequency pulses that represent the original analog signal [1]. In the audio world, ΣΔMs are commonly used in digital audio processing applications, such as in car sound systems and playback, as well as in digital signal processing applications such as equalization and filtering.

One of the main advantages of ΣΔMs is their ability to achieve high resolution with relatively simple circuitry, making them ideal for use in audio applications where accuracy and precision are critical. Additionally, ΣΔMs are highly resistant to noise and other forms of interference, making them well-suited for use in challenging environments.

However, a common issue with this technique is the integrator overload, which occurs when the input amplitude approaches the modulator full-scale level and the quantizer is unable to accurately track the input signal. This can lead to distortion and other unwanted artifacts in the output power spectrum. In order to mitigate this problem, various techniques, such as those reported in [2]–[7], have been developed to address the saturation problem.

This paper reports an alternative solution to the problem of the integrator overload in ΣΔMs, which in audio amplifiers [8], [9], such as the one shown in Fig. 1 [8], can lead to saturation of the entire system. In these types of audio systems, a digital anti-windup control around the digital filter is not enough, as it is not able to deal with fast transients, and the system would still saturate. For this reason, a solution that is capable of following fast changes is proposed, which, despite the integrator output clamping, guarantees that the inputs remain at the common mode voltage, allowing the system to exit saturation more quickly. In this way the integrator remains within its linear range and the resulting audio signal is of high quality. Furthermore, this solution is different from the usual approaches, in which the integrator output signal is applied to the gate of a transistor to kill the integrator gain, or in which a non-linear input-output relationship with a "dead zone" is obtained using precision rectifiers based on operational amplifiers, such as in [10].

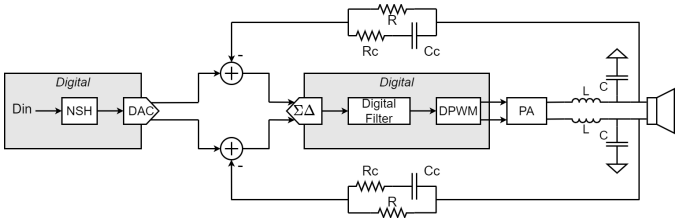

Fig. 1. Digital class-D audio amplifier

II. Saturation-Control Architecture

Fig. 2 illustrates the block diagram of the proposed solution, consisting of a fully-differential integrator with an additional saturation control block. For simplicity in this discussion, only the integrator is considered and not the entire ΣΔM, as the goal is to demonstrate, that despite having a fast input variation, causing the integrator to go into overload, its inputs remain fixed at the common-mode voltage. This helps ΣΔM-based systems, like the one shown in Fig. 1, to exit from saturation more quickly.

In this case, a current generator is used as a signal source for the integrator, as in the audio system shown in Fig. 1,

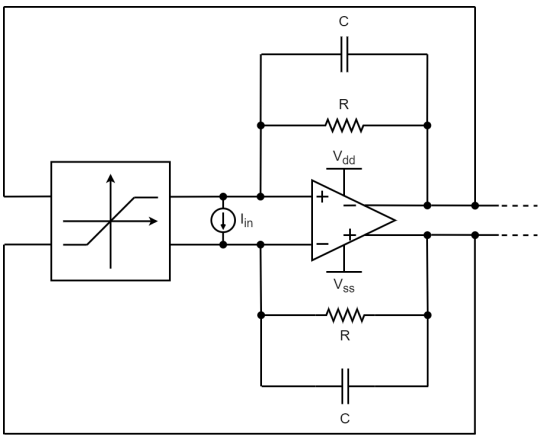

Fig. 2. Saturation-control architecture

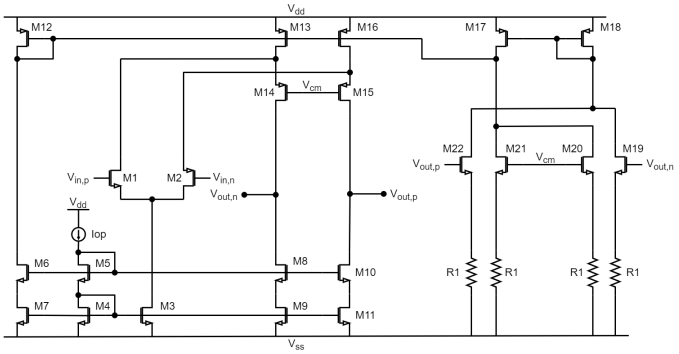

Fig. 3. Fully-differential operational amplifier schematic

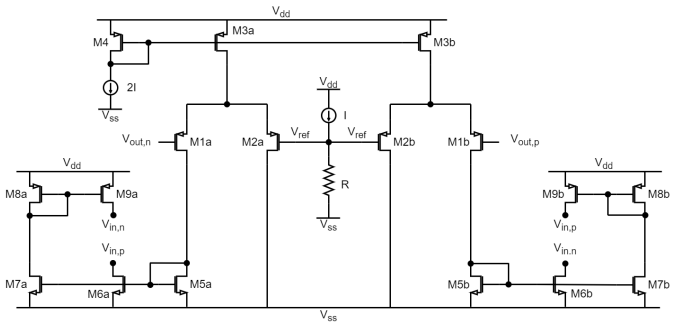

Fig. 4. Conventional saturation control scheme

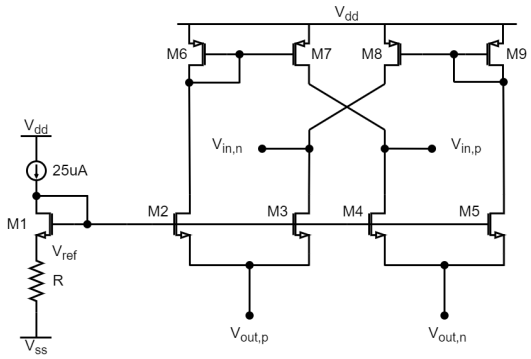

Fig. 5. Proposed saturation control scheme

the continuous-time ΣΔM receives at the input the difference between the feedback current and the audio signal produced by a current-mode D/A converter. The fully-differential operational amplifier is based on a folded-cascode topology with continuous-time common-mode feedback, as shown in Fig. 3. The common-mode feedback is designed to maintain the outputs at the common-mode voltage $V_{cm} = V_{dd}/2$. If the output common-mode voltage changes, the current flowing through M18 changes, bringing it back to the desired value. The gain of the folded-cascode operational amplifier is given by

$$A_1 \approx gm_{1,2}[((r_{ds16} \parallel r_{ds2})gm_{15}r_{ds15}) \parallel (gm_{10}r_{ds10}r_{ds11})] \quad (1)$$

In the conventional saturation-control solution, whose schematic is shown in Fig. 4, both integrator outputs are compared with a reference voltage V_{ref}, typically about 400 mV below V_{cm}. Whenever the positive or negative integrator output falls below V_{ref}, the saturation control circuit is activated and keeps the inputs fixed at V_{cm}. Assuming the positive output drops below V_{ref}, transistor M1b begins to pull current and the system becomes unbalanced. In this case, the current mirrored from M5b to M6b pulls down the negative input of the integrator, while the current mirrored in M9b through M8b pulls up the positive one. This causes the negative input to fall relative to the positive one, bringing the positive output of the integrator back up. Throughout this process, transistor M1a, M5a, M6a, M7a, M8a and M9a are drawing no current. By contrast, in the proposed saturation-control solution, whose schematic is shown in Fig. 5, the positive and negative outputs of the integrator are connected to the source of a transistors M2-M3 and M4-M5. respectively. Therefore, when the positive or negative output of the integrator approaches V_{ref}, transistors M2 and M3 or M4 and M5 reach value of V_{gs} that turns them on drawing a current approximately equal to I. Assuming, for example, that the positive output falls below V_{gs}, M2 and M3 turn on while M4 and M5 remain off. Current I is mirrored in M3, thus pulling down the negative input of the integrator, while the positive input is pulled up by M7, causing the positive output to rise again.

The proposed solution has several advantages over the conventional circuit. First of all it requires a smaller number of transistors, making it more suitable for low-voltage operation (1.2 V). Moreover, the conventional solution, excluding the branches required to generate V_{ref}, consumes significantly more power than the proposed one ($7I$ vs $2I$). Finally, in saturation conditions, with the proposed solution, the input resistance of the saturation-control circuit, which is connected to the output of the main operational amplifier, becomes $1/g_m$, thus reducing the open-loop gain of approximately 10 dB and, hence, making the approach of the integrator to saturation smoother.

In order to analyze the stability of the feedback loop associated with saturation control, the complete fully-differential circuit

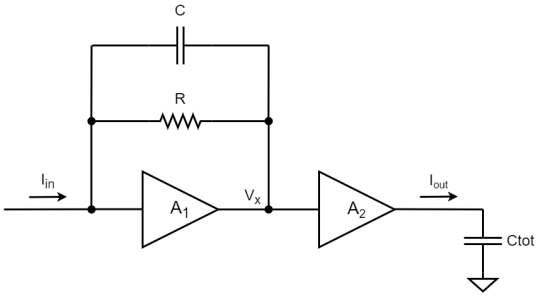

Fig. 6. Single-ended equivalent circuit of the saturation-control architecture

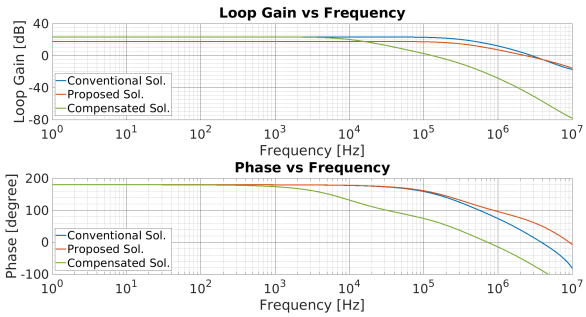

Fig. 7. Bode diagram of the saturation-control circuit loop gain

shown in Fig. 2 can be simplified, considering the single-ended equivalent circuit shown in Fig. 6, in which A_1 represents the folded-cascode operational amplifier, while A_2 models the gain associated to the saturation-control circuit. The transfer function from the input to the output of the integrator is

$$\frac{V_x}{I_{in}} = -\frac{A_1}{1 + A_1\beta} \tag{2}$$

where

$$\beta = -\frac{R}{1 + sCR} \tag{3}$$

The output current is then given by

$$I_{out} = V_x A_2 \tag{4}$$

As a result, the overall loop gain of the circuit turns out to be

$$G_{loop} = \frac{I_{out}}{I_{in}} = -A_1 A_2 \frac{1 + sCR}{1 + sCR + A_1 R} \tag{5}$$

Assuming $A_1\beta \gg 1$,

$$G_{loop} \approx A_2\left(\frac{1 + sCR}{R}\right) \tag{6}$$

If now we consider the actual fully-differential implementation, the loop gain becomes

$$G_{loop,FC} \approx 2 \cdot G_{loop} = 2A_2\left(\frac{1 + sCR}{R}\right) \tag{7}$$

where A_2, for the conventional and the proposed saturation-control solutions is given by

$$A_{2,c} \approx \left(\frac{g_{m,1A}g_{m,6A}}{g_{m,5A}} - \frac{g_{m,1B}g_{m,7B}g_{m,9B}}{g_{m,5B}g_{m,8B}}\right) \tag{8}$$

and

$$A_{2,p} \approx \left(g_{m,4} - \frac{g_{m,2}g_{m,7}}{g_{m,6}}\right) \tag{9}$$

respectively.

III. Simulations and Results

In order to verify the performance of the proposed saturation-control approach, the complete circuit shown in Fig. 2 has been simulated in the Cadence environment.

As a first analysis, we verified whether, under normal operating conditions (no saturation), the saturation-control circuit is actually completely turned off, in order to avoid worsening the linearity of the ΣΔM (any current injected by the saturation-control circuit at the input of the integrator would be seen as a disturbance by the ΣΔM). In this respect, the choice of the correct value of V_{ref} is of paramount importance. In the proposed circuit we selected a value of V_{ref} about 400 mV lower than V_{cm}, resulting in a saturation-control circuit output current of the order of pA under normal operating conditions. Fig. 7 shows the open-loop gain achieved in simulation for the convention and the proposed solutions. It is evident that, with the same value of V_{ref}, the DC gain is almost the same, but the proposed solution had a phase margin ($\approx 70°$) that ensures stability, while for the conventional solution ($\approx 18°$) this is not the case. This is due to the fact that, the conventional solution (Fig. 4), due to the larger number of branches, introduces an additional phase shift that significantly deteriorates the phase margin. This is also confirmed by the simulation shown in Fig. 8, which illustrates the closed-loop gain achieved with both solutions. With the conventional approach, a resonance peak appears around 200 MHz. The proposed solution remains stable even if V_{ref} is changed in the range 350-450-mV, to guarantee better flexibility. Indeed, a variation of the reference voltage leads to a phase margin variation, but only as large as a few degrees. On the other hand, with the conventional solution, this is not the case and the circuit becomes unstable. Form the results shown in Fig. 7, it is clear that the proposed solution is inherently compensated and achieves a good phase margin under any operating conditions, while the conventional solution requires additional compensation to achieve a phase margin around 60°. This can be achieved by introducing an RC network between the differential outputs of the integrator and the gates of transistors M1a and M1b. From various analyses, it emerged that the optimal case for achieving the correct phase margin is to introduce a dominant pole at 10^4 Hz, with values of R_c = 100 kΩ and C_c = 150 pF. As it can be observed from Fig. 7, the curves achieved with compensation feature a phase that guarantees stability, but this comes at the cost of area (two resistors and two capacitors) and a slightly reduced bandwidth compared to the proposed solution.

Finally, the complete saturation-control circuit (Fig. 2) was simulated in transient to verify that, in the event of an input signal variation that would drive the system into saturation, the differential inputs of the integrator actually remain fixed

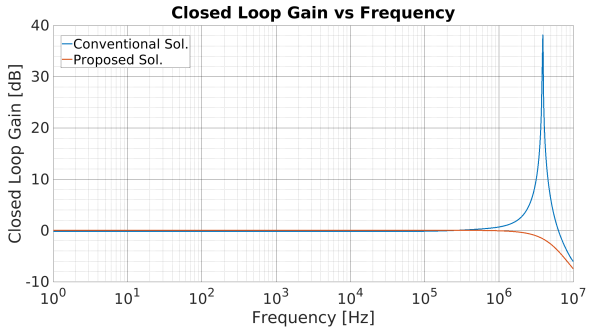

Fig. 8. Closed-loop gain vs frequency

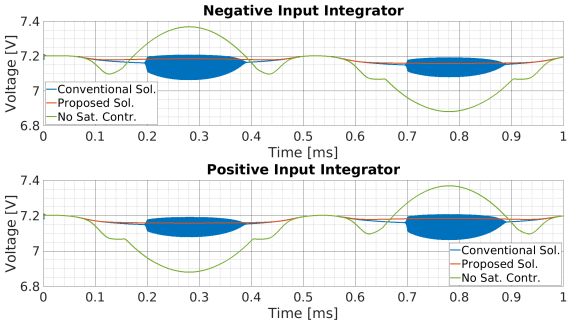

Fig. 9. Transient simulation of negative and positive inputs of the integrator

at V_{cm}. The results are summarized in Fig. 9, in which it can be observed that without saturation-control circuit, the input of the integrators diverge, while with the saturation control-circuit (both conventional and proposed solutions), they remain close to V_{cm}. This is important, as if the system goes into overload but the differential inputs of the integrator remain fixed, no current flows into the integrator capacitance ($i = C\frac{dv}{dt}$), allowing the system to exit the saturation condition more quickly.

From Fig. 9, it can also be observed that with the proposed solution, the differential inputs of the integrator are stable at V_{cm}, while with the conventional solution, they feature an overshoot that causes small oscillations around V_{cm}. This oscillation at a frequency of about 3-MHz is due to the poor phase margin of the conventional solution, which leads to a resonance peak. Finally, Fig. 10 shows the differential output signal of the integrator in transient conditions. Without saturation-control circuit the output signal diverges, while, with the saturation-control circuit, the output signal is correctly clamped to V_{DD} or V_{SS}, showing, however, again an oscillation with the conventional solution, which is not present with the proposed one.

IV. Conclusions

In this paper an analog saturation-control circuit for preventing overload in ΣΔM integrators is proposed. The circuit guarantees that under overload conditions, the inputs of the operational amplifier used in the integrator are maintained at the common-mode voltage. This allows the system to

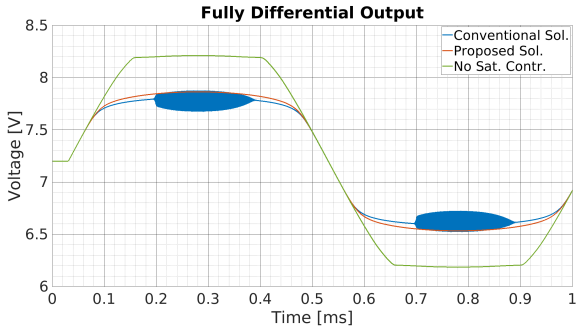

Fig. 10. Fully differential outputs transient response.

exit the saturation condition more quickly, improving the performance of audio systems. Furthermore, compared to conventional saturation-control solutions, the proposed circuit is characterized by lower complexity and significantly lower power consumption. Moreover, it is suitable for operating at low power supply voltage (1.2 V). The proposed solution also lowers the integrator gain in saturation condition saturation condition, making the return to normal operation easier. Finally, the proposed solution inherently provides a good phase margin without requiring any compensation networks, that would cost in terms of area and bandwidth. The large phase margin achieved allows changing the threshold voltage for saturation detection without causing overshoots nor instability. The circuit has been designed at transistor-level and thoroughly simulated using a 90-nm CMOS technology.

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