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Fast Prediction of Worst-Case Voltage Droops in Power Distribution Networks

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***Abstract*—Building on well-known system theoretical results, simple numerical tools are introduced for the evaluation of the worst-case voltage droops in Power Distribution Networks (PDN), in various Power Integrity verification scenarios. Given a PDN model and suitable bounds on load current values and slew rates, the proposed approach provides an explicit bound of the worst-case voltage droop, as well as the particular input current waveforms that produce it. Validations are provided based on two realistic PDN models.**

I. Introduction

Power Integrity (PI) verification of any modern computing system is a mandatory step for ensuring proper functioning under practical workload conditions [1], [2]. Here we consider a typical Power Distribution Network (PDN) structure that connects a platform Voltage Regulator Module (VRM) to each individual logic block in one or more microprocessors, by means of a complex interconnect network routed through board-package-chip, including suitable sets of decoupling capacitors [3]. No particular system topology is required, so that the proposed approach is also applicable to heterogeneous integrated systems [4], provided that the PDN behavior can be represented as a Linear Time Invariant (LTI) system.

The methodology described in this document applies to both concept (pre-layout) studies but especially to post-layout verification, where all PDN parts are defined and a final verification needs to be performed in order to verify that the voltage levels at all prescribed locations are within allowed bounds. Such verification is typically performed through costly transient simulations that compute all voltage waveforms given a set of loading current stimuli. Of course, such simulations inevitably require accurate models for all PDN structures and components. In this work, we propose a systematic approach that produces a reduced amount of information, namely only the largest voltage droop that a generic multiport PDN will be able to produce under a variety of operating conditions that are relevant in applications, together with the particular loading current pattern that produces it. This work extends and generalizes [5], [6], which demonstrated how to systematically build the worst-case stimulus under finite rise-time constraints for single-port PDNs.

No transient simulation is required, but only the application of a number of well-known system theoretical bounds on signal and operator norms. The viability of the approach is enabled by the application of established rational macromodeling techniques. These techniques provide a closed form approximation of the PDN impedance matrix in terms of a Linear Time Invariant (LTI) system, also when the underlying structure can be hardly characterized in terms of a physics-based lumped equivalent. Furthermore, in case active or switching components enter the design (e.g. as integrated voltage regulators, see [2]), the method can still be proficiently applied for PI verification, as long as the linearized PDN impedance provides a representative performance indicator. Our results show that the availability of a surrogate with LTI structure can provide meaningful information about the reliability of the underlying design even without relying on equivalent circuit-based transient simulations.

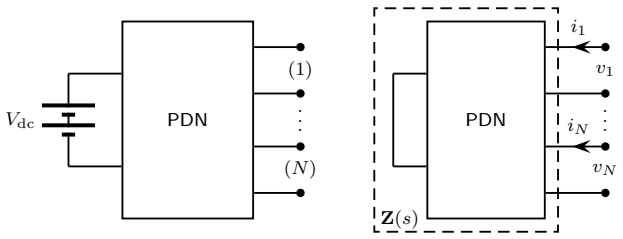

Fig. 1. Schematic illustration of a PDN (left) with definition of ports and output impedance matrix (right).

II. Formulation

Let us consider the high-level PDN block description depicted in Fig. 1, where the entire PDN structure is represented in the $(N+1)$-port $\mathbf{H}(s)$, and where the N output ports correspond to loading points subjected to independent current stimuli. In this work we assume that the nominal (DC) solution is subtracted so that the DC voltage source is replaced by a short circuit, and both current stimuli $i_j(t)$ and output port voltages $v_j(t)$ represent (small-signal) variations around the nominal operating point. Note that this scenario includes also locally regulated PDNs by means of banks of Integrated Voltage Regulators (IVRs), as far as a small-signal description of the closed-loop (regulated) output impedance applies. In the following, we collect all port currents and voltages in vectors $\boldsymbol{i}(t)$, $\boldsymbol{v}(t)$, respectively. With the above assumptions, the voltage signals are obtained as

$$\boldsymbol{v}(t) = \int_0^t \mathbf{z}(\tau)\boldsymbol{i}(t-\tau)d\tau = (\mathbf{z}\star\boldsymbol{i})(t), \quad \boldsymbol{V}(s) = \mathbf{Z}(s)\boldsymbol{I}(s)$$

in the time and Laplace domain, respectively, where $\mathbf{z}(t)$ is the impulse response matrix corresponding to the output impedance matrix $\mathbf{Z}(s)$. Note that since currents are defined as entering the PDN, the corresponding voltages represent droops with respect to the nominal output voltage. In the following, we analyze various scenarios starting from the simplest case of a single output port $N = 1$. This case serves to introduce the main results and to set notation.

A. The unconstrained single-port case

Let us assume a single-port PDN with $N = 1$. The port voltage $v(t)$ and current $i(t)$ are related by a scalar convolution integral $v(t) = (z \star i)(t)$. We are interested in the worst-case value $V_{\max} = \max_{t\geq 0} v(t)$ that can be attained by the voltage, given a constraint on the maximum amplitude of the load current. Two types of constraints can be considered

$$|i(t)| \leq I_{\max} \tag{1a}$$

$$0 \leq i(t) \leq I_{\max} \tag{1b}$$

where (1b) is more realistic for PI applications than (1a) given that current stimuli are necessarily unidirectional.

Considering (1a), we see that

$$|v(t)| \leq \int_0^t |z(\tau)| \cdot |i(t-\tau)| d\tau \leq I_{\max} \int_0^t |z(\tau)| d\tau. \tag{2}$$

By extending the integration limit to $t \to \infty$ we obtain the well-known bound [5], [7] for the worst-case voltage droop

$$V_{\max,\infty} = I_{\max} \int_0^\infty |z(\tau)| \, \mathrm{d}\tau = I_{\max} ||z||_1 \tag{3}$$

in terms of the L_1 norm of the impulse response. On a finite interval $[0, t]$ the worst case is achieved by choosing the excitation

$$i_{\mathrm{w},\infty}(t-\tau) = I_{\max} \operatorname{sign}\{z(\tau)\}, \tag{4}$$

which is basically a sequence of ideal (positive and negative) steps placed at the zeros of the time-reversed impulse response, centered at time t, and scaled to an amplitude equal to the limit current. This input makes the first inequality in (2) an equality since the convolution integrand becomes nonnegative.

The constraint (1a) gives a similar result,

$$V_{\max,+} = I_{\max} \int_0^\infty |z(\tau)|_+ \, \mathrm{d}\tau \tag{5}$$

where $|x|_+$ is equal to x if $x \geq 0$ and is 0 otherwise. Since $|x|_+ = \frac{1}{2}(|x| + x)$, we have

$$V_{\max,+} = \frac{V_{\max,\infty} + I_{\max} Z_{\mathrm{dc}}}{2}$$

where $Z_{\mathrm{dc}} = Z(0) = \int_0^\infty z(\tau) d\tau$ is the input impedance at DC ($f = 0$). In this situation, the finite time worst case current stimulus results

$$i_{\mathrm{w},+}(t-\tau) = \frac{1}{2} I_{\max} (\operatorname{sign}\{z(\tau)\} + 1), \tag{6}$$

namely a shifted version of (4) attaining values $I_{\max}$ or 0.

B. Single-port with slew rate constraints on load currents

In practical systems, any load current step is not instantaneous but is characterized by a maximum slew rate, in fact equivalent to a bound $\Delta_{\max}$ on the local derivative of $i(t)$

$$\left| \frac{di(t)}{dt} \right| \leq \Delta_{\max}, \tag{7}$$

which for a step transition $0 \leftrightarrow I_{\max}$ implies a finite rise time $\tau_r \geq I_{\max}/\Delta_{\max}$. This constraint is not compatible with the worst-case stimuli (4) or (6), which are locally discontinuous. A derived input signal that fulfils (7) can be readily obtained as the convolution

$$\hat{\imath}_{w,\nu}(t) = (i_{w,\nu} \star g_{\tau_r})(t) \tag{8}$$

with $\nu = \{\infty, +\}$ and where $g_{\tau_r}(t)$ is a unit-area square pulse having width τ_r. The contribution of this smoothing filter can be embedded in the system transfer function as

$$\hat{Z}(s) = Z(s) G_{\tau_r}(s), \quad G_{\tau_r}(s) = \frac{1 - e^{-s\tau_r}}{s\tau_r}.$$

Applying the procedure of Sec. II-A to $\hat{z}(t) = \mathcal{L}^{-1}\{\hat{Z}(s)\}$ will result in a worst-case current excitation in form (4)-(6), that when subjected to the smoothing operator (8) will produce an excitation $\hat{\imath}_{w,\nu}(t)$ with finite rise time for the PDN impedance $Z(s)$. This signal is only an approximation of the true worst-case finite-derivative input discussed in [6], whose construction is however more involved.

C. Multi-port case, identical stimuli

Extension to the multiport $N > 1$ case with the constraint of identical and synchronous inputs is straightforward. This scenario is typical in voltage droop verification at multiple ports of a single microprocessor core, assuming a unique switching pattern of all loads. In this case, the input current vector can be expressed in terms of a single scalar excitation as $\boldsymbol{i}(s) = \mathbf{1}\, i(t)$, the vector of output voltages is readily obtained as $\boldsymbol{V}(s) = \mathbf{Z}(s) \cdot \mathbf{1} I(s) = \boldsymbol{Z}_c(s) I(s)$ with $\boldsymbol{Z}_c(s)$ denoting the column sum of the impedance matrix. Application of the procedure of Sec. II-A or II-B to each element of $\boldsymbol{z}_c(t) = \mathcal{L}^{-1}\{\boldsymbol{Z}_c(s)\}$ leads to the worst-case current excitation and to an array of corresponding worst-case voltage droops, from which the largest is trivially computed.

D. Multi-port case, quasi-synchronous switching

A more realistic situation occurs when the same switching pattern is applied with port-dependent delays τ_j. In such scenario one can write $\boldsymbol{I}(s) = \boldsymbol{T}(s) I(s)$ where $\boldsymbol{T}(s)$ is a $N \times 1$ vector with components $e^{-s\tau_j}$. Also in this case we can embed in the impedance elements all delays as $\boldsymbol{Z}_T(s) = \mathbf{Z}(s) \cdot \boldsymbol{T}(s)$, resulting in $\boldsymbol{V}(s) = \boldsymbol{Z}_T(s) I(s)$. All above derivations extend to this case by processing $\boldsymbol{z}_T(t) = \mathcal{L}^{-1}\{\boldsymbol{Z}_T(s)\}$.

E. General multi-port case

In the general multi-port case with all input currents considered as independent stimuli, we have

$$v_i(t) = \sum_{j=1}^{N} \int_0^t z_{ij}(\tau) i_j(t-\tau) d\tau, \quad 0 \le i_j(t) \le I_{j,\max}.$$

Similarly to (2), we can write

$$|v_i(t)| \le \sum_{j=1}^{N} \int_0^t |z_{ij}(\tau)| \cdot |i_j(t-\tau)| d\tau \le \sum_{j=1}^{N} I_{j,\max} ||z_{ij}||_1$$

where the worst-case is obtained by processing each component of the impulse response matrix as in Sec. II-A or Sec. II-B. Note that in this situation the worst-case signal and voltage droop may depend on the particular port i that is observed.

F. Practical evaluation of the L_1 norm

Evaluation of worst-case droops in all above-described scenarios requires the computation of the L_1 norm of some impulse response $h(t)$, whereas the determination of the corresponding worst-case input signals involves finding all zeros of $h(t)$. In this work, we propose to perform the above operations based on a closed form approximation of the impulse response of interest, obtained via frequency domain rational macromodeling. Specifically, we assume that a characterization for the PDN impedance matrix $\mathbf{Z}(s)$ is available in terms of frequency samples $s_k = \mathrm{j}\omega_k$ retrieved within a finite bandwidth $\omega_k \in \Omega = [0, \omega_{\max}]$. These samples are used to drive the Vector Fitting iteration [8], which returns a closed form rational approximation $\tilde{\mathbf{Z}}(s)$ of the PDN impedance matrix and an associated state-space realization

$$\tilde{\mathbf{Z}}(s) = \mathbf{C}\,(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} \approx \mathbf{Z}(s),$$

together with the corresponding PDN impulse response

$$\tilde{\mathbf{z}}(t) = \mathcal{L}^{-1}\{\tilde{\mathbf{Z}}(s)\} = \mathbf{C}\, e^{\mathbf{A}\, t}\, \mathbf{B} \approx \mathbf{z}(t). \tag{9}$$

The same modeling strategy can be applied to obtain approximations of the functions $\tilde{\mathbf{Z}}(s)$, $\mathbf{Z}_c(s)$ and $\mathbf{Z}_T(s)$ and of the corresponding impulse responses, as defined in Sec. II-B–II-D.

Once a closed form approximation of a given $h(t)$ is obtained via macromodeling, the L_1 norm can be estimated, e.g., using the algorithm introduced in [9]. Alternatively, numerical integration routines can be directly applied to the impulse response (9) to compute (3) or (5). The worst-case inputs (4) or (6) are obtained from the zeros of the impulse response.

III. Numerical verification

The proposed approach is illustrated on two test cases. The first is a template PDN structure with $N = 9$ output ports, which includes only passive interconnect models loaded with a suitable set of decoupling capacitors. Selected output impedance responses are depicted with the corresponding rational macromodel responses in Fig. 2. The three panels of Fig. 3 depict the worst-case bound for the voltage droop and the actual response to the worst-case stimulus, for three

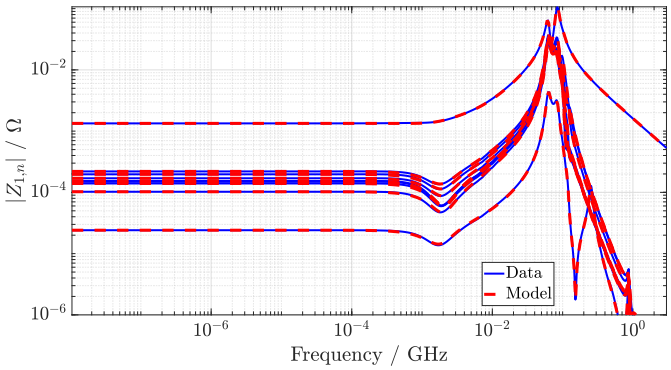

Fig. 2. Template PDN: comparison between VF model and impedance data samples.

different verification scenarios: identical stimuli at all ports (Sec. II-C, panel (a)); real worst-case with independent worst-case excitation at all ports (Sec. II-E, panel (b)); and independent worst-case excitation at all ports with finite rise time (5 ns) for all input transitions (realized as in Sec. II-B, panel (c)). All three panels show that the actual response reaches the worst-case bound in finite time. Note that the bounds are in fact different for different scenarios, the largest value corresponding to the unconstrained case ($V_{\max,+} = 274\,\mathrm{mV}$). Adopting a finite rise time constraint has the effect of lowering the worst-case droop ($V_{\max,+} = 209\,\mathrm{mV}$) due to the low-pass filtering effect of the smoothing operator g_{τ_r}.

The second example is a simplified PDN model of an actual product, namely a high-end server platform whose details are found in [2]. For present analysis we selected a portion of the PDN corresponding to a single core with a total of $N = 10$ loading ports. The PDN is locally regulated through a bank of per-core multiphase Fully Integrated Voltage Regulators (FIVRs) equipped with suitable output voltage sensing circuitry and associated feedback compensators. The PDN interconnect at board and package level are modeled through full-wave solvers and cast as rational macromodels through Vector Fitting. The PDN is completed by inductor models and MIM capacitance models for the FIVR part, and by the full set of decoupling capacitors.

For present analysis, we consider the closed-loop (regulated) output impedance linearized around the nominal operating point. One representative element of this impedance is depicted in Fig. 4 with the corresponding rational macromodel response. Figure 5 depicts the worst-case bound $V_{\max,+}$ assuming a maximum current excitation of 1 A/port, with no constraints on the input waveforms. One representative worst-case current stimulus is depicted by the red line, which as expected is given by a sequence of transitions between zero and $I_{\max}$ occurring at the impulse response zeros. The blue line depicts the actual voltage droop response at the same port, which attains the worst-case bound in finite time, as expected.

In terms of runtime, the evaluation of the worst-case voltage droops through numerical L_1 norm estimation was achieved for the two test cases in 7 and 30 seconds, respectively.

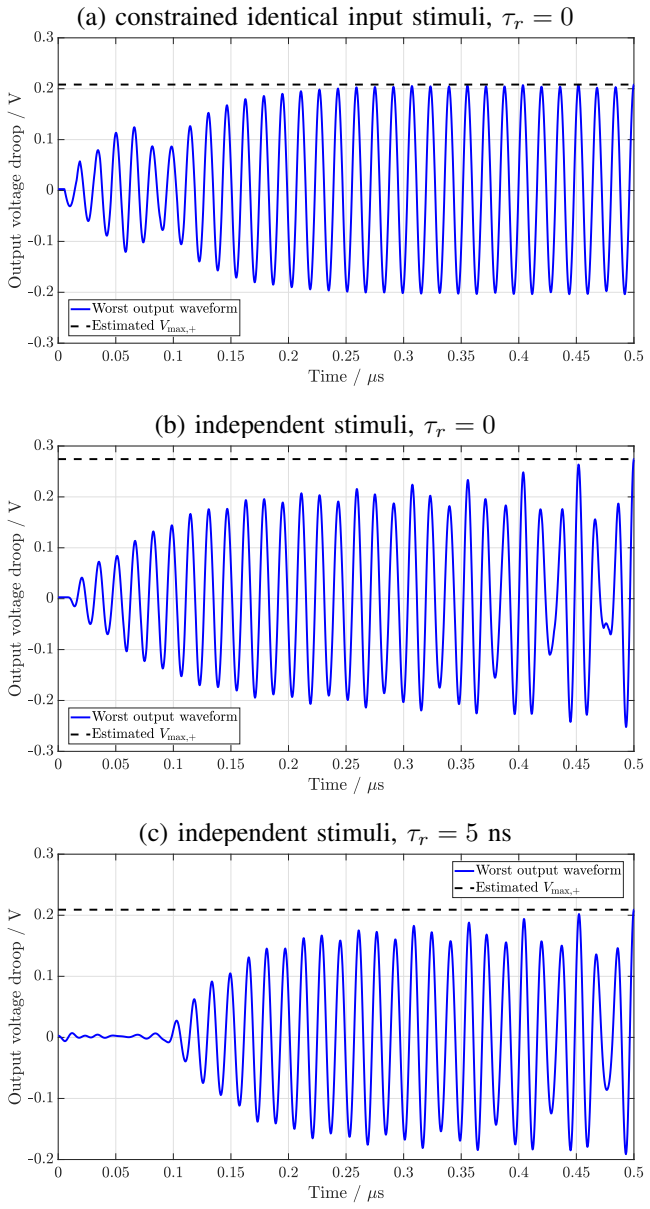

Fig. 3. Template PDN: worst-case voltage droop bound $V_{\max,+}$ (dashed black line) and a selected voltage droop port response (blue line). In all cases the maximum current of all ports is set to 10 A.

IV. Conclusions

A simple methodology for estimating the worst-case voltage droop in PDN models was proposed, which does not require any transient simulation. The estimation is performed through a numerical evaluation of the L_1 norm of a suitably defined set of impulse responses. The latter depend on the particular scenario of interest for Power Integrity verification. The runtime required for the estimation is negligible with respect to any realistic transient analysis. As a byproduct, the proposed method also produces a set of input current stimuli that, when applied to the PDN, induce a voltage droop waveform that reaches the worst-case bound in finite time. A verification was demonstrated on two different PDN testcases.

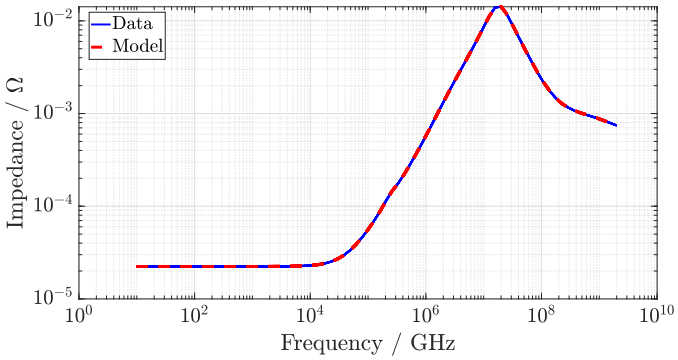

Fig. 4. Server PDN model: comparison between sampled impedance and fitted VF model.

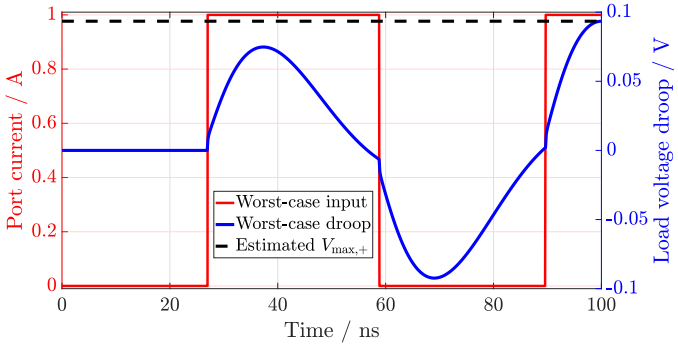

Fig. 5. Server PDN: worst case input (red line, left axis labels) and corresponding response (blue line, right axis labels) for a single-core example with 10 load ports. The maximum current is set to 1 A/port.

References

[1] M. Swaminathan, D. Chung, S. Grivet-Talocia, K. Bharath, V. Laddha, and J. Xie, "Designing and modeling for power integrity," *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 2, pp. 288–310, May 2010.

[2] A. Carlucci, T. Bradde, S. Grivet-Talocia, S. Mongrain, S. Kulasekaran, and K. Radhakrishnan, "A compressed multivariate macromodeling framework for fast transient verification of system-level power delivery networks," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 13, no. 10, pp. 1553–1566, Oct 2023.

[3] K. Radhakrishnan, M. Swaminathan, and B. K. Bhattacharyya, "Power delivery for high-performance microprocessors—challenges, solutions, and future trends," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 4, pp. 655–671, 2021.

[4] "Heterogeneous integration roadmap," 2021 Edition. [Online]. Available: https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html

[5] V. Drabkin, C. Houghton, I. Kantorovich, and M. Tsuk, "Aperiodic resonant excitation of microprocessor power distribution systems and the reverse pulse technique," in *2002 IEEE 11th Topical Meeting on Electrical Performance of Electronic Packaging*, 2002, pp. 175–178.

[6] W. Reinelt, "Maximum output amplitude of linear systems for certain input constraints," in *Proceedings of the 39th IEEE Conference on Decision and Control*, vol. 2, 2000, pp. 1075–1080.

[7] C. A. Desoer and M. Vidyasagar, *Feedback systems: input-output properties*. SIAM, 2009.

[8] S. Grivet-Talocia and B. Gustavsen, *Passive Macromodeling: Theory and Applications*. New York: John Wiley and Sons, 2016.

[9] N. K. Rutland and P. G. Lane, "Computing the 1-norm of the impulse response of linear time-invariant systems," *Systems & Control Letters*, vol. 26, no. 3, pp. 211–221, 1995.