Modeling the Impact of Fabrication Variabilities on the Performance of Silicon Avalanche Photodetectors

Modeling the Impact of Fabrication Variabilities on the Performance of Silicon Avalanche Photodetectors

David Liu, Luca F. Errico, Matteo G. C. Alasio, *Member, IEEE*, Mike Zhu, and Enrico Bellotti, *Senior Member, IEEE*

***Abstract*—This work presents a systematic study of the sensitivities of silicon avalanche photodiode (APD) performance metrics, including gain, excess noise, and bandwidth, to potential variabilities in the fabrication process. The APDs simulations are performed using a state-of-the-art Full-Band Monte Carlo (FBMC) device simulator with the integrated band structure and scattering rates calculated $ab-initio$ with density-functional theory (DFT). The focus of this work is placed on the performance of CMOS-compatible lateral transport separate-absorber-multiplier APDs (SAM APDs) fabricated on an SOI layer. The FBMC material models are validated against experimental data for carrier velocities and impact ionization coefficients, in addition to the reported APD performance of a germanium-on-silicon (Ge-on-Si) separate-absorber-charge-multiplier APD (SACM APD). The fabrication variations considered for the SAM APD include slight variations to the doping concentration and physical dimensions of the multiplier and absorber regions, as well as the thickness of the SOI layer. The results show that fabrication variations may have significant effects on the gain of the APD, but minimally affect the excess noise factor and bandwidth of the devices.**

***Index Terms*—Silicon photonics, avalanche photodetector, silicon APDs, lateral avalanche photodetector, integrated optoelectronics.**

I. Introduction

THE ability to detect with high sensitivities in low light conditions is of utmost importance for a diverse range of applications, including fiber optic communications [1], [2], [3], LiDAR [4] and Quantum Key Distribution (QKD) [5], [6]. For each, avalanche photodetectors (APDs) have been successfully employed as the primary detectors to meet the sensitivity and responsivity requirements [7], [8], [9]. Silicon is a desirable material for APDs due to its ability to detect a wide range of wavelengths, ranging from ultra-violet (UV) to near-infrared (NIR), and has demonstrated desirable multiplication properties [8], [10], [11], [12], [13], [14], [15]. Its desirable multiplication properties have also motivated its use as the multiplier material for infrared heterojunction APDs, such as Ge-on-Si [11], [12], [13], [16], or GeSn-on-Si [17] photodetectors. Other advantages of silicon-based APDs (SiAPDs) include monolithic integration with read-out integrated circuitry and compatibility with the CMOS fabrication infrastructure [18], [19], which promote high yield and high pixel densities [20].

The desirable multiplication properties of silicon are mainly attributed to its low ionization coefficient ratio (k-ratio). Modern sub-micrometer thick multiplication layers have demonstrated a low effective k-ratio of approximately 0.1 [11], [12], [13], [14]. Having a k-ratio in this range is preferable for maintaining a low excess noise factor at high gain [21], which allows the APDs to reach high detection sensitivities. Furthermore, a low k-ratio also promotes high gain-bandwidth product due to the decreased "avalanche build-up effect" [22].

Although silicon has demonstrated its promise as a multiplier material, sharp electric field profiles induced by the high doping values, and small physical dimensions of sub-micrometer scale APDs have created challenges in attaining consistent device performance. For example, some fabrication facilities account for small dimensional variations incurred by process variation to minimize the effects on device-to-device performance [23]. For APDs, the variation in performance is primarily attributed to the sensitivity of the carrier multiplication process to the local electric field. Carriers within these sharp high field regions will be rapidly energized by the field, and carriers with energies in excess of the bandgap may impact ionize. However, the small dimensions of the sharp high-field regions limit where carriers can multiply. Thus, small variations in the high-field regions, including variations in its magnitude and dimensions, may significantly affect the performance metrics of APDs [14], [24], [25].

In this work, we investigate how potential variabilities in the fabrication process, including changes to the physical dimensions and doping values, may impact the performance of silicon separate-absorber-multiplier (SAM) APDs. The APD is fabricated on a silicon-on-insulator (SOI) film, using conventional CMOS techniques to form the device structure and implement the doping profiles. The baseline geometry used to benchmark the performance is inspired by literature [8]. Understanding how

Manuscript received 22 January 2024; revised 12 March 2024; accepted 17 April 2024. Date of publication 24 April 2024; date of current version 13 May 2024. This work was supported by the U.S. Army Research Laboratory under Award W911NF-23-2-0090 managed by Dr. J. Schuster, in part by U.S. Army Research Laboratory through the Center for Semiconductor Modeling under Grant W911NF-18-2-0027, managed by Dr. M. Reed and Dr. J. Schuster, in part by DoD HPC Systems and the 2019 Army Research Office DURIP Award under Grant W911NF-19-1-0161, and in part by DoD HPC Modernization Program. *(Corresponding author: Matteo G. C. Alasio.)*

David Liu, Luca F. Errico, Mike Zhu, and Enrico Bellotti are with the Department of Electrical and Computer Engineering, Boston University, Boston, MA 02215 USA (e-mail: liudavid@bu.edu; lerrico@bu.edu; mjzhu@bu.edu; bellotti@bu.edu).

Matteo G. C. Alasio is with the Dipartimento di Elettronica e Telecomunicazioni, Politecnico di Torino, 10129 Torino, Italy (e-mail: matteo.alasio@polito.it).

Digital Object Identifier 10.1109/JPHOT.2024.3393366

fabrication variations affect performance metrics will help guide the fabrication of these APDs, and ensure that they meet the required specifications.

The APD performance metrics of gain, excess noise factor, and bandwidth are simulated using a full-band Monte Carlo (FBMC) device simulator. Due to its inclusion of the full band-structure of silicon, the FBMC is well-suited for simulating high-field transport phenomena [26]. Compared to the drift-diffusion method, which does not account for carrier energies and treats impact ionization phenomenologically, carriers in FBMC simulations respect the bandstructure of the material and only impact ionize when the carrier reaches sufficient energies. Furthermore, its inclusion of stochastic scattering models allow it to simulate noise. Finally, Monte Carlo has also demonstrated effectiveness in simulating short-channel effects, such as velocity overshoot, which may not be captured by other simulation methodologies. Thus the physical accuracy of the FBMC method make it well-suited for accurate simulations of APDs.

This paper is structured as follows: Section II describes our methodologies, including the Full Band Monte Carlo Model (Section II-A), device simulations (Section II-B), device structures (Section II-C), and the fabrication variations explored (Section II-D). Section III presents our findings covering the gain characteristics (Section III-A), excess noise factor, and the impulse response and bandwidth of the devices, highlighting their dependence on device geometry and doping. The paper concludes with a summary of these findings and their implications for the design and fabrication of silicon APDs.

II. Methods and Device Structures

A. Full Band Monte Carlo Model

The simulations presented in this work have been performed using the three-dimensional full-band Monte-Carlo code FBMC3D developed at Boston University [27], [28]. The description of the material is based on an *ab-initio* model of full-band structure and scattering rates of silicon obtained using density function theory (DFT) and hybrid functionals (HSE). A detailed description of the simulation methodology can be found in our previous work [29]. All the simulations' results have been obtained for an operating temperature of 300 K. Silicon carrier-phonon interaction is described using *effective* scattering rates, which have been calibrated to match *ab-initio* calculated values by scaling with a deformation potential. A comparison between *effective* and *ab-initio* scattering rates for acoustic and optical phonons is shown in Fig. 1.

The carrier velocity-field curves obtained using the *ab-initio* electronic structure and *effective* scattering rates are shown in Fig. 2. Electrons and holes velocities were computed for applied electric fields in the $\langle 100 \rangle$ and $\langle 111 \rangle$ crystallographic directions and are compared to the available experimental values [30], [31], [32]. The numerical results are well aligned in both low and high electric fields. Furthermore, the simulated results exhibit the same anisotropy observed in the experimental data, with velocities in the $\langle 111 \rangle$ slightly higher than $\langle 100 \rangle$ for electrons above $5 \times 10^3\,\mathrm{V\,cm^{-1}}$ and slightly lower than $\langle 100 \rangle$ for holes above $2 \times 10^4\,\mathrm{V\,cm^{-1}}$.

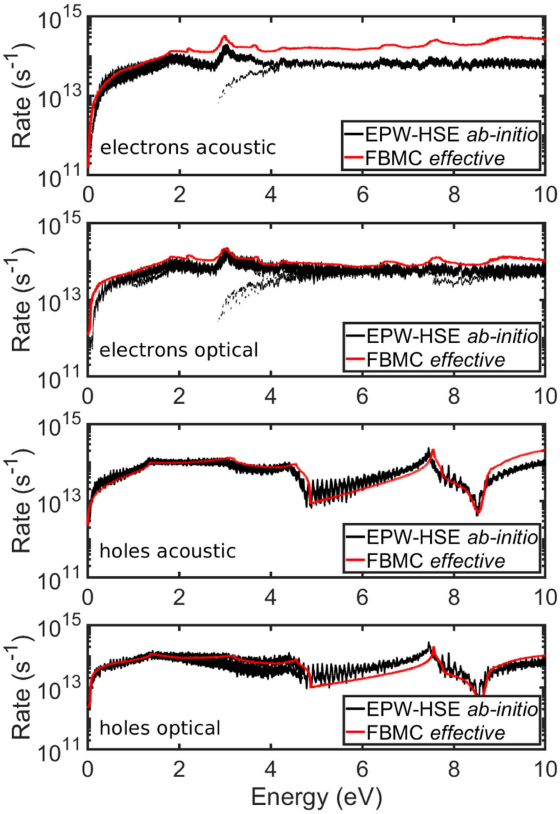

Fig. 1. Scattering rates used for the silicon FBMC3D model. The mechanisms included in the simulation are acoustic (aco) and optical (opt) phonons. The red lines are the energy-dependent rates used in the simulations. The black markers are the rates computed through DFPT using the HSE computed bands.

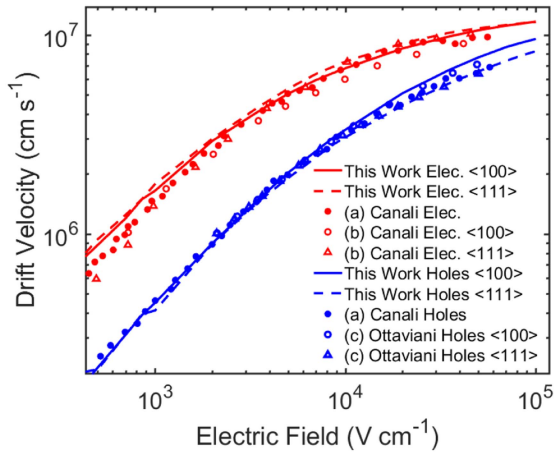

Fig. 2. Simulated and experimental velocities for electrons (red) and holes (blue) compared to experimentally obtained values from (a) Canali [30], (b) Canali [31], and (c) Ottaviani [32].

For simulating APDs, the description of the impact ionization process for electrons and holes, which is responsible for the carrier multiplication process, must also be included. In this work, the energy-dependent electron, $(R_{\mathrm{e,ii}})$, and hole, $(R_{\mathrm{h,ii}})$, impact ionization rates are approximated using the Keldysh formula [33]. The calculated impact ionization coefficients computed using the rates from (1) and (2) are compared to experimental and inferred data [34], [35], [36] in Fig. 3, showing

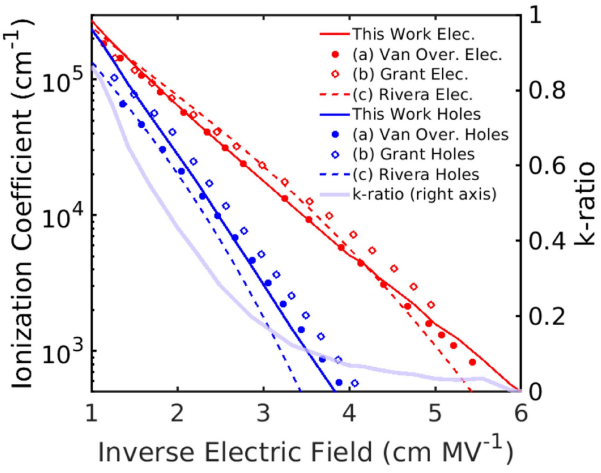

Fig. 3. Simulated and experimental impact ionization coefficients for electrons (red) and holes (blue) compared to experimentally obtained values from (a) Van Overstraetenden [34], (b) Grant [35], and (c) Rivera [36]. The k-ratio is computed as β/α. At high electric fields the k-ratio approaches 1.

good agreement with the previously published values up to $800\,\mathrm{kVcm^{-1}}$ for both electrons and holes. In this work, the electron and hole ionization coefficients are referred to as α and β, respectively.

$$R_{\mathrm{e,ii}}(E_{\mathrm{e}}) = \begin{cases} 4\times10^{12}\cdot\left(\dfrac{E_e-1.12}{1.12}\right)^{2.5}\ \mathrm{s}^{-1} & E_e > 1.12\,\mathrm{eV} \\ 0 & \text{Otherwise} \end{cases} \quad (1)$$

$$R_{\mathrm{h,ii}}(E_{\mathrm{h}}) = \begin{cases} 1\times10^{12}\cdot\left(\dfrac{E_h-1.12}{1.12}\right)^{2.5}\ \mathrm{s}^{-1} & E_h > 1.12\,\mathrm{eV} \\ 0 & \text{Otherwise} \end{cases} \quad (2)$$

B. Device Simulation

The simulations of gain, excess noise factor, and bandwidth are performed using a frozen field (FF) approximation, which assumes that the electric field profile changes negligibly from its steady-state values during the operation of the APD. This approach is valid for simulations where the number of secondary carriers generated from impact ionization events do not incur significant carrier screening effects. Thus, the simulated APDs in this work are biased well-below breakdown levels to ensure the validity of the simulations. Running simulations with the FF approximation significantly reduces the computational cost due to removing the need to repeatedly solve Poisson's equation to obtain the electric field profile.

Running simulations with FF requires first obtaining the steady-state electric field profile for a set biases. The rationale for choosing which biases to simulate is detailed in Section III-A. Using the steady-state electric field, electrons and holes are seeded at the edge of the absorber-multiplier interface, where they are subsequently energized by the sharp electric fields of the device. The average multiplication gain of the APDs is calculated using the formula:

$$\langle M\rangle = N_{\mathrm{ionizations}}/N_{\mathrm{seeded}} + 1 \quad (3)$$

where $\langle M\rangle$ is the mean value of the gain distribution, N_{ion} is the total number of ionizations incurred, and N_{seeded} is the number of seeded electrons. To enhance the statistics, N_{seeded} of 500 is used for each gain simulation.

The evaluation of excess noise factor follows a similar methodology. In this case, a single electron is injected at absorber-multiplier interface with a depth corresponding to the average depth of absorption for the wavelength of interest. For the wavelength of 350 nm, the corresponding average depth of absorption is approximately 10 nm below the surface [37]. With M_0 being the gain distribution of single electron injections, the excess noise factor, $F(M)$, can be calculated by:

$$F(M) = 1 + Var(M_0)/\langle M_0\rangle^2. \quad (4)$$

Finally, the bandwidth of the APD can be estimated by its impulse response [38], [39]. Using the same methodology as the gain simulations, the electrons seeded at the absorber-multiplier interface can be considered an impulse signal. With $i(t)$ being the time-dependent current response of the impulse signal, its frequency response, $I(f)$, can be obtained by applying the Fourier Transform, $\mathcal{F}$, on $i(t)$, as given below:

$$I(f) = \mathcal{F}(i(t)). \quad (5)$$

The 3-dB bandwidth can then be extracted from $I(f)$. It should be noted that the bandwidth obtained using this approach is the bandwidth contribution from only the multiplier region without contributions from carrier diffusion and parasitic RC delay due to the read-out electronics.

C. Device Structure

The device structure used to study the effects of fabrication variations is based on the lateral transport separate-absorber-multiplication (SAM) configuration fabricated on an SOI layer. To simulate this device structure, a quasi-2D mesh was employed. The geometrical and doping characteristics of this device, along with the electric field distribution at an arbitrary applied voltage, are presented in Fig. 5. The design of these devices is highly compatible with the existing CMOS fabrication process, making them desirable from a yield and pixel density perspective [8], [10].

The CMOS SAM APD design used for this work was inspired by Ref. [8], which exhibited favorable characteristics such as high responsivity and large bandwidth. The smallest critical dimension of Ref. [8] was 50 nm, while for the design of this work it is 250 nm, and was fabricated using a standard SOI CMOS process. Other APDs that were fabricated using CMOS 130 nm and 180 nm technology nodes were also able to achieve high bandwidth and responsivity for silicon based APDs [18], [19]. The primary objective of this design is to explore the impact that fabrication variations has on its performance, and potentially aid in the design considerations of similar technology node SiAPDs.

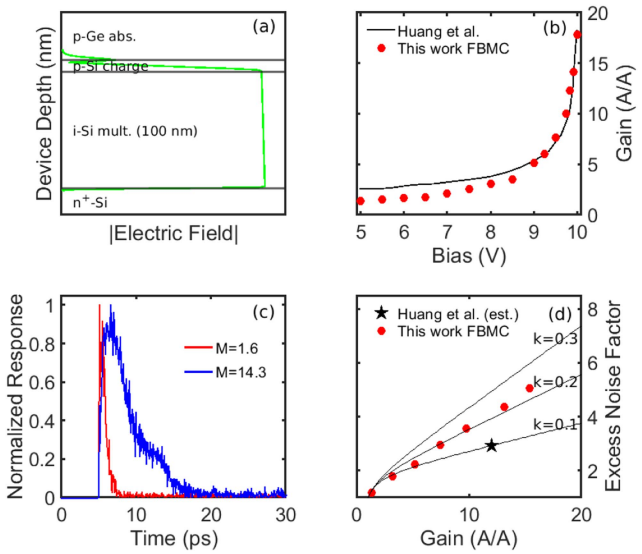

Fig. 4. Comparison of simulated and experimental data from Ref. [12]. Panel (a) shows the electric field at an arbitrary bias of the 1D geometry used to simulate the vertical SACM Ge-on-Si APD. Panel (b) shows the APD gain versus applied bias. Panel (c) shows the normalized impulse response of the APD. Panel (d) shows the simulated excess noise factor plotted against McIntyre's curves [21]. The doping (with the values of the experimental devices in parentheses) used to produce the simulation results in cm^{-3} are 1×10^{16} (1×10^{16}) in the p-Ge absorber, 1.7×10^{16} (2×10^{17}) in the p-Si charge layer, 1×10^{16} ($< 2 \times 10^{16}$) in the i-Si multiplication layer, and 1×10^{19} ($> 1 \times 10^{20}$) in the n^+-Si contact layer.

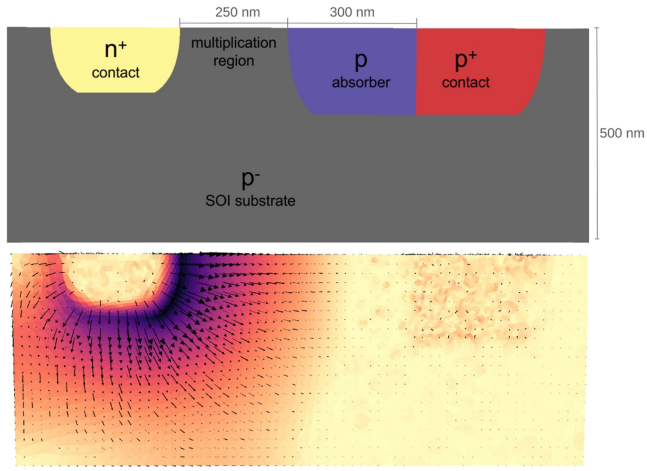

Fig. 5. The 2D geometry used to simulate the lateral-transfer SAM APD. The dimensions provided are the same dimensions given by Table I of the baseline device. When biased, the electric field radiates around the n^+ contact region, with the peak of the field occurring near the surface between the n^+ contact region and multiplication region. Darker colors indicate higher electric field magnitudes. The dimensions and doping values for.

To validate the FBMC model, we use a vertically-stacked separate-absorber-charge-multiplication (SACM) structure due to the availability of experimental data on Ge-on-Si APDs [11], [12], [13]. To simulate this structure, a simple one-dimensional (1D) model is used to represent a vertical cross-section through the device. In this structure, infrared light is absorbed in the p-type germanium absorber layer (p-Ge abs), and the photo-generated carriers diffuse and multiply in the intrinsically-doped silicon region (i-Si mult.). An example of the 1D model and its electric field when biased at an arbitrary voltage is shown in Fig. 4(a). The geometry and doping profile follow the example provided in Ref. [12], with a p-type charge layer doped at 1.7×10^{16} cm^{-3}, a 100 nm multiplication layer doped at 1×10^{16} cm^{-3}, and a n-type contact layer doped at 1×10^{19} cm^{-3}. The 1D simulation results of gain (Fig. 4(b)) and excess noise factor (Fig. 4(d)) using the FBMC3D simulator with the full band structure of silicon presents values similar to the experimental data, with gain increasing super-exponentially at an applied bias of ≈ 9.5 V, and an excess noise factor following the McIntyre curve for a k-ratio of approximately 0.2. The impulse responses of the multiplication region for an average gain of 1 and 14.3 is shown in Fig. 4(c), which demonstrates the much longer response at higher gain. A detailed study of the impact of fabrication variations on the performance a vertical SACM APDs will be published elsewhere.

To accurately seed the electrons in the quasi-2D SAM APD, the absorption profile of incident light must be considered. In those devices, the incident light is absorbed near the surface. In our model, we assume that a reflective surface is placed above the contact regions and the multiplication region. As a result, light can only be absorbed in the absorber region, similarly to the case of the SACM device. For simulating the detector performance, a monochromatic beam with a wavelength of 350 nm is assumed to be incident on the top of the device. The absorption coefficient for silicon corresponding to the incident wavelength is approximately 1×10^6 cm^{-1} [37]. Since the inverse of the absorption coefficient is much shorter than the thickness of the SOI layer, a simple Beer's law profile is assumed for photon distribution in the absorber layer, and is given by:

$$I(z) = I(0)e^{-\kappa z} \tag{6}$$

where $I(z)$ is the intensity of the illumination at a depth z into the device, and κ is the absorption coefficient and is equal to 1×10^6 cm^{-1}. At the beginning of each simulation, photo-electrons are seeded at the absorber-multiplier interface with the given Beer's law profile. This method assumes that the photo-electrons reach the multiplication region at a similar depth to where they were generated.

D. Fabrication Variations

At sub micrometer scales, minute changes to the doping concentrations and physical dimensions of an APD may alter the electric field profiles enough to significantly affect their performance. For example, it has been previously shown that slight changes to the doping profile caused by manufacturing process variations altered the breakdown voltage and bandwidth of otherwise identical SiAPDs [18]. The changes in APD performance can be attributed to the sensitivity of the ionization coefficients to the strength of the electric field, as seen in Fig. 3. Furthermore, the larger k-ratios at higher electric field strengths are correlated with higher excess noise factor [21] and lower bandwidth [22].

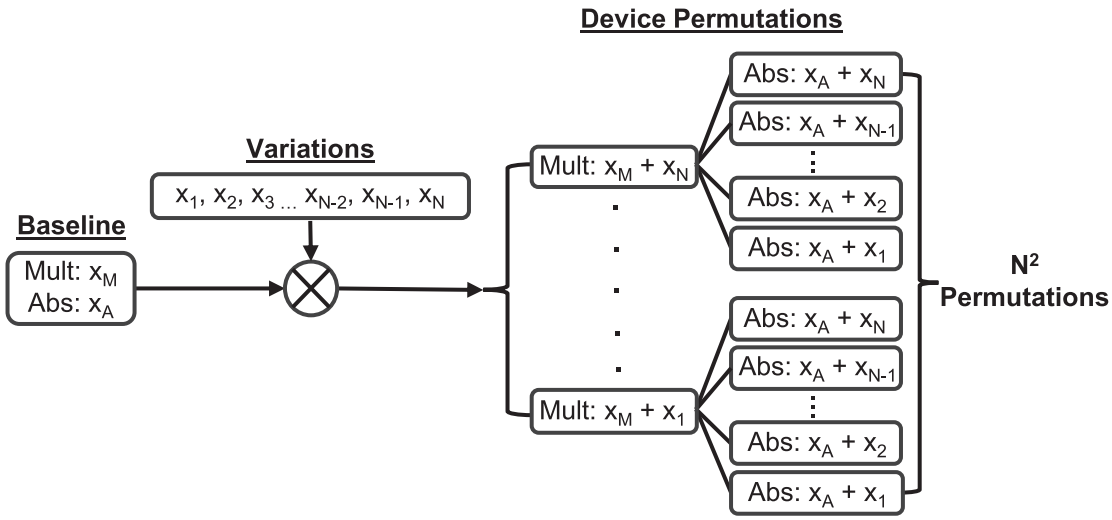

Fig. 6. Visualization of the permutations resulting from N number of applied variations to the properties (x) of the multiplication region (Mult), and the absorber region (Abs), using their baseline parameter values of x_M and x_A respectively. The variations applied to the baseline are listed in Tables II and III.

TABLE I
BASELINE DEVICE PARAMETER VALUES

Device Parameters	Parameter Value
Multiplier Width	250 nm
Absorber Width	300 nm
SOI Layer Thickness	500 nm
Multiplier Doping	5×10^{16} cm^{-3}
Absorber Doping	8×10^{16} cm^{-3}
n^+ well	1×10^{18} cm^{-3}
p^+ well	1×10^{18} cm^{-3}

TABLE II
MULTIPLIER AND ABSORBER WIDTH VARIATIONS

Width Variation	Percent Change To The Multiplier	Percent Change To The Absorber
±50.0 nm	±20%	±16.7%
±37.5 nm	±15%	±12.5%
±25.0 nm	±10%	±8.3%
±12.5 nm	±5%	±4.2%
±0.0 nm	±0%	±0.0%

The fabrication variations explored in this work are changes to the doping concentrations and widths of the multiplication and absorber regions, as well as the thickness of the SOI layer. The impact of each variation on the performance of the SAM APD is quantified by simulating different combinations of process variations applied onto a baseline device as permutations, which is depicted in Fig. 6. For example, applying N number of variations to both the baseline absorber parameter (i.e. width or doping), x_A, and the baseline multiplier parameter, x_M, results in N^2 number of permutations of different device designs. The impact of variations on absorber and multiplier widths is analyzed by performing simulations on all N^2 permutations consisting of combinations of different absorber and multiplier widths, while keeping doping concentrations at baseline values. The same analysis is performed for permutations of absorber and multiplier doping concentrations while keeping widths at baseline values. Finally, the SOI thickness is also varied while keeping both widths and dopings at baseline values.

The baseline device parameters of the SAM APD, including the doping and dimensions of the multiplier, absorber, and SOI layer, are given in Table I. The baseline dimensions of the device geometry are also shown in Fig. 5. The values of these variations were chosen to be representative of the fabrication process, while also avoiding a significant shift in the breakdown voltage of the baseline device. The values selected for the variations in widths for the multiplication and absorber region are −50 nm to +50 nm, which corresponds to a change of ±20% and ±16.67%, respectively, as shown in Table II. These values were chosen to represent the total accumulated variation in the physical dimensions during the photolithography, etching, and the annealing/diffusion processes. For example, during photolithography the illumination dose and the distance between the photoresist and the last lens of the photolithography's machinery are sources of its process variations. For the 193 nm dry lithography process the observed difference between the minimum and maximum critical dimensions was up to 10 nm [40]. The etching process of the photoresist presents another source of variability [23]. Furthermore the random trajectory of an ion during the ion implantation process also leads to variations in the placement of the dopants, which can be modeled as a Gaussian distribution. Dopant diffusion during high temperature annealing steps may further broaden the distribution, and thus effectively widening the implanted area. [41].

For doping variations, values selected for the variations in the multiplication and absorber regions of -3×10^{15} cm^{-3} to $+3\times10^{15}$ cm^{-3} correspond to a change of ±6% and ±3.75%,

TABLE III
MULTIPLIER AND ABSORBER DOPING VARIATIONS

Doping Variation	Percent Change To The Multiplier	Percent Change To The Absorber
$\pm 3\times10^{15}$ cm^{-3}	±6%	±3.75%
$\pm 2\times10^{15}$ cm^{-3}	±4%	±2.50%
$\pm 1\times10^{15}$ cm^{-3}	±2%	±1.25%
$\pm 0\times10^{15}$ cm^{-3}	±0%	±0.0%

TABLE IV
THICKNESS OF SOI LAYER VARIATIONS

Thickness Variation	Percentage Change To The Thickness
−25 nm	−5%
−50 nm	−10%
−100 nm	−20%
−150 nm	−30%
−200 nm	−40%
−250 nm	−50%

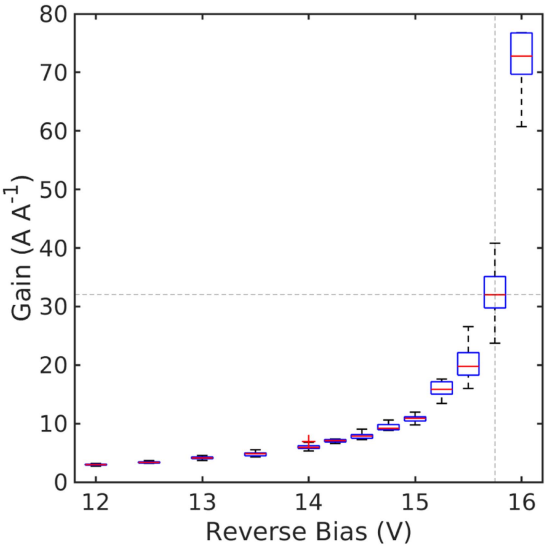

Fig. 7. The simulated gain of the baseline device reverse bias (V) curve. The baseline device's attributes are described in Table I. The intersection of the dashed vertical and horizontal lines is the median gain for the selected reference reverse bias 15.75 V, and the red crosshairs are the statistical outliers of simulation results.

respectively, as shown in Table III. These values represent the product of variations in the ion implantation and diffusion processes, which are the two main methods used to create doping profiles in semiconductor devices. During ion implantation, the random nature of the damage in the silicon crystalline structure, placement of the dopants, dopants lost due to sputtering, and their activation during the annealing process leads to variations in doping concentrations. For example, the doping concentration of boron implanted at 200 keV can decay by an order of magnitude over a depth of 300 nm. Likewise, the doping profile created by the diffusion process is variable due to the non-constant dopant diffusivity parameter [41].

The values selected for the variations in thickness of the SOI layer are −25 nm to −250 nm, which corresponds to a −5% to −50% change as shown in Table IV. The −25 nm value is representative of variations in the three major methods of manufacturing SOI wafers: Smart Cut, separation by implanted oxygen (SIMOX) and bonded silicon-on-insulator (BSOI) process of wafer-bonding-and-etch-back (BESOI). The observed difference between the minimum and maximum SOI thicknesses of the Smart Cut method is 4 nm, while SIMOX and BESOI observed a difference of 20 to 30 nm [42]. The purpose of the −250 nm variation is to emphasize the impact of varying SOI thickness.

III. RESULTS

Before analyzing the impact of fabrication variabilities, we evaluate the gain of the baseline CMOS SAM APD device with the geometry shown in Fig. 5 and the dimension and doping values given in Table I. A bias sweep was performed on the baseline device, as shown in Fig. 7, to find an appropriate reference reverse bias to apply on all permutations of the device. This bias is chosen so that the gain of all permutations is significant, but still below their breakdown voltage, which helps make clear the effects of potential fabrication variabilities. For analyzing the impact of fabrication variabilities on gain, 15.75 V was selected to be the reference reverse bias of all the following simulations.

In this work, 5 to 25 simulations were performed per permutation to obtain sufficient statistics for the gain. For each gain simulation, the methodology outlined in Section II-B was followed, with 500 photo-electrons seeded at the multiplier-absorber interface. Permutations at applied biases that observed a large amount of noise required a maximum of 25 simulations to be performed in order to achieve sufficient statistics. Permutations at applied biases that observed a very low amount of noise only required 5 simulations to be performed in order to optimize computational usage. To present the statistics of the resulting data from our simulations, boxplots were used to display the maximum and minimum values of non outliers, and the median, first, and third quartile values.

A. Gain

Changes in the gain due to the variations in the widths of the multiplication and absorber regions are explored. The computed distribution of the median gain for these permutations is presented in Fig. 8. It can be observed that the gain is highly sensitive to changes in the width of the multiplier, while changes to the width of the absorber did not produce appreciable changes to the gain. To further explore this trend, additional simulations were performed by only varying the multiplier and absorber widths of the baseline device separately. Fig. 9 shows the results of the additional simulations, showing that variations in the multiplier widths have a profound impact on gain, while varying the absorber width does not affect the gain at all.

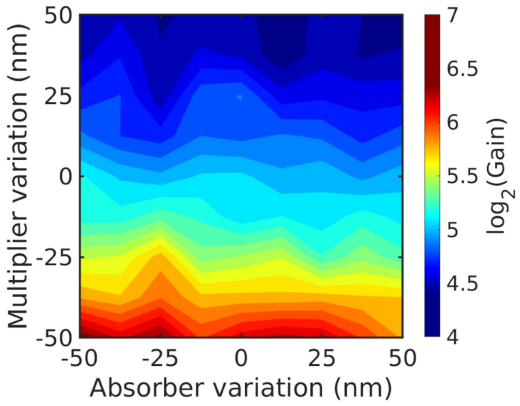

Fig. 8. 2D plot of the simulated median gain for the geometrical variations applied from Table II onto both the multiplier and absorber. The reference reverse bias of 15.75 V was applied to all permutations.

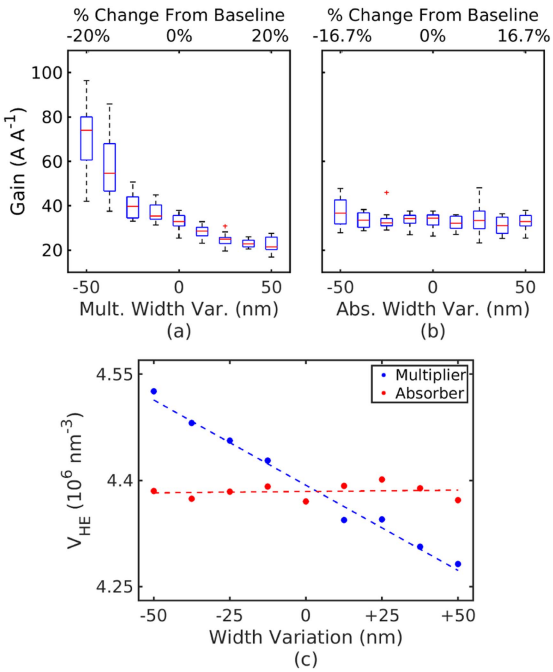

Fig. 9. The simulated results of applying the geometric variations to the multiplier (Mult.) and absorber (Abs.) separately. All simulations of the separate geometric permutations are represented by boxplots in Fig. 8(a) and (b). The red crosshairs are representative of the statistical outliers of some simulations. Fig. 8(c) plots V_{HE} as the width changes for Fig. 8(a) (blue) and (b)(red). The reference reverse bias of 15.75 V was applied to all permutations.

These trends can be explained by observing the behavior of the depletion region in the multiplier. The low doping concentration of the multiplier and higher doping concentration of the absorber causes the depletion region to be mostly confined to the multiplier. As the applied reverse bias increases, the depletion region radiates from the n^+/multiplier interface until it reaches the boundary of the absorber. The depletion region negligibly penetrates into the absorber region due to its higher doping. Thus, varying the multiplier's width has a significant effect on the electric field distribution of the device.

To quantify the changes in the electric field distribution with changes in the multiplier and absorber widths, we introduce the

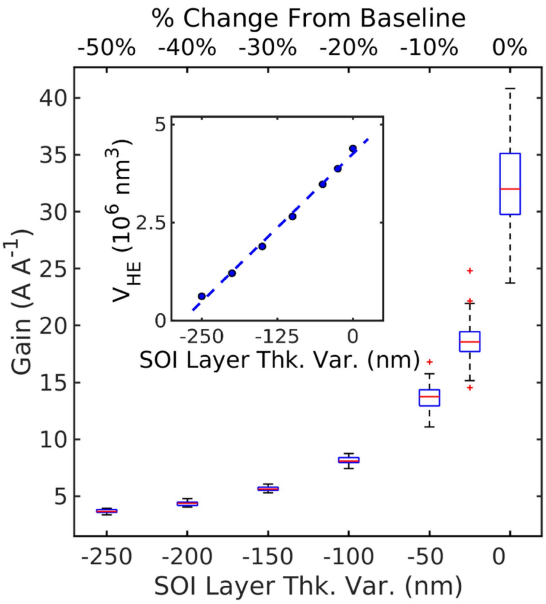

Fig. 10. Plot of the simulated median gain for the geometrical variations applied from Table IV onto both the thickness of the SOI layer. The inset displays the change of V_{HE} as the permutations in thickness are applied. The reference reverse bias of 15.75 V was applied to all permutations.

parameter V_{HE}, which is defined as the volume of the device that contains high electric field magnitudes of above 600 kV cm^{-1} at the reference reverse bias of 15.75 V. The lower bound of 600 kV cm^{-1} was selected as it corresponds to the field when β^{-1} is approximately the length of the multiplier (250 nm), and α^{-1} is approximately half the length of the multiplier as shown in Fig. 3. This indicates that carriers in these regions have a high propensity for incurring impact ionization events. V_{HE} was calculated using the following equation:

$$V_{HE} = \int_R d\vec{r} \text{ where } R = \{\vec{r} | \mathcal{E}(\vec{r}) > 600\,\text{kV}\,\text{cm}^{-1}\}. \quad (7)$$

Where $\mathcal{E}(\vec{r})$ is the magnitude of the electric field at a position $\vec{r}$ and R is the set of positions where the electric field magnitude is greater than 600 kV cm^{-1}.

Fig. 9(c) presents the calculated V_{HE} using (7) as a function of the width variations applied to the multiplier and absorber separately. Since V_{HE} correlates with higher ionization coefficients, devices with higher V_{HE} are expected to yield higher gain. This dependence is reflected by the increase in both V_{HE} and the gain as the width of the multiplier decreases as shown in Fig. 9(c) and (a), respectively. Conversely, changing the width of the absorber region does not appreciably change V_{HE} nor gain, as shown in Fig. 9(b).

The impact of SOI thickness variations on the gain is examined next. For these simulations, the widths and doping values of the multiplier and absorber are kept at their baseline values, which are given in Table I. Impact on the median gain as a function of variations in the thickness of the SOI layer are shown in Fig. 10, showing that the median gain decreases significantly as the thickness of the SOI layer is reduced. The inset of Fig. 10, which plots the V_{HE} versus variations in the thickness of the

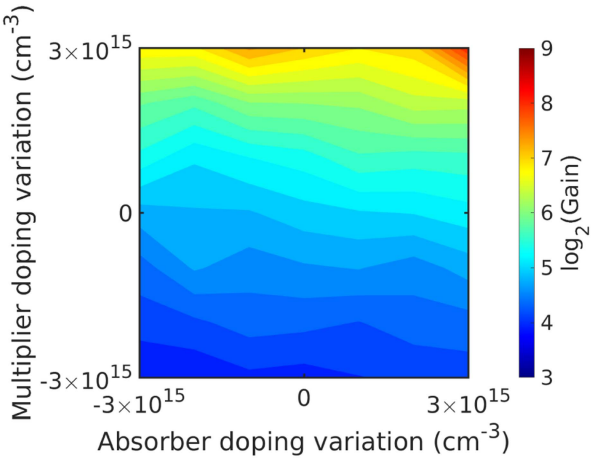

Fig. 11. 2D plot of the simulated median gain with the doping concentration variations applied from Table III onto both the multiplier and absorber. The reference reverse bias of 15.75 V was applied to all permutations.

SOI layer, shows that V_{HE} decreases as the thickness of the SOI layer decreases. Thus, reducing the SOI thickness reduces the available volume where carriers can impact ionize, which reduces the gain of the APD.

Lastly, we investigate the impact of varying the doping concentrations in the multiplication and absorber regions on the gain. The gain values of the doping permutations are plotted in Fig. 11, showing that varying the doping of the multiplier region has the dominant effect. To explore this observation, the effects of the changes in the doping concentration of the multiplier and absorber were decoupled. This was done by performing additional simulations where the changes to the doping concentration of the multiplier and absorber regions were applied separately. The results of these simulations are shown in Fig. 12. It can be seen that the gain is much more sensitive to the variations in the doping of the multiplier compared to the doping of the absorber, which matches our initial observation.

To better explain why the doping of the multiplier has such a significant effect on the gain, the PN junction characteristics of the n^+/multiplier interface, as shown in Fig. 5, is examined. The magnitude of the electric field at the n^+/multiplier interface is also the maximum electric field of the device. In 1D, the maximum electric field of such a PN diode can be expressed as [43]:

$$\mathcal{E}_{max} = \left[\frac{2qN_{\text{eff}}}{\epsilon_s}(\phi_{bi} + |V_r|)\right]^{0.5} \tag{8}$$

$$N_{\text{eff}} = \left[\frac{1}{N_a} + \frac{1}{N_d}\right]^{-1}. \tag{9}$$

Where ϕ_{bi} is the built in potential of the PN diode formed by the n^+ contact and multiplication region, ϵ_s is the permittivity of silicon, V_r is the applied reverse bias, N_a is the p-type doping concentration of the multiplication region and N_d is the n-type doping concentration of the n^+ contact.

The lowest doping concentration between N_a and N_d dominates the N_{eff} term, with higher N_{eff} resulting in a higher maximum electric field. Since the doping concentration of the multiplier is significantly lower than the n^+ contact doping, its term dominates in the calculation of N_{eff}. Thus, variations in the multiplier doping is expected to significantly affect the maximum electric field.

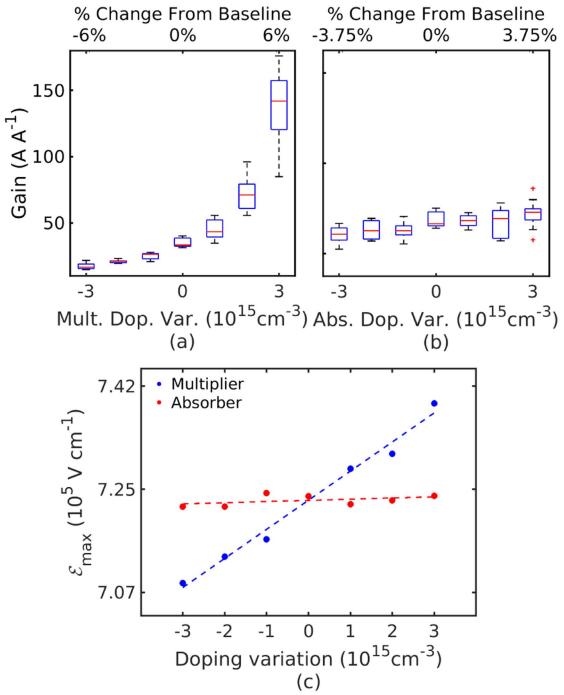

Fig. 12. The simulated results of applying the doping permutations to the multiplier (Mult.) and absorber (Abs.) separately. All simulations of the separate geometric permutations are represented by boxplots in Fig. 12(a) and (b). Fig. 12(c) displays the maximum electric field of the APD as the doping permutations are applied separately. The reference reverse bias of 15.75 V was applied to all permutations.

Fig. 12(c) shows the dependence of the maximum electric field strength as a function of the doping changes in multiplier and the absorber separately. The maximum electric field magnitude of the APD increases as the doping of the multiplier increases. Changing the doping of the absorber has a negligible effect on the magnitude of the maximum electric field. Due to the exponential relationship between the inverse of the electric field and ionization coefficients, as shown in Fig. 3, the operation of the APD is particularly sensitive to changes in the electric field due to the doping variations in the multiplier.

B. Excess Noise Factor

To analyze the impact that fabrication variability has on excess noise factor, the noise performance of a few selected devices from the set of permutations were compared to the performance of the baseline device. These devices and their deviation from the baseline device are listed in Table V. These devices were chosen for their significantly different simulated gains at the reference bias compared to the baseline device. The excess noise factors of each device were computed using the methodology given in II-B. The gain-dependent excess noise factor of each device is plotted in Fig. 13, and fitted to McIntyre's curves using least squares fitting approach. The fitted curves of the excess noise factors

TABLE V
DEVICES CHOSEN TO SIMULATE ENF AND BANDWIDTH

	Region Changed	Property	Permutation applied
Device A	Multiplier	Width	+50 nm (+20%)
Device B	Multiplier	Width	−50 nm (−20%)
Device C	Multiplier	Doping	$2 \times 10^{15}\,\mathrm{cm}^{-3}(+6\%)$
Device D	Substrate	Thickness of SOI Layer	−25 nm (−5%)

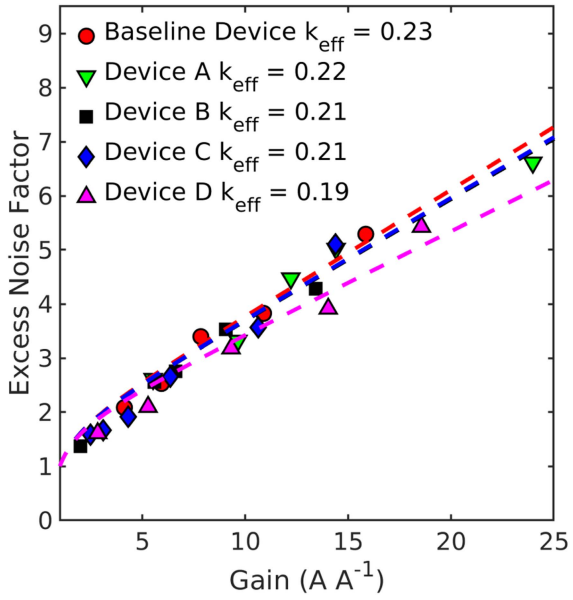

Fig. 13. The excess noise factor of the baseline device, and devices A, B, C, and D as a function of their gain. The dashed lines are their respective fitted McIntyre's curves. The excess noise factor was calculated using (4).

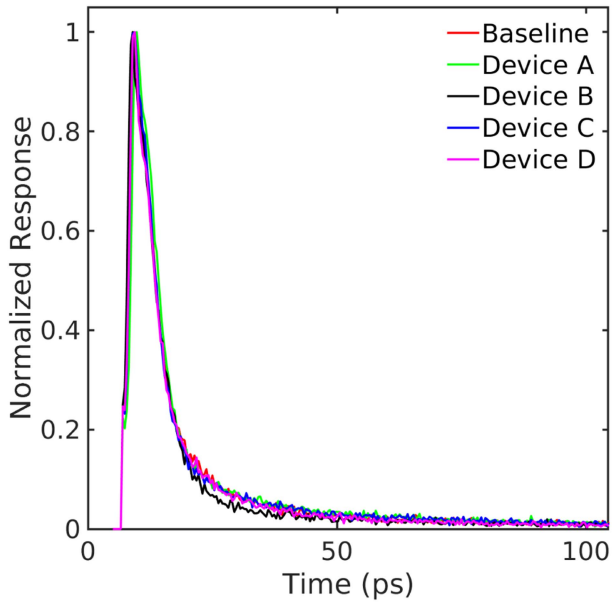

Fig. 14. Normalized impulse response comparison between the devices in Table V biased to produce a gain of roughly 5.5 A A^{-1}.

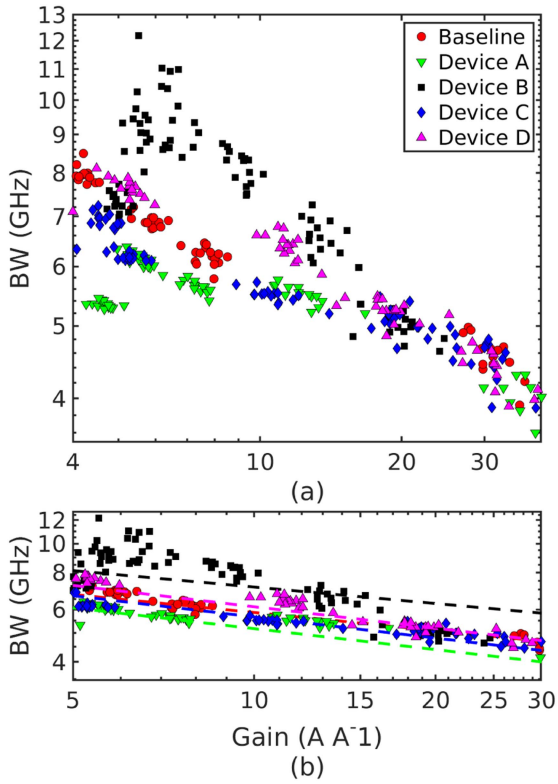

Fig. 15. The simulated −3 dB bandwidths (BW) of the baseline device and Device A-D for gains above 4 is plotted in Fig. 15(a). A first order transfer function model was used to fit the bandwidths of these devices for gains above 5 in Fig. 15(b).

shown in Fig. 13 suggest that small variations in the fabrication process do not significantly affect the k-ratio of the devices.

C. Impulse Response and Bandwidth

Optimizing the performance of APDs requires understanding the interplay between their gain and bandwidth. Generally, the bandwidth of the APDs decrease as their gain increases, which can primarily be attributed to two effects. First, impact ionization events significantly relaxes the energy of the initializing carriers, which may reduce their velocity from their saturation values and increase their transit time through the multiplier. Second, and the more important effect, is that secondary carriers of the opposite type (holes for initiating electrons and vice versa) are accelerated in the opposite direction by the field, which significantly extends the time for which carriers are transiting in the multiplier. In fact, APD breakdown, which occurs roughly when α^{-1} and β^{-1} are both equal to or less than multiplier width, can induce an infinitely long current response and may require externally "quenching" the APD for a reset [44].

The interplay between gain and bandwidth is analyzed by simulating the impulse response and the −3 dB bandwidths of the baseline device, along with the devices defined in Table V. To simulate the impulse response and the −3 db bandwidths of the devices, 500 electrons were seeded at the multiplier-absorber interface in order to isolate the contribution of the multiplier

region to the bandwidth of the device. Details of the simulation methodology are given in II-B.

Fig. 14 shows the impulse responses of the device structures outlined in Table V at a gain of approximately 5.5 $A\,A^{-1}$. This comparison was done by adjusting the bias for every device to achieve comparable gain values. The current responses show that there is not a significant change in behaviour between the devices, except in Device B, which exhibited a marginally shorter tail.

The -3 dB bandwidths of each device at varying gains were calculated by following the methodology outlined in Section II-B and are plotted in Fig. 15(a). It was observed that for gains above 5, the -3 dB bandwidths of all devices exhibited a downwards trend as the gain increased, and can be fitted with a least squares polynomial model as shown in Fig. 15(b). Based on this fit, it can be observed that throughout the gains Device B had larger -3 dB bandwidths compared to the baseline device, Device A had lower -3 dB bandwidths compared to the baseline device, while the -3 dB bandwidths of Device C and Device D did not deviate far from the baseline device. The larger relative bandwidths of Device B is due to the shorter multiplication region that leads to faster collection, while the longer multiplication width of Device A leads to a slower collection. The lack of width changes to the multiplication region prevents the -3 dB bandwidths of Device C and Device D from deviating from the baseline device.

IV. Conclusion

The impacts of fabrication variations on the gain, excess noise factor, and impulse response were examined using FBMC. These alterations consisted of geometrical changes to the width of the multiplier and absorber, and the overall thickness of the SOI layer, and changes to the doping concentration in the multiplier and absorber regions.

An APD could be designed and optimized to match the desired specifications for an application, however, it is still susceptible to the effects of fabrication variations. For example, the notable effects that fabrication variations had on the gain of the baseline device were: a 4-fold increase when the doping of the multiplier was increased by 6%, a 2-fold increase when the multiplier was shortened by 20%, and a 1.8-fold decrease when the thickness of the SOI layer decreased by 5%.

Devices that showed significant deviation from the gain of the baseline device were chosen to perform comparative simulations of excess noise factor and bandwidth. We observed that for these devices the change in the excess noise factor was minimal across all variations. However, devices with changes in their multiplier widths showed a noticeable shift in their -3 db bandwidths, while the other devices showed less pronounced differences compared to baseline.

The potential impact on the gain and bandwidths due to fabrication variabilities should be taken into account in the design of an APD as shown by the simulated results. For example if an APD was designed for very high gain applications, it would potentially be beneficial to adjust the doping to be higher than its target value. In this case this is done to reduce the fabrication of APDs that do not meet the specified gain requirements. Our work can be utilized to help guide the design of an APD against the effects of fabrication variations.

References

[1] J. C. Campbell, "Recent advances in avalanche photodiodes," *J. Lightw. Technol.*, vol. 34, no. 2, pp. 278–285, Jan. 2016.

[2] H. Hamadouche, B. Merabet, and M. Bouregaa, "Performance analysis of WDM PON systems using PIN and APD photodiodes," *Int. J. Comput. Aided Eng. Technol.*, vol. 18, no. 1-3, pp. 1–18, 2023.

[3] C. Gunn, "CMOS photonics for high-speed interconnects," *IEEE Micro*, vol. 26, no. 2, pp. 58–66, Mar./Apr. 2006.

[4] Q. Hao, Y. Tao, J. Cao, and Y. Cheng, "Development of pulsed-laser three-dimensional imaging flash LiDAR using apd arrays," *Microw. Opt. Technol. Lett.*, vol. 63, no. 10, pp. 2492–2509, 2021.

[5] V. Sharma and A. Bhardwaj, "Analysis of differential phase shift quantum key distribution using single-photon detectors," in *Proc. Int. Conf. Numer. Simul. Optoelectron. Devices*, 2022, pp. 17–18.

[6] C.-X. Zhu et al., "Experimental quantum key distribution with integrated silicon photonics and electronics," *Phys. Rev. Appl.*, vol. 17, no. 6, 2022, Art. no. 064034.

[7] A. Liu and M. Paniccia, "Advances in silicon photonic devices for silicon-based optoelectronic applications," *Physica E: Low-Dimensional Syst. Nanostructures*, vol. 35, no. 2, pp. 223–228, 2006.

[8] H. Xu, Y. Yang, J. Tan, L. Chen, H. Zhu, and Q. Sun, "High-performance lateral avalanche photodiode based on silicon-on-insulator structure," *IEEE Electron Device Lett.*, vol. 43, no. 7, pp. 1077–1080, Jul. 2022.

[9] M. McClish, R. Farrell, R. Myers, F. Olschner, G. Entine, and K. Shah, "Recent advances of planar silicon APD technology," *Nucl. Instrum. Methods Phys. Res. Sect. A: Accel., Spectrometers, Detect. Assoc. Equip.*, vol. 567, no. 1, pp. 36–40, 2006. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0168900206008655

[10] A. Rochas, A. R. Pauchard, P.-A. Besse, D. Pantic, Z. Prijic, and R. S. Popovic, "Low-noise silicon avalanche photodiodes fabricated in conventional CMOS technologies," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 387–394, Mar. 2002.

[11] Y. Kang et al., "Monolithic germanium/silicon avalanche photodiodes with 340 Ghz gain–bandwidth product," *Nature Photon.*, vol. 3, no. 1, pp. 59–63, 2009.

[12] Z. Huang et al., "25 Gbps low-voltage waveguide Si–Ge avalanche photodiode," *Optica*, vol. 3, no. 8, pp. 793–798, 2016.

[13] M. Huang et al., "Germanium on silicon avalanche photodiode," *IEEE J. Sel. Topics Quantum Electron.*, vol. 24, no. 2, 2017, Art. no. 3800911.

[14] P. Bérard, M. Couture, and R. J. Seymour, "Excess noise factor of front and back-illuminated silicon avalanche photodiode," *Proc. SPIE*, vol. 11388, pp. 68–78, 2020.

[15] Q. Liu et al., "Ultraviolet response in coplanar silicon avalanche photodiodes with CMOS compatibility," *Sensors*, vol. 22, no. 10, 2022, Art. no. 3873.

[16] J. Michel, J. Liu, and L. C. Kimerling, "High-performance Ge-on-Si photodetectors," *Nature Photon.*, vol. 4, no. 8, pp. 527–534, 2010.

[17] Y. Dong et al., "Germanium-tin on Si avalanche photodiode: Device design and technology demonstration," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 128–135, Jan. 2015.

[18] F.-P. Chou, G.-Y. Chen, C.-W. Wang, Y.-C. Liu, W.-K. Huang, and Y.-M. Hsin, "Silicon photodiodes in standard CMOS technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 3, pp. 730–740, May/Jun. 2011.

[19] M.-J. Lee, "First CMOS silicon avalanche photodetectors with over 10-Ghz bandwidth," *IEEE Photon. Technol. Lett.*, vol. 28, no. 3, pp. 276–279, Feb. 2016.

[20] W. Zhi, Q. Quan, P. Yu, and Y. Jiang, "A 45 nm CMOS avalanche photodiode with 8.4-Ghz bandwidth," *Micromachines*, vol. 11, no. 1, 2020, Art. no. 65.

[21] R. McIntyre, "Multiplication noise in uniform avalanche diodes," *IEEE Trans. Electron Devices*, no. 1, pp. 164–168, Jan. 1966.

[22] R. Emmons, "Avalanche-photodiode frequency response," *J. Appl. Phys.*, vol. 38, no. 9, pp. 3705–3714, 1967.

[23] C.-F. Chien, Y.-J. Chen, and C.-Y. Hsu, "A novel approach to hedge and compensate the critical dimension variation of the developed-and-etched circuit patterns for yield enhancement in semiconductor manufacturing," *Comput. Operations Res.*, vol. 53, pp. 309–318, 2015.

[24] M. M. Hayat, B. E. Saleh, and M. C. Teich, "Effect of dead space on gain and noise of double-carrier-multiplication avalanche photodiodes," *IEEE Trans. Electron Devices*, vol. 39, no. 3, pp. 546–552, Mar. 1992.
[25] K. G. McKay, "Avalanche breakdown in silicon," *Phys. Rev.*, vol. 94, no. 4, 1954, Art. no. 877.
[26] K. Hess, *Monte Carlo Device Simulation: Full Band and Beyond*, vol. 144. Berlin, Germany: Springer, 2012.
[27] I. Prigozhin, S. Dominici, and E. Bellotti, "FBMC3D–A large-scale 3-D Monte Carlo simulation tool for modern electronic devices," *IEEE Trans. Electron Devices*, vol. 68, no. 1, pp. 279–287, Jan. 2021.
[28] M. Zhu, M. G. C. Alasio, and E. Bellotti, "Impact of fabrication variabilities on performance of avalanche photodetectors," in *Proc. Int. Conf. Numer. Simul. Optoelectron. Devices*, 2023, pp. 109–110.
[29] M. Zhu, M. Matsubara, and E. Bellotti, "Carrier transport in cubic boron nitride: First-principles and semiempirical models," *Phys. Rev. Appl.*, vol. 20, no. 3, 2023, Art. no. 034055.
[30] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Trans. Electron devices*, vol. 22, no. 11, pp. 1045–1047, Nov. 1975.
[31] C. Canali, C. Jacoboni, F. Nava, G. Ottaviani, and A. Alberigi-Quaranta, "Electron drift velocity in silicon," *Phys. Rev. B*, vol. 12, no. 6, 1975, Art. no. 2265.
[32] G. Ottaviani, L. Reggiani, C. Canali, F. Nava, and A. Alberigi-Quaranta, "Hole drift velocity in silicon," *Phys. Rev. B*, vol. 12, no. 8, 1975, Art. no. 3318.
[33] L. Keldysh, "Concerning the theory of impact ionization in semiconductors," *Sov. Phys. JETP*, vol. 21, no. 6, 1965, Art. no. 1135.
[34] R. Van Overstraeten and H. De Man, "Measurement of the ionization rates in diffused silicon pn junctions," *Solid-State Electron.*, vol. 13, no. 5, pp. 583–608, 1970.
[35] W. Grant, "Electron and hole ionization rates in epitaxial silicon at high electric fields," *Solid-State Electron.*, vol. 16, no. 10, pp. 1189–1203, 1973.
[36] E. C. Rivera and M. Moll, "Study of impact ionization coefficients in silicon with low gain avalanche diodes," *IEEE Trans. Electron Devices*, vol. 70, no. 6, pp. 2919–2926, Jun. 2023.
[37] C. Jacoboni, C. Canali, G. Ottaviani, and A. A. Quaranta, "A review of some charge transport properties of silicon," *Solid-State Electron.*, vol. 20, no. 2, pp. 77–89, 1977.
[38] M. M. Hayat et al., "Gain-bandwidth characteristics of thin avalanche photodiodes," *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 770–781, May 2002.
[39] M. Moresco, F. Bertazzi, and E. Bellotti, "GaN avalanche photodectors: A full band Monte Carlo study of gain, noise and bandwidth," *IEEE J. Quantum Electron.*, vol. 47, no. 4, pp. 447–454, Apr. 2011.
[40] J. Lorenz et al., "Process variability–technological challenge and design issue for nanoscale devices," *Micromachines*, vol. 10, no. 1, 2018, Art. no. 6.
[41] J. Plummer and M. Deal, *Silicon VLSI Technology Fundamentals, Practice and Modeling*. Englewood Cliffs, NJ, USA: Prentice Hall, 2000.
[42] X.-Q. Feng and Y. Huang, "Mechanics of smart-cut technology," *Int. J. Solids Struct.*, vol. 41, no. 16-17, pp. 4299–4320, 2004.
[43] C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, vol. 2. Upper Saddle River, NJ, USA: Prentice Hall, 2010.
[44] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Appl. Opt.*, vol. 35, no. 12, pp. 1956–1976, 1996.

Open Access funding provided by 'Politecnico di Torino' within the CRUI CARE Agreement