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Fast Overcurrent Protection for Direct Drive Cascode GaN HEMT Semiconductors Based on Industrial Gate Drivers

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***Abstract*—Gallium nitride high electron mobility transistors exhibit excellent switching and conduction performance. However, their adoption in safety-critical applications is subject to concerns about their capability to withstand severe overcurrents. Therefore, fast and reliable overcurrent protections are needed to guarantee the safe operation of the power switches. The conventional desaturation protection methods, widely used for MOSFETs and IGBTs, do not match with the reduced short-circuit capability of new GaN HEMTs semiconductors. To address this issue, this paper proposes a fast overcurrent protection scheme specifically designed for direct drive cascode GaN HEMT. The proposed solution uses an industrial gate driver along with a few additional components, leveraging the measurement of the conduction voltage of the cascode MOSFET as an indirect indicator of the device current with very good precision and reduced intervention time. The effectiveness of the proposed overcurrent protection scheme is supported by experimental results.**

***Index Terms*—DESAT, Overcurrent Protection, WBG, Wide Bandgap Semiconductors, GaN.**

I. Introduction

In recent years, gallium nitride high electron mobility transistors (GaN HEMTs) have gained more and more interest due to their superior characteristics compared to their silicon (Si) counterparts. Specifically, they offer lower switching losses, reduced conduction resistance, and improved thermal conductivity [1]. All these favourable characteristics come at a comparable production cost, making GaN HEMT devices an attractive solution for modern power converters. However, the penetration of this technology in safety-critical applications, such as automotive [2]- [4] and aerospace, is hindered by concerns regarding its reliability. In this context, the implementation of robust and fast overcurrent protections is mandatory for guaranteeing the secure and reliable operation of such devices. Although current sensors provide accurate current protection during overloads, their restricted bandwidth is inadequate for impulsive overcurrent events, such as short circuits. In the case of short circuit events, semiconductors may undergo a rapid increase in junction temperature, potentially resulting in catastrophic failure.

While traditional silicon based semiconductors such as Si IGBTs have a short-circuit withstand time (SCWT) that can exceed 10μs [5], this value drops to less than 2μs in the case of wide bandgap devices such as SiC MOSFET [5], [12]. However, in the case of GaN HEMT devices, this value becomes critical, being less than 1μs [10], [14]. Such low SCWT is the result of a high power density combined with a low thermal capacitance of the die, resulting in a sudden junction temperature rise in case of overcurrents. Therefore, when dealing with power semiconductors, it is of paramount importance to implement fast overcurrent protections able to safely turn off the component before overcoming its SCWT. The prevailing guard technique in case of faults leading to sudden increases in current is the desaturation (DESAT) protection. This technique utilizes the device's conduction voltage as an indirect indicator of its current and it is widely used for both Si IGBTs and SiC MOSFETs [6] - [13]. Most commercial ICs (Integrated Circuit) gate drivers already integrate DESAT protections, allowing the power switch to be safely turned off with response times typically within a few microseconds. This has proven to be sufficient in the case of Si and SiC based devices. However, in the case of GaN devices, this action time is not adequate to safeguard the device. This critical requirement poses a challenge to the adoption of commercially available IC gate drivers in power converters utilizing GaN devices.

To address this challenge, this paper proposes a rapid overcurrent protection system specifically designed for

the new generation of direct drive cascode GaN HEMTs devices. This protection system utilizes a commercial IC gate driver with a few additional components, offering a viable solution to the dilemma posed by GaN devices' low SCWT.

This paper is organized as follows. In Section II the main overcurrent protection methodologies available in the literature for power semiconductors are presented, while Section III described the structure and the main characteristics of cascode GaN HEMT devices. In Section IV a fast overcurrent protection methodology for cascode GaN HEMT devices is proposed. In Section V the proposed solution is experimentally validated on a half-bridge GaN converter. Finally, Section VI summarizes the benefits of the proposed solution and provides suggestions for future improvements.

II. Fast Overcurrent Protection of Power Semiconductors

In the literature, multiple techniques have been explored to protect GaN converters against impulsive short-circuit overcurrents.

As mentioned previously, DESAT-based protections are extensively employed in commercial power converters utilizing both Si and SiC power semiconductors. The DESAT solution uses the device's conduction voltage, as an indirect indicator of its current. When the conduction voltage ($v_{DS,on}$) overcomes a specific threshold, after a designated blanking time an overcurrent event is triggered and the switch is commanded in the off state performing a controlled turn off. This turn off is normally referred to as "soft turn off" as the device is turned off at a reduced speed thus avoiding excessive commutation overvoltages due to the fast current slew rate. While DESAT is commonly used for IGBTs and SiC MOSFETs, its application in GaN devices has been recently explored in literature [6] - [11]. However, this technique presents some important drawbacks especially when implemented on GaN devices. The device conduction characteristic, especially in GaN devices, is highly temperature-dependent, thus anticipating or delaying the device protection with respect to the desired current threshold. Furthermore, as GaN is a relatively new technology, it is still affected by large parametric dispersion compared to other more mature technologies such as Si, therefore additional margins on the current intervention level must be taken. Additionally, to protect the DESAT voltage sensing circuit from the high voltage on the component during the off state, a high rated voltage diode is required, with a threshold voltage that in turn is affected by its junction temperature and the parametric dispersion.

Therefore, alternative fast overcurrent techniques specifically designed for GaN have been presented in the literature. One of the most promising solutions involves monitoring the device current derivative (di/dt) using a pulsed current sensor in conjunction with a band-pass filter to detect fast current changes that are caused by short circuit events [15]. Despite its effectiveness, this solution needs many discrete components, leading to a decrease in power density and a cost increase.

An alternative solution involves the use of the loop stray inductance (L_{stray}) and stray resistance (R_{stray}) as indicators of leg current derivative and amplitude. While this approach holds potential, the implementation and estimation of parasitic elements become increasingly challenging as stray elements are minimized. In [20] a fast overcurrent protection for e-mode GIT GaN is presented. This technique involves monitoring the gate-source voltage (v_{GS}) to estimate the device drain current. However, it relies on the knowledge of the internal device parameters, which are often not readily available from datasheet information.

Alternatively, few GaN switches with integrated current sensors are available on the market, enabling fast and precise current short circuit detection [16], [17]. It is important to emphasize that almost all the proposed protection methods are targeting e-mode GaN (with the exception of [15]), while the goal of this paper is to propose an efficient, cost-effective, precise, and reliable overcurrent protection solution for direct drive cascode GaN devices.

III. Target Direct Drive Cascode GaN HEMT

It is well known that the Si IGBT and SiC MOSFET have a vertical structure. Due to the complexity of GaN substrates manufacturing [21], the GaN devices with a vertical structure are still very expensive. Therefore, at this moment the majority of the commercially available GaN devices adopt a lateral structure [21].

Typically, the GaN layer is grown using techniques like metalorganic chemical vapour deposition (MOCVD) [23] or molecular-beam epitaxy (MBE) [24] on a more economical Si substrate. Therefore, existing manufacturing processes, expertise, and equipment used for Si MOSFET production can be leveraged, leading to significant cost reductions. GaN on Si has become the standard technology structure for GaN power devices [22] ensuring low production costs and enabling them to compete effectively in the market, even against well-established technologies.

The fundamental structure for GaN switches is the normally-on depletion devices (d-mode) illustrated in Fig.1. However, a challenge with d-mode devices is that it is naturally in the ON state, requiring a negative voltage gate-to-source to turn it OFF [21]. This characteristic poses a safety concern in power electronics, where normally-OFF devices are preferred, especially during startup or in the event of a failure when the auxiliary power supply is disabled.

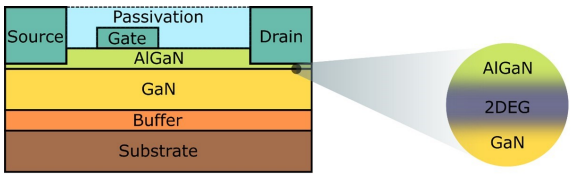


Fig. 1: d-mode normally on GaN layer stucture

To overcome this issue of the d-mode GaN HEMT, the cascode configuration is typically adopted by integrating a low

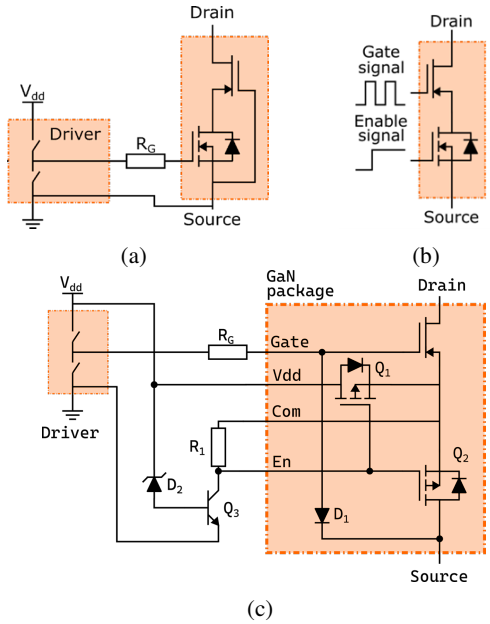


Fig. 2: (a) Depletion GaN in standard cascode configuration. (b) Depletion GaN in direct drive cascode configuration. (c) Direct drive cascode configuration GaN (V08TC65S1A2 from VisIC Technologies).

voltage Si MOSFET in series configuration to the GaN HEMT. In particular, the direct drive cascode configuration variant is becoming popular. In the standard cascode arrangement, the device is commanded ON and OFF by driving the series MOSFET, as shown in Fig.2a. This has the advantage of the use of standard gate driver voltage levels (i.e. comparable with Si MOSFET). However, this configuration degrades the switching performance of d-mode GaN due to the introduction of the commutation losses of the Si MOSFET (including reverse recovery).

In the direct drive cascode configuration, the GaN is directly driven and the series MOSFET only guarantees the safety acting as enable for the commutation, as reported in Fig.2b. This arrangement does not alter the commutation performance of the GaN switch. The available implementations of the two solutions depend on the different manufacturers. The target GaN HEMT for this paper is the direct drive cascode V08TC65S1A2 GaN HEMT (VisIC Technologies) that is shown in Fig.2c. It is possible to notice that the diode D_1 and switches Q_1 and Q_2 are integrated in the GaN package to provide negative gate voltage at the d-mode GaN die. In this way, it is possible to drive the GaN switch using standard gate-driver with positive output voltage, for the selected switch 0V in OFF state and 15V in ON state are required. Moreover, an external circuit providing the under voltage lock out (UVLO) function is added. Q_1 and Q_2 are p-channel Si MOSFET, the pull-up resistance R_1 ensure to keep them in the OFF state.

IV. Proposed Fast Overcurrent Protection

A simplified schematic of the proposed overcurrent protection circuitry is shown in Fig.3a, where the direct drive GaN HEMT is driven by the UCC21750, a commercial gate driver widely employed in industrial and automotive applications [25]- [26]. Although this driver is specifically designed for IGBT and SiC MOSFET, it can be used also for direct drive d-mode GaN HEMT devices as well.

The main advantage of a commercial gate driver is that it already integrates most of features required by most applications, such as galvanic insulation, high common mode immunity, under-voltage detection, soft turn-off, temperature monitoring via a thermistor, input PWM signals glitch filter, DESAT protection and so on. In this case, the standard DESAT protection of the driver has been modified, as shown in the schematic. Instead of monitoring the conduction voltage of the GaN HEMT device, the conduction voltage of the cascode Si MOSFET Q_2 is employed.

The cascode Si MOSFET is therefore used as a shunt resistor to monitor the GaN current without introducing additional parasitics into the commutation loop. This brings additional advantages: 1) the voltage across the MOSFET Q_2 remains low during the normal switching operation of the GaN HEMT and at most rises up to 10V when the gate driver is not powered, and consequently, no high voltage diode is needed to protect the conduction voltage measurement system, 2) Q_2 is maintained in ON state during the normal GaN operation and therefore there is no need to filter out disturbances created by the device commutation, 3) the low voltage Si MOSFET has better thermal stability and lower parametric dispersion compared to the GaN HEMT, so its conduction resistance is more stable (i.e. it is possible to set more accurate current intervention levels).

The conduction voltage of the cascode MOSFET is measured by the LTC6752, a precise and fast voltage comparator that triggers at a preset level (i.e. current in the MOSFET). When the output of the voltage comparator goes in a high state, it triggers the DESAT pin of the gate driver, which after a preset DESAT propagation delay time performs a soft turn-off of the device.

The delay introduced by the comparator, the leading edge blank time (time during which the gate driver forces to zero the voltage of the DESAT pin following the turn on of the power device) and the DESAT propagation delay time are summarized in Table I.

TABLE I: Intervention times of the IC gate driver and comparator.

Component	Delay Type	Delay Time (ns)
Gate Driver UCC21750	Leading Edge Blank Time (t_{LEBT})	200
	DESAT Propagation Delay ($t_{DESAT,OFF}$)	300
Comparator	Comparator Delay ($t_{COMPARATOR}$)	20

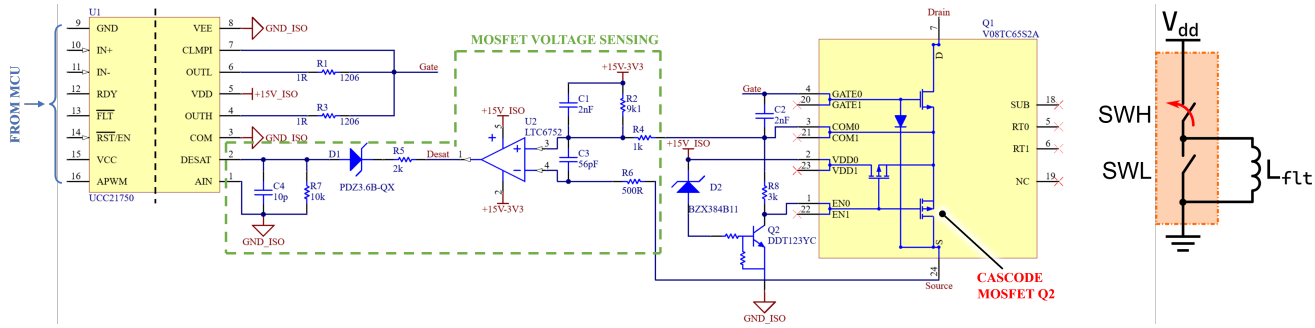


Fig. 3: (a) Simplified schematic of the proposed overcurrent protection solution. (b) Overcurrent testing principle, with the high side switch turned on different values of inductance for fault emulation.

A. Simulation Results

A SPICE simulation is performed to evaluate the performance of the proposed solution. The simulation uses accurate SPICE models of the GaN HEMT switch (i.e. V08TC65S1A2), of the gate driver (i.e. UCC21750), and of the comparator (i.e. LTC6752). In particular, the gate driver model takes into account the complex internal logic of the IC gate driver including its behaviour during the desaturation protection intervention. The voltage comparator is configured to trigger at a current of 240A corresponding to a voltage on the cascode MOSFET of 326mV, this is obtained by properly tuning R2 and R4. The fault condition is emulated by closing the power switch on an inductive load (L_{flt}) of 5μH as shown by the functional schematic in Fig.3b.

The results are shown in Fig.4, where i_d is the drain current of the device, v_{ds} is the drain-source voltage of the device, v_{meas} is the measured voltage drop across the low-voltage MOSFET and v_{DESAT} is the voltage at the DESAT pin of the driver.

As soon as the power GaN device is commanded in the on state at $t = 0$, the current in the switch increases and the voltage across cascode MOSFET starts increasing as well. Initially, the voltage at the DESAT pin of the gate driver is forced to zero during the initial leading edge blank time (t_{LEBT}). After 200ns, the DESAT pin is released and its voltage rises to around 7.5V. When the current in the cascode MOSFET reaches 240A, the comparator triggers and the voltage at the DESAT pin is brought to about 10.5V, thus triggering the DESAT protection of the IC gate driver. According to the datasheet, the desaturation protection of the IC gate driver is triggered when the voltage on the DESAT pin exceeds 9.15V. After a DESAT propagation delay time $t_{DESAT,OFF}$ of 300ns that consists of the sum of a 140 ns deglitch time filter and 160ns execution time (worst case condition), the IC gate driver performs a soft turn off of the device, thus avoiding excessive overvoltages due to the commutation at high current. At this point, the switch remains open and the fault condition is communicated to the main control unit (e.g. control microcontroller) by lowering the $\overline{FLT}$ pin of the IC gate driver located on the control logic side.

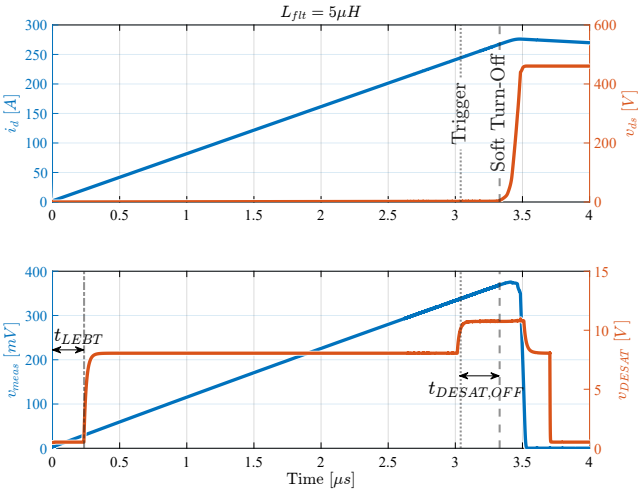


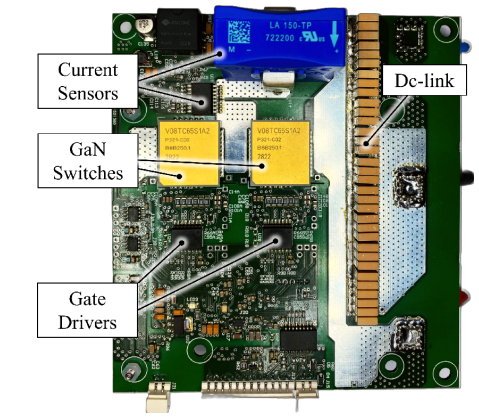
Fig. 4: SPICE simulation of the proposed protection system showing its operation following an overcurrent detection.

V. Experimental Validation

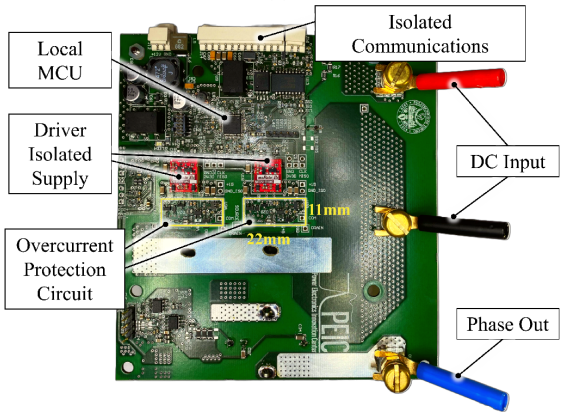
The proposed overcurrent protection has been tested on a two level, half-bridge converter consisting of two VisIC V08TC65S1A2 GaN HEMT (same as in simulation), having a rated breakdown voltage of 650V and a rated current of 200A @T_C=25°C. The power converter is shown in Fig.5a and Fig.5b. The two GaN devices, together with the IC gate driver, are visible in Fig.5a, while the main control MCU is visible in Fig.5b.

The overcurrent protection is tested by turning on the high side switch on an inductive load L_{flt}, thus emulating the fault condition, as previously shown in 3b. The GaN leg is supplied with a constant DC voltage V_{dd} of 400V, while different values of L_{flt} inductance have been used for the tests. The experimental results are summarized in Fig.6.

In Fig.6a, a L_{flt} of 17.6μH is used to emulate the fault condition. In this case, when the high-side switch is turned on, its current starts rising at around 22A/μs. As soon as the



(a)

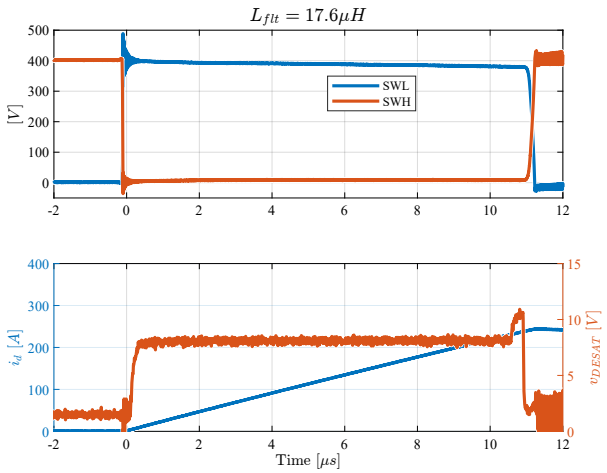


(b)

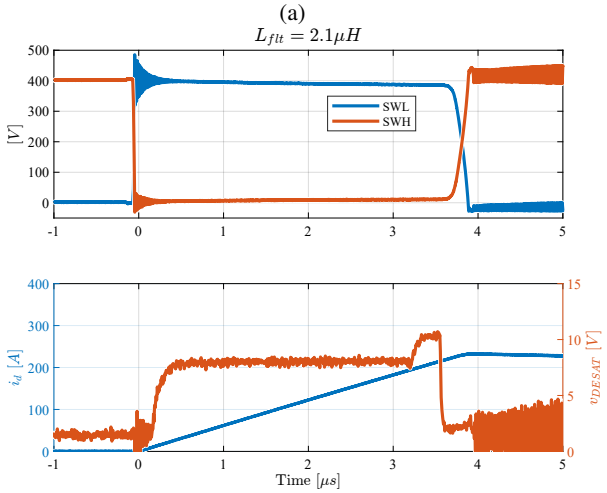
Fig. 5: (a) Bottom view of the two-level inverter leg showing the two are GaN 650V/200A V08TC65S1A2 from VisIC. (b) Top view of the two-level inverter leg.

voltage across the cascode MOSFET reaches approximately 326mV, the comparator triggers with a delay of about 20ns and the DESAT pin of the IC gate driver goes from 7.5V to 10.5V, thus starting the desaturation protection procedure of the gate driver. After a $t_{DESAT,OFF}$ of around 300ns (given by the sum of the deglitch time and the execution time), a soft turn off is performed. It must be highlighted that this delay is an inherent characteristic of the IC gate driver and can not be externally reduced. After the $t_{DESAT,OFF}$, the gate driver performs a soft turn-off of the power device and communicates the fault to a microcontroller (MCU). In this case, the peak current reached in the switch during the fault condition is 243A.

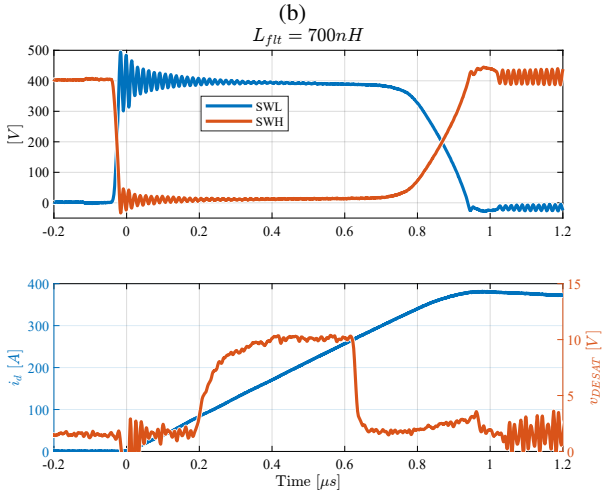
In Fig.6b shows the same test, but using for L_{flt} a value of only 2.1μH to emulate a more severe fault condition. As expected, in this case the current slew rate increases to 157A/μs. However, the IC gate driver DESAT pin is triggered when the current in the cascode MOSFET is only 213A. This premature triggering is due to the contribution of the parasitic inductance of the MOSFET that causes an additional voltage drop on the device due to the high current slew rate. The



(a)



(b)



(c)

Fig. 6: Overcurrent protection operation for different values of L_{flt}. Top plot: voltage across the power switches v_{DS} (V). Bottom plot: output current i_d (A) and voltage measured at the DESAT pin of the driver UCC21750 (refer to Fig. 3a). a) L_{flt}=17.6 μH, b) L_{flt}=2.1 μH, c) L_{flt}=700nH.

equivalent circuit of the cascode MOSFET is reported in Fig. 7, consequently the conduction voltage of the device can be expressed as in (1).

$$v_{meas} = R_{MOS} \cdot i_d + L_{\sigma,MOS} \cdot \frac{di_d}{dt} \tag{1}$$

Considering that from the datasheet R_{MOS} is 1.25mΩ, it is possible to estimate that $L_{\sigma,MOS}$ value is around 1nH. In this case, the peak current during the fault condition is limited to 227A.

The results from Fig.6c are obtained by further reducing L_{flt} to only 700nH. Due to the high current slew rate of 380A/μs, the comparator is triggered immediately (high voltage drop on the parasitic inductance of the cascode MOSFET). However, during the initial leading edge blank time t_{LEBT} of the IC gate driver, the DESAT pin is kept to zero. After 200ns, the DESAT pin is released and this starts the desaturation procedure of the gate driver that performs a soft turn off of the switch after around 300ns. In this case, the peak current in the power switch reaches 380A. Different L_{flt} values have been tested and the results are summarized in Table II, where the following parameters have been evaluated:

- di_d/dt: drain current derivative during the fault condition.
- t_{trg}: time after which the comparator triggers following turn on of the switch.
- I_{trg}: current at which the the comparator triggers.
- $I_{flt,max}$: peak current reached in the switch during the fault condition.

It is possible to note that when the current slew rate overcomes 326A/μs, the voltage drop across $L_{\sigma,MOS}$ is always higher than the 326mV trigger value, so the comparator is immediately triggered. However, there is still a minimum intervention time that is given by the sum of t_{LEBT} and $t_{DESAT,OFF}$. This minimum intervention time is an intrinsic characteristic of the IC gate driver and can not be reduced.

The data reported in Table II are graphically represented in the plot shown in Fig.8.

Lower L_{flt} values below 700nH have been tested, however, the protection circuit proved ineffective in safeguarding the switch. The cause of the failure remains unclear, as it can be due to multiple reasons such as the overcoming of the SCWT of the switch, potential failures in other components (such as the auxiliary power supply of the gate driver), or an improper turn off procedure during the current fault.

TABLE II: Intervention time tests

L_{flt} (μH)	di_d/dt $(A/\mu s)$	t_{trg} (μs)	I_{trg} (A)	$I_{flt,max}$ (A)
17.6	21.74	10.66	231	243
10.5	36.01	6.01	216	236
6.3	60.07	3.25	195	231
2.1	156.7	0.73	114.5	227
1.4	238.0	0.33	72.5	239
0.7	415.6	0	0	380

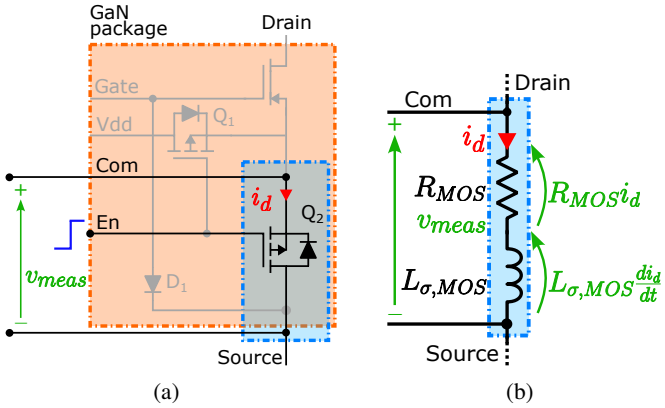


Fig. 7: (a) Parasitic. (c) Parasitic equivalent circuit.

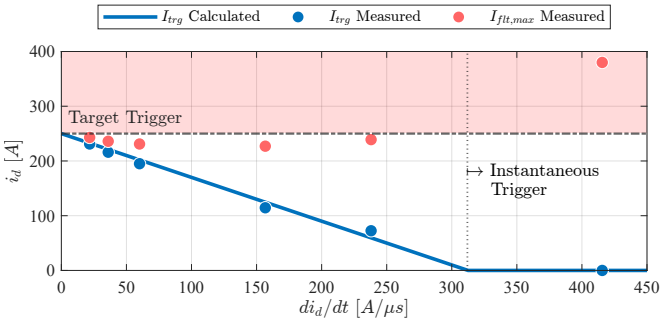


Fig. 8: Intervention curve of the proposed overcurrent protection system.

VI. Acknowledgments

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VII. Conclusions

In this paper, a fast overcurrent protection system targeting direct drive cascode GaN HEMTs devices has been presented and tested. The main benefits of the proposed approach can be summarized as follows:

- It can be implemented on standard IC gate drivers that already integrate all the advanced functionalities required by modern power electronic applications, including the functional safety aspect.
- Sensing the voltage on the cascode MOSFET enables to eliminate the high voltage clamping diode thus performing a more fast and accurate voltage sensing.
- The conduction resistance of the cascode Si MOSFET [27]- [28] is less sensitive to the temperature with respect to the GaN on-state resistance [29], resulting in a more accurate current intervention level.

- The parasitic inductance of the cascode MOSFET can be leveraged to trigger in advance the overcurrent protection, thus gaining precious time.
- As the cascode MOSFET does not switch, its conduction voltage remains relatively noise-free, eliminating the need for heavy filters and consequent delays.

The main drawback of the proposed solution is the inherited delay of the IC gate driver that does not allow to reduce the desaturation intervention time below a certain value. This did not allow to protect the power switch for L_{flt} lower than 700nH. Future work will be performed with different gate drivers exhibiting shorter intervention times.

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